

## 40-44GHz Up converter

### GaAs Monolithic Microwave IC

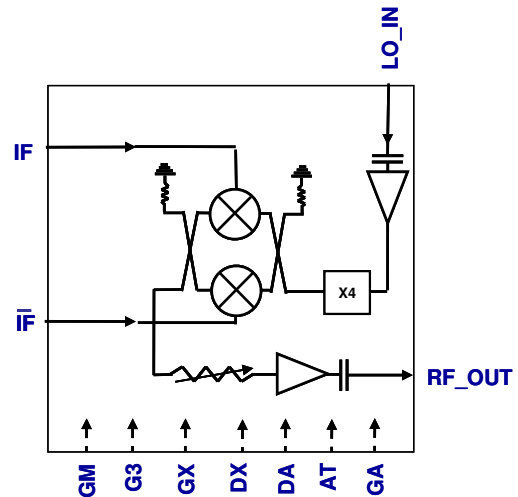
#### Description

The CHU2299-99F is an up converter multifunction chip, which integrates LO X4 multiplier, a balanced cold FET mixer and a RF amplifier with gain control.

It is designed for a wide range of applications, from military to commercial communication systems.

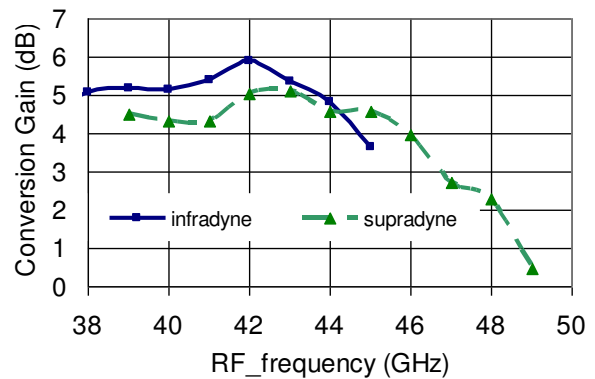
The circuit is manufactured with a power pHEMT process, 0.15 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



#### Main Features

- 40-44GHz RF bandwidth
- 5dB conversion gain
- 20dB of gain control
- x4 LO frequency multiplier
- 16dBm output IP3
- DC bias: Vd = 4V @ Id = 250mA
- Chip size 3.97x2.25x0.1mm



#### Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	40		44	GHz
F <sub>LO</sub>	LO frequency range	9.5		11.5	GHz
G <sub>c</sub>	Conversion gain		5		dB

## Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	40		44	GHz
F <sub>LO</sub>	LO frequency range	9.5		11.5	GHz
G <sub>c</sub>	Conversion gain @min. attenuation		5		dB
ΔG	Gain control range		20		dB
P <sub>LO</sub>	LO Input power		1		dBm
NF	Noise figure at gain max Noise figure all case		13 27		dB
OIP3	Output IP3@ min. attenuation Output IP3@ max. attenuation		16 4		dBm
RL	RF & LO Return Loss		12		dB
4xF <sub>LO_1k</sub>	4xLO leakage on RF port @min. Att.		-5		dBm
DX, DA	LO multiplier, buffer and RF amplifier biasing		4		V
GM	Mixer DC gate biasing		-0.6		V
G3	LO buffer gate biasing		-0.3		V
GX	Multiplier gate biasing		-1.2		V
GA	RF amplifier gate biasing		-0.5		V
AT	Attenuation voltage control	-1.5		0.5	V
Id	Drain current		250		mA

Electrostatic discharge sensitive device observe handling precautions!

These values are representative of chip on board measurements with an external 180° hybrid balun between IF & IFb.

## Absolute Maximum Ratings <sup>(1)</sup>

Tamb.= +25°C

Symbol	Parameter	Values	Unit
DX, DA	LO multiplier, buffer and RF amplifier biasing	4.5	V
Id	Drain bias current	310	mA
G3, GA	Amplifier gate biasing	-2; +0.6	V
GX, GM	Multiplier and mixer gate biasing	-2; +0.6	V
AT	Attenuation voltage control	-2	V
P_LO	Maximum peak LO input power overdrive <sup>(2)</sup>	10	dBm
Pin_RF	Maximum peak RF input power overdrive <sup>(2)</sup>	17	dBm
T <sub>j</sub>	Junction temperature	175	°C
T <sub>a</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +155	°C
R <sub>Th</sub>	Thermal resistance, Tback side = +85°C, Ptotal = 1 W	73	°C/W

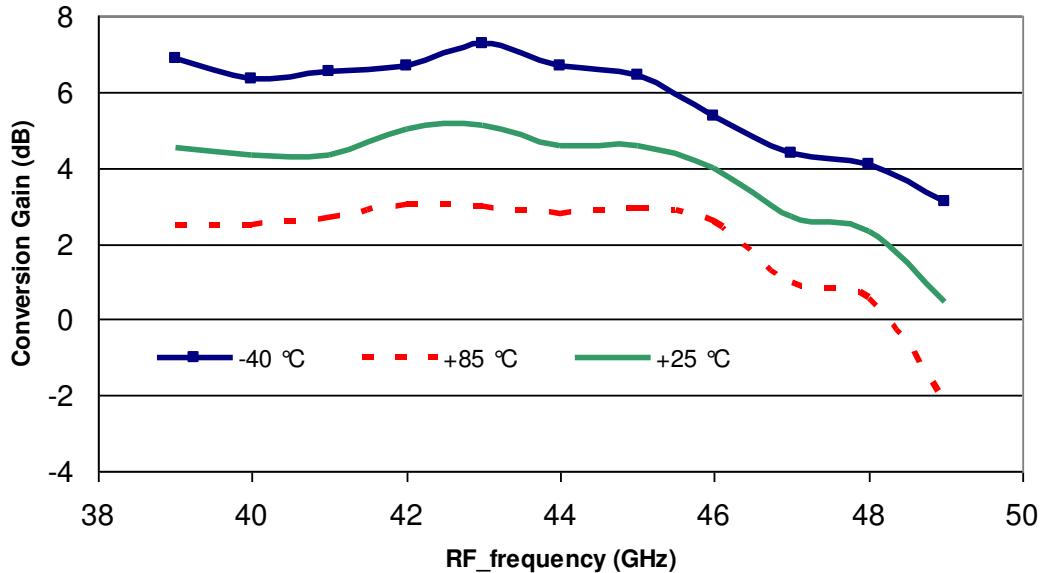
<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage

<sup>(2)</sup> Duration < 1s

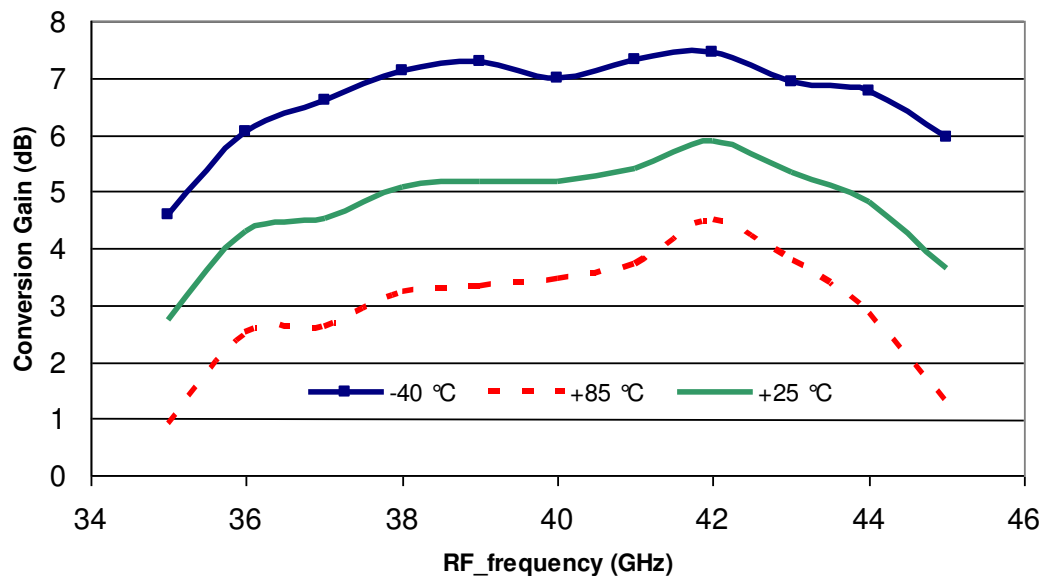
**Typical chip on board Measurements in Temperature**

DX = DA = 4V, GA = -0.5V, GM = -0.6V, G3 = -0.3V, GX = -1.2V, P\_LO = 1dBm.  
 These values are representative of onboard measurements as defined on the paragraph "Evaluation mother board". The losses are de-embedded.

**Conversion Gain versus RF frequency & temperature**  
 RF= 4LO+IF; IF = 2GHz; AT = -1.5V



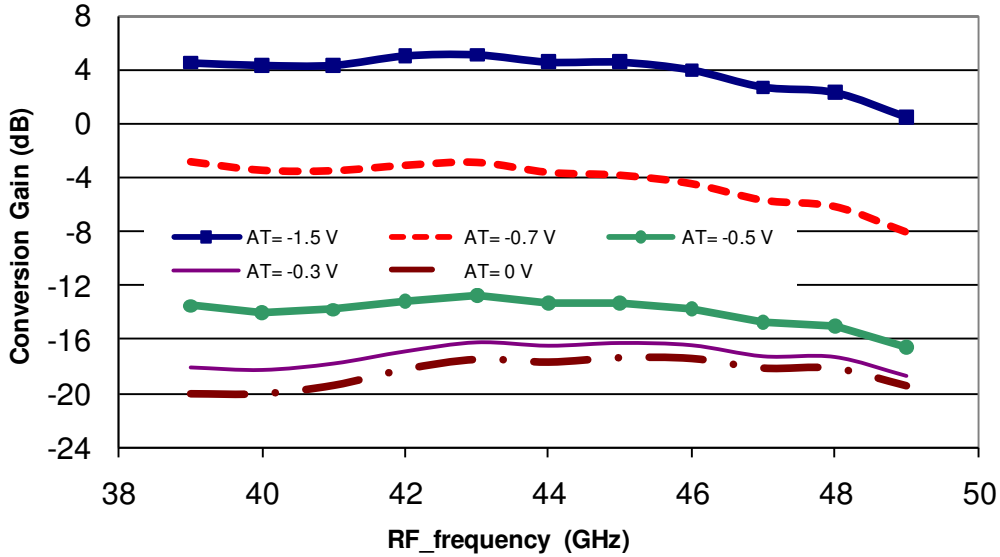
**Conversion Gain versus RF frequency & temperature**  
 RF= 4LO-IF; IF = 2GHz; AT = -1.5V



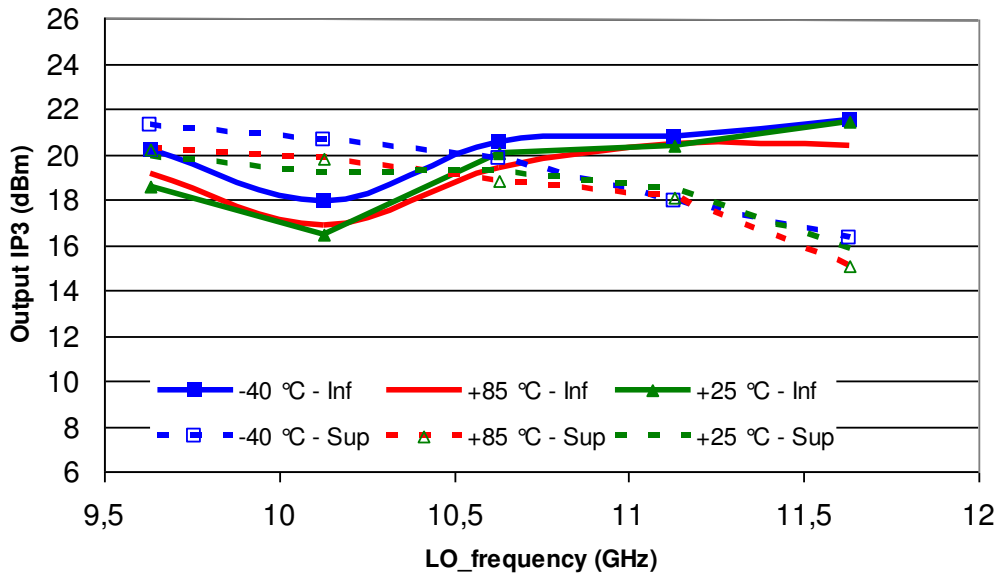
Typical chip on board Measurements in Temperature

DX = DA = 4V, GA = -0.5V, GM = -0.6V, G3 = -0.3V, GX = -1.2V, P\_LO = 1dBm.

Conversion Gain versus RF frequency & attenuation  
 RF = 4LO+IF; IF = 2GHz

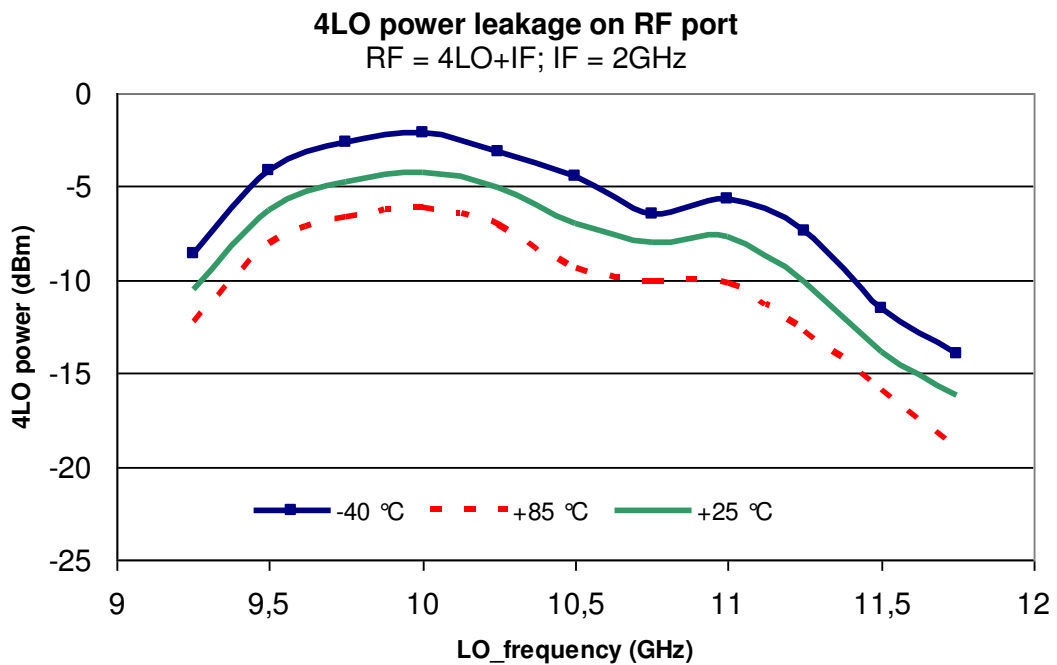
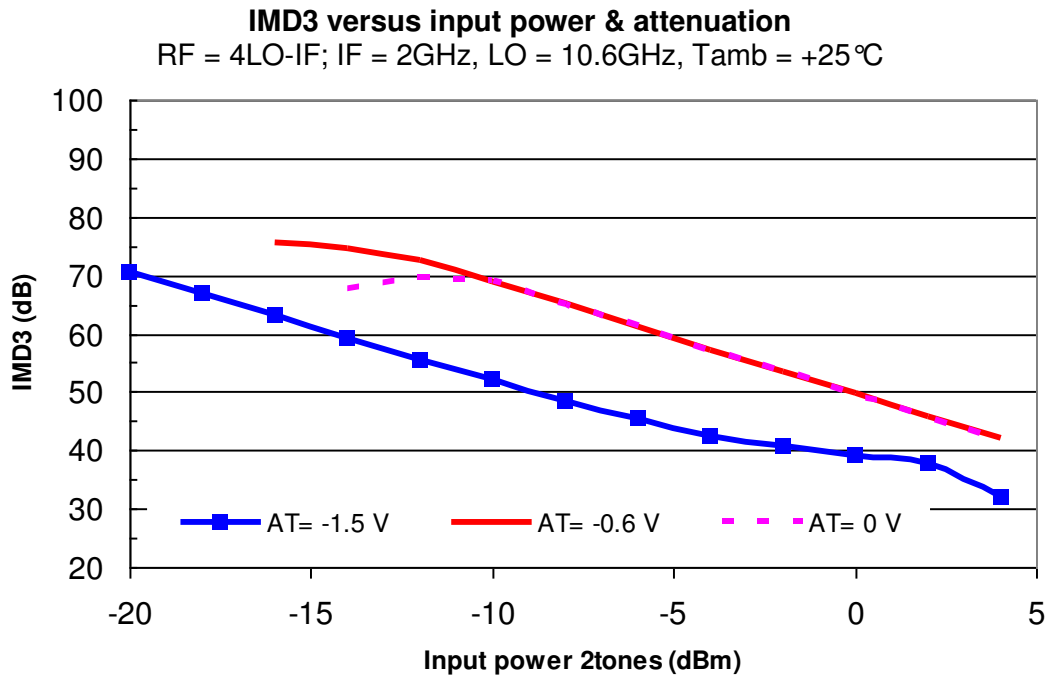


Output IP3 versus LO frequency at max. gain  
 RF = 4LO+/-IF; IF = 2GHz; Pin = -16dBm



**Typical chip on board Measurements in Temperature**

DX = DA = 4V, GA = -0.5V, GM = -0.6V, G3 = -0.3V, GX = -1.2V, P\_LO = 1dBm.

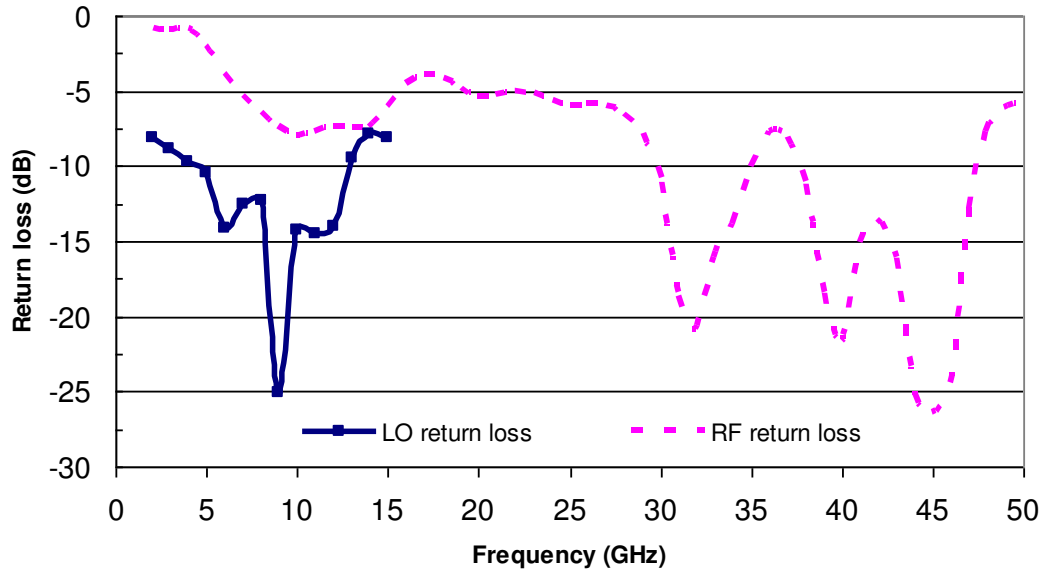


## Typical chip on board Measurements

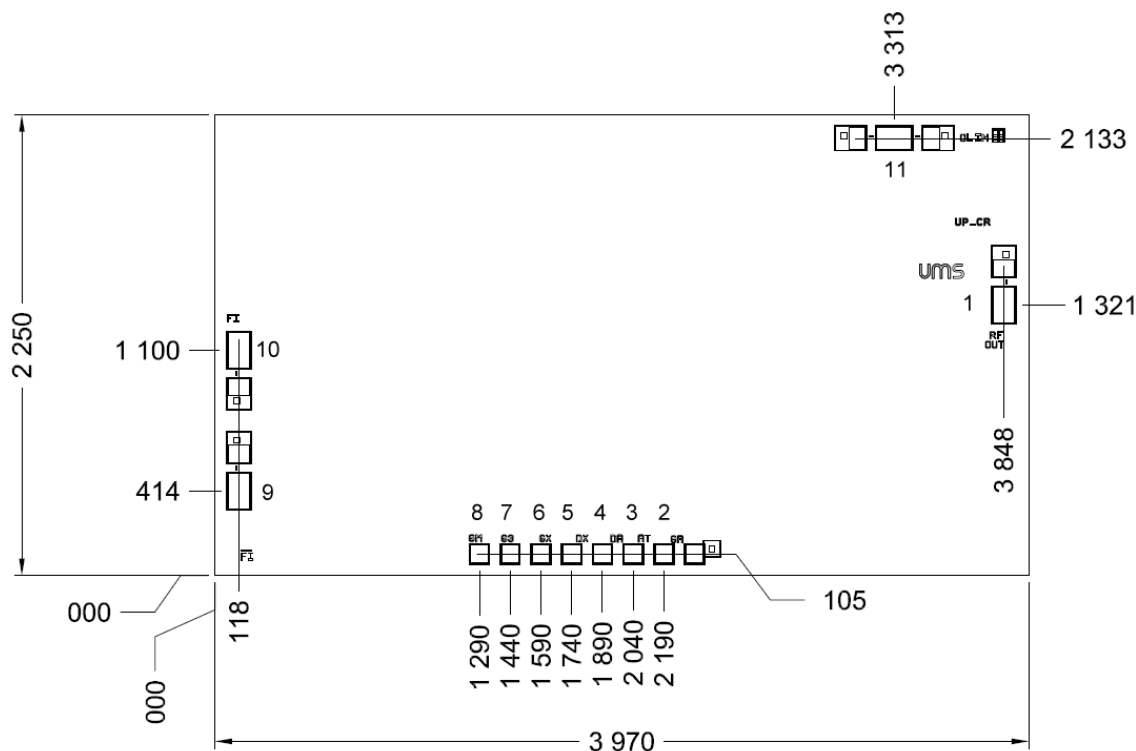
Tamb = +25°C, DX = DA = 4V, GA = -0.5V, GM = -0.6V, G3 = -0.3V, GX = -1.2V,  
P\_LO = 1dBm.

### RF & LO return loss (in the connectors plan)

RF = 4LO-IF; IF = 2GHz, LO = 10.6GHz



## Mechanical data



Chip thickness: 100 μm, units: μm, tol: +/- 35 μm

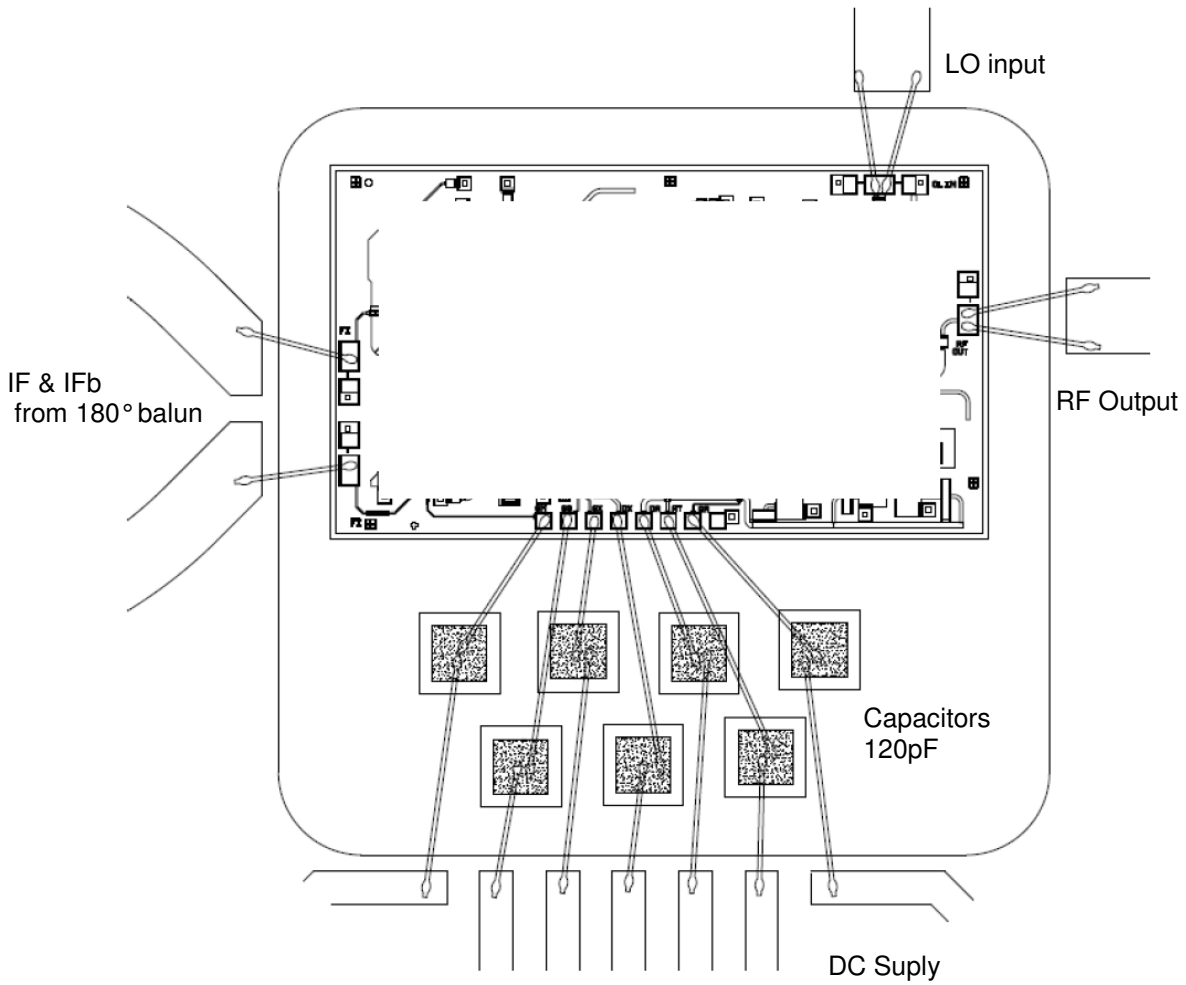
DC pads = 92x92 μm, RF pads = 178x114 μm

Pin number	Pin name	Description
1	RF_OUT	RF output
2	GA	RF buffer gate voltage
3	AT	Attenuation control voltage
4	DA	RF buffer drain voltage
5	DX	Multiplier & LO Buffer drain voltage
6	GX	Multiplier gate voltage
7	G3	Buffer gate voltage
8	GM	Mixer gate voltage
9, 10	IF & IFb	IF inputs
11	LO_IN	LO input

## Recommended biasing

Pin Name	Pin Number	Parameter	Nominal value
GM	8	Mixer Gate voltage	-0.6V
G3	7	Buffer Gate voltage	-0.3V
GX	6	X4 Gate voltage	-1.2V
GA	2	RF amplifier Gate voltage	-0.5V
DX	5	X4 Drain voltage	4V
DA	4	RF amplifier Drain voltage	4V
AT	3	Attenuation control voltage	-1.5V to +0.5V

## Chip assembly



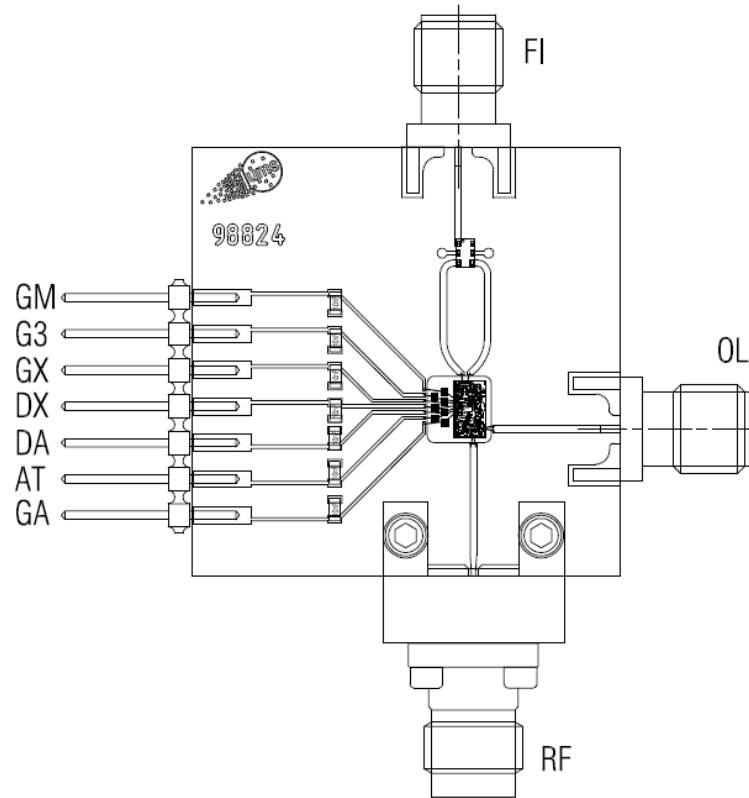
Note: Supply feed should be capacitively bypassed. 25 $\mu$ m diameter gold wire is recommended

**Evaluation mother board**

Based on typically Ro4003 / 8 mils or equivalent.

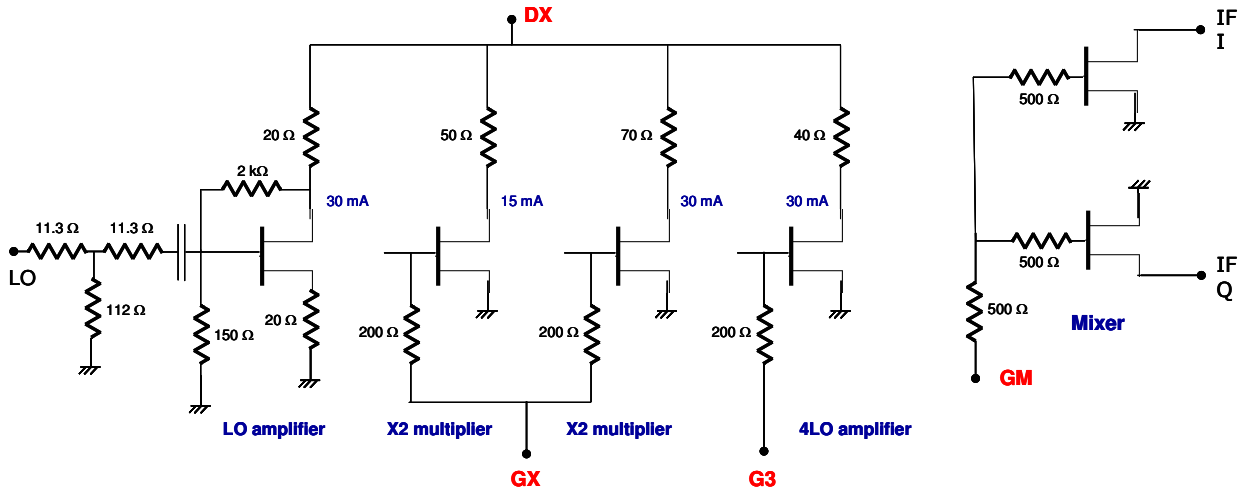
Decoupling capacitors of 10nF  $\pm 10\%$  and chip 120pF  $\pm 10\%$

180° hybrid balun: 2-2.5GHz

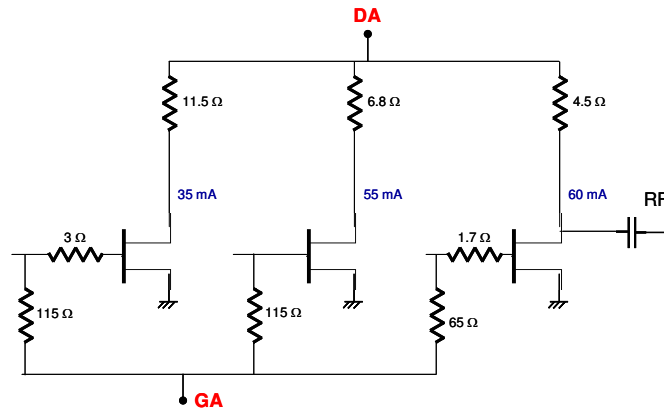


## DC Schematic

LO multiplier and buffers: 4V, 105mA



RF amplifier: 4V, 150mA



**Notes**

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

## Ordering Information

Chip form:

CHU2299-99F/00

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