

DC-4GHz reflective SPDT GaAs Monolithic Microwave IC

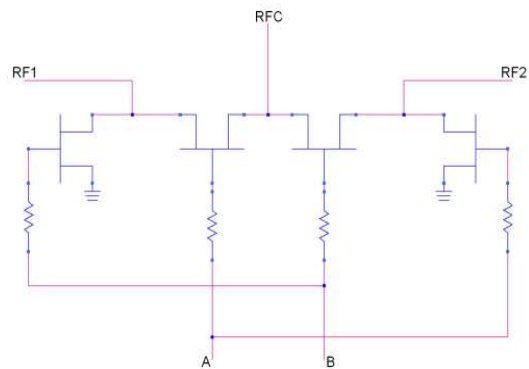
Description

The CHS5104-99F is a monolithic FET based reflective switch.

It is designed for a wide range of applications, from defense to commercial communication systems.

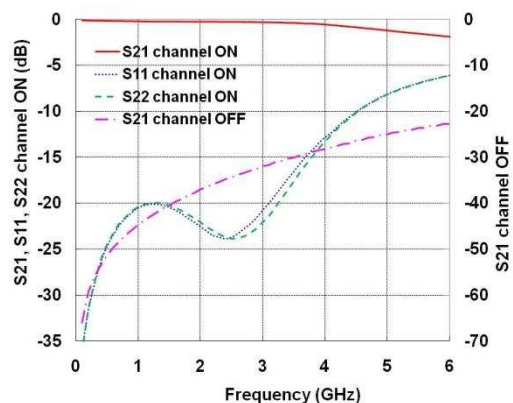
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performance: DC-4GHz
- Low insertion loss: 0.5dB@4GHz
- Isolation: 38dB@2GHz
30dB@4GHz
- Return loss: 20dB@2GHz
13dB@4GHz
- Input P1dB: 30dBm
- Chip size: 0.8x0.8x0.07mm³



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	DC		4	GHz
IL	On state insertion loss		0.5		dB
ISOL	Off state isolation		35		dB
RL	On state return loss		20		dB
IP1dB	Input Power @1dB gain compression		30		dBm

Electrical Characteristics ⁽¹⁾

T_{amb.} = +25°C, specifications are given for 50Ω source and load impedances.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Freq	Frequency range		DC		4	GHz
IL	On state insertion loss ⁽²⁾	DC - 2GHz DC - 4GHz		0.25 0.5		dB
ISOL	Off state isolation	DC - 2GHz DC - 4GHz		38 30		dB
RL	On state input and output return losses	DC - 2GHz DC - 4GHz		20 13		dB
VH	Control voltage high level			0	0.5	
VL	Control voltage low level		-8	-5		V
IP1dB	Input Power @1dB gain compression.	Freq. >0.5GHz VL=-5V/VH=0V VL=-8V/VH=0V		30 33		dBm
Ton / Toff	Switching time	50% control to 90% RF, and 50% control to 10% RF		10		ns
Ic_L	Current consumption on the control supply voltage	VH= 0V VL=-5V VL=-8V		40 20 200		μA

⁽¹⁾ These values are representative of on-board measurements with a typically bonding wire of 1nH at each RF ports.

⁽²⁾ Variation rate of insertion loss with temperature in the range -55°C to +125°C: -0.002dB/°C

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25 °C

Symbol	Parameter	Values	Unit
VH	High level control voltage	0.8	V
VL	Low level control voltage	-10	V
Pin	Maximum peak input power overdrive ⁽²⁾	38	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-55 to +125	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.⁽²⁾ Duration < 1s.**SPDT truth table (complementary logic)**

PAD A	PAD B	Electrical path RFC to RF1	Electrical path RFC to RF2
VH	VL	ON	OFF
VL	VH	OFF	ON

Typical on-wafer Sij parameters

Tamb.= +25°C, Bias Conditions : VL = -5V, VH = 0V, **ON-state** (RFC-RF1 path or RFC-RF2 path)

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.2	-31.10	-105.7	-0.18	-2.0	-0.19	-2.0	-31.06	-105.2
0.4	-25.37	-101.3	-0.20	-3.8	-0.20	-3.8	-25.40	-101.0
0.6	-21.97	-100.9	-0.22	-5.7	-0.22	-5.7	-21.97	-100.5
0.8	-19.55	-102.1	-0.24	-7.6	-0.24	-7.6	-19.51	-101.1
1.0	-17.68	-103.4	-0.27	-9.4	-0.28	-9.4	-17.62	-102.2
1.2	-16.21	-105.0	-0.31	-11.2	-0.32	-11.2	-16.15	-103.7
1.4	-14.82	-106.1	-0.34	-13.1	-0.35	-13.1	-14.81	-104.7
1.6	-13.70	-107.5	-0.38	-15.0	-0.39	-15.0	-13.75	-106.1
1.8	-12.72	-109.3	-0.43	-16.9	-0.44	-16.9	-12.69	-107.4
2.0	-11.86	-111.2	-0.50	-18.6	-0.50	-18.7	-11.84	-109.2
2.2	-11.04	-113.6	-0.56	-20.2	-0.56	-20.2	-10.96	-110.1
2.4	-10.51	-114.9	-0.61	-22.4	-0.62	-22.3	-10.36	-113.1
2.6	-9.83	-116.4	-0.71	-24.0	-0.71	-24.0	-9.78	-114.3
2.8	-9.27	-118.3	-0.79	-25.7	-0.79	-25.7	-9.21	-115.8
3.0	-8.84	-119.9	-0.88	-27.3	-0.88	-27.3	-8.69	-117.4
3.2	-8.30	-120.8	-0.95	-29.0	-0.96	-29.0	-8.22	-119.0
3.4	-7.80	-122.7	-1.04	-30.6	-1.04	-30.6	-7.78	-120.6
3.6	-7.37	-125.0	-1.14	-32.2	-1.14	-32.2	-7.38	-121.9
3.8	-6.99	-126.7	-1.24	-33.8	-1.24	-33.8	-7.01	-123.4
4.0	-6.67	-128.2	-1.33	-35.3	-1.33	-35.3	-6.67	-125.0
4.2	-6.33	-129.7	-1.41	-36.9	-1.42	-36.9	-6.30	-126.0
4.4	-6.06	-131.2	-1.52	-38.5	-1.52	-38.5	-5.97	-127.7
4.6	-5.74	-132.4	-1.63	-40.0	-1.62	-40.0	-5.72	-129.0
4.8	-5.47	-134.0	-1.74	-41.5	-1.74	-41.5	-5.43	-130.5
5.0	-5.22	-135.7	-1.86	-42.9	-1.86	-42.9	-5.18	-131.9
5.2	-4.98	-137.1	-1.98	-44.2	-1.98	-44.3	-4.96	-133.2
5.4	-4.75	-138.6	-2.09	-45.7	-2.09	-45.6	-4.74	-134.4
5.6	-4.56	-140.0	-2.21	-47.0	-2.21	-47.0	-4.52	-135.8
5.8	-4.30	-141.8	-2.36	-48.7	-2.37	-48.7	-4.29	-137.4
6.0	-4.11	-143.4	-2.50	-50.0	-2.50	-50.0	-4.12	-138.6
6.2	-3.96	-144.9	-2.61	-51.3	-2.62	-51.3	-3.90	-139.5
6.4	-3.81	-146.2	-2.75	-52.7	-2.75	-52.7	-3.73	-141.2
6.6	-3.62	-147.7	-2.90	-53.9	-2.90	-53.9	-3.64	-142.3
6.8	-3.48	-149.2	-3.03	-55.0	-3.03	-55.0	-3.51	-143.2
7.0	-3.36	-150.6	-3.14	-56.1	-3.14	-56.1	-3.31	-144.0
7.2	-3.25	-151.8	-3.24	-57.2	-3.24	-57.2	-3.08	-145.2
7.4	-3.16	-153.0	-3.32	-58.6	-3.33	-58.6	-2.84	-146.8
7.6	-3.05	-154.1	-3.47	-60.1	-3.48	-60.1	-2.76	-148.5
7.8	-2.93	-155.2	-3.63	-61.4	-3.64	-61.3	-2.70	-149.7
8.0	-2.79	-156.4	-3.84	-62.6	-3.84	-62.6	-2.70	-150.9

Typical on-wafer Sij parameters

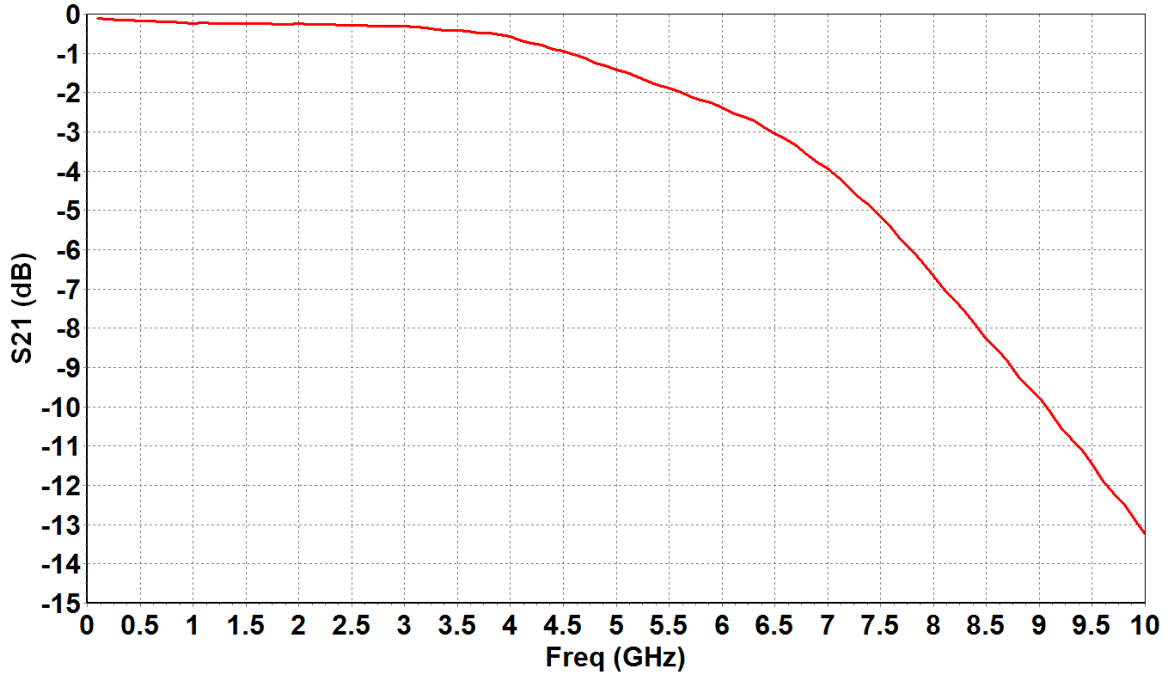
Tamb.= +25 °C, Bias Conditions : VL = -5V, VH = 0V, **OFF-state** (RFC-RF1 path or RFC-RF2 path)

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.2	-30.73	100.9	-64.80	106.1	-64.19	106.1	-0.43	179.2
0.4	-30.14	-92.1	-54.91	99.1	-54.97	99.7	-0.44	178.8
0.6	-22.46	-96.0	-52.98	102.6	-53.03	103.3	-0.45	178.4
0.8	-19.43	-103.5	-50.24	104.5	-50.29	105.0	-0.45	177.9
1.0	-17.33	-107.1	-48.14	107.7	-48.13	108.1	-0.46	177.4
1.2	-16.19	-111.2	-46.26	110.0	-46.21	109.9	-0.46	176.9
1.4	-15.12	-113.1	-44.41	109.5	-44.42	109.4	-0.47	176.4
1.6	-14.10	-117.4	-43.16	110.2	-43.19	110.4	-0.48	175.9
1.8	-13.98	-119.5	-41.95	114.5	-41.95	114.3	-0.47	175.5
2.0	-13.77	-117.1	-40.51	115.3	-40.52	115.3	-0.47	175.0
2.2	-12.85	-115.3	-40.03	118.2	-40.04	118.1	-0.43	175.3
2.4	-11.97	-113.6	-38.27	118.0	-38.25	118.1	-0.42	173.5
2.6	-11.31	-116.5	-37.16	118.6	-37.14	118.6	-0.49	173.3
2.8	-10.70	-116.0	-36.12	118.8	-36.12	118.7	-0.49	172.8
3.0	-9.79	-115.2	-34.96	119.9	-34.99	119.9	-0.53	172.3
3.2	-9.13	-118.1	-33.68	116.7	-33.70	116.8	-0.54	172.1
3.4	-8.40	-119.8	-32.97	114.4	-33.00	114.5	-0.50	171.7
3.6	-7.48	-121.1	-32.56	112.2	-32.55	112.3	-0.48	171.2
3.8	-7.16	-124.3	-31.96	114.5	-31.96	114.5	-0.51	170.7
4.0	-6.50	-128.4	-31.25	112.2	-31.25	112.1	-0.51	170.1
4.2	-6.61	-131.8	-30.79	113.1	-30.79	113.0	-0.51	169.7
4.4	-6.58	-133.9	-30.10	114.0	-30.08	114.0	-0.51	168.9
4.6	-6.52	-133.8	-29.37	113.0	-29.37	113.0	-0.54	168.6
4.8	-6.45	-133.8	-28.69	113.5	-28.68	113.5	-0.54	168.0
5.0	-5.99	-133.8	-27.96	111.8	-27.96	111.9	-0.55	167.5
5.2	-5.83	-133.9	-27.30	111.4	-27.30	111.4	-0.56	167.1
5.4	-5.25	-133.8	-26.64	109.2	-26.62	109.2	-0.57	166.6
5.6	-4.82	-135.6	-26.15	107.5	-26.15	107.6	-0.56	166.0
5.8	-4.59	-137.3	-25.72	106.5	-25.71	106.5	-0.58	165.5
6.0	-4.47	-139.5	-25.31	106.1	-25.31	106.0	-0.58	165.0
6.2	-4.13	-139.8	-24.72	104.6	-24.73	104.6	-0.58	164.6
6.4	-3.79	-142.2	-24.32	102.5	-24.33	102.4	-0.58	163.9
6.6	-3.42	-143.8	-23.93	100.4	-23.93	100.4	-0.62	163.4
6.8	-3.53	-146.2	-23.66	100.6	-23.64	100.6	-0.63	163.0
7.0	-3.29	-148.5	-23.38	99.2	-23.38	99.2	-0.59	162.8
7.2	-3.39	-151.1	-23.18	99.6	-23.17	99.7	-0.53	162.2
7.4	-3.36	-150.2	-22.48	98.9	-22.48	98.8	-0.44	161.3
7.6	-3.33	-151.7	-22.15	98.5	-22.15	98.5	-0.52	160.0
7.8	-3.06	-153.3	-21.81	95.9	-21.80	95.9	-0.61	159.4
8.0	-2.91	-153.4	-21.50	94.1	-21.51	94.1	-0.73	159.1

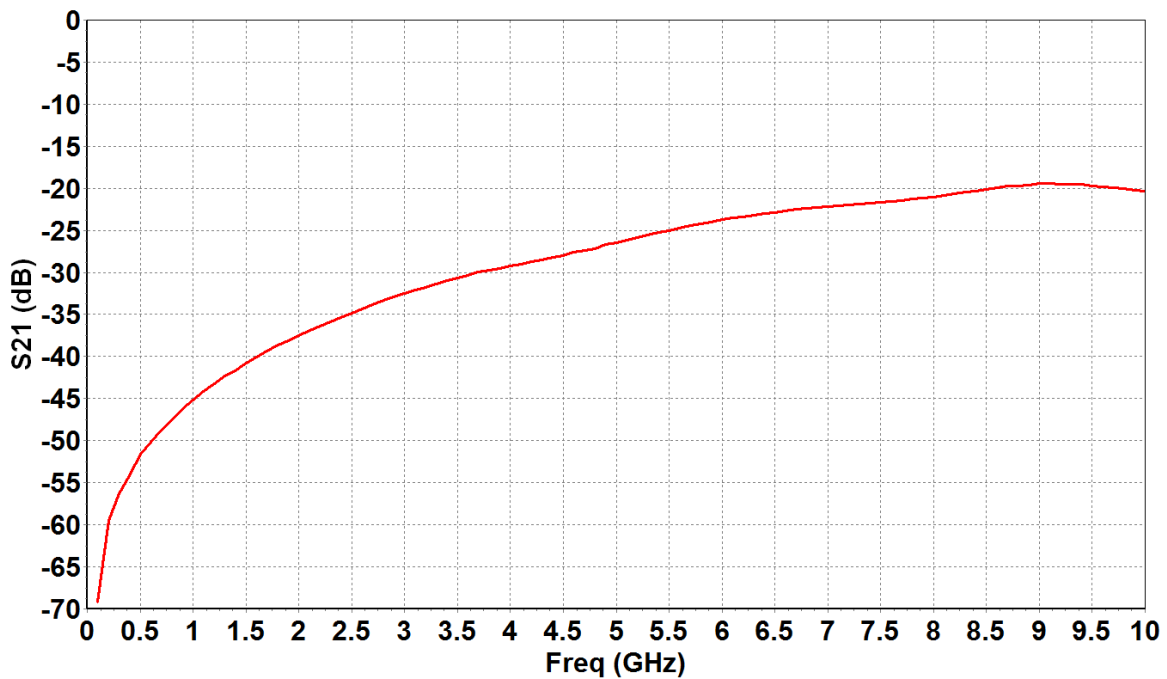
Typical Test Fixture Measurements

Tamb.= +25°C, VL=-5V, VH=0V

ON state: S21 versus Frequency



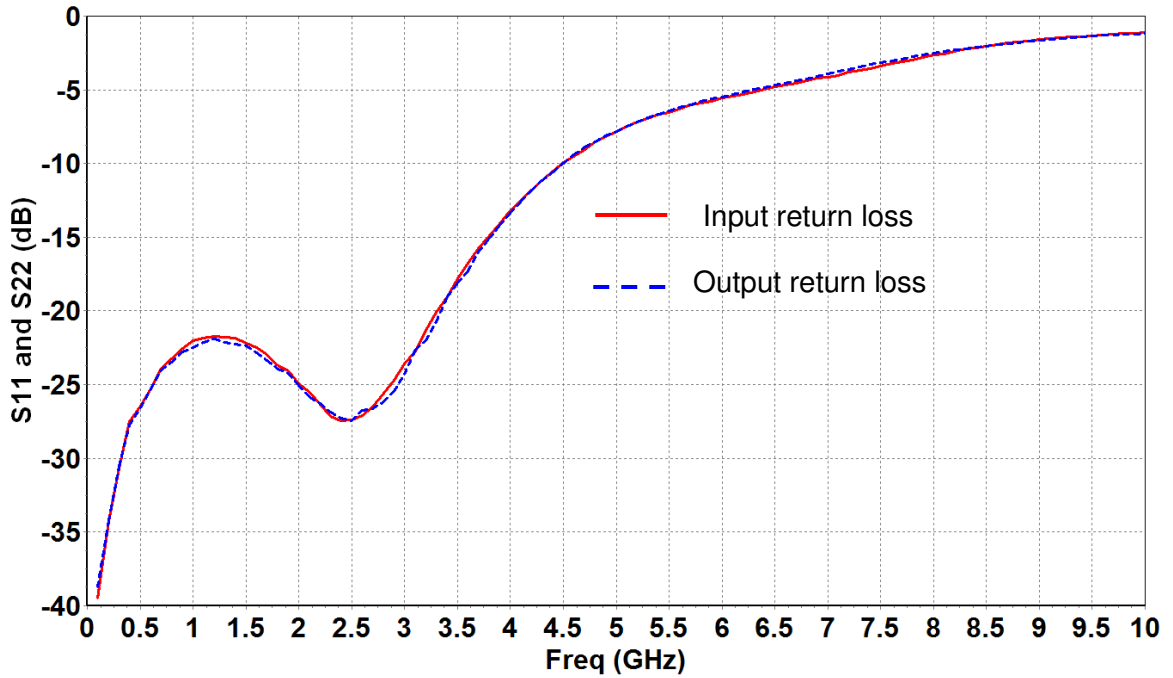
OFF state: S21 versus Frequency



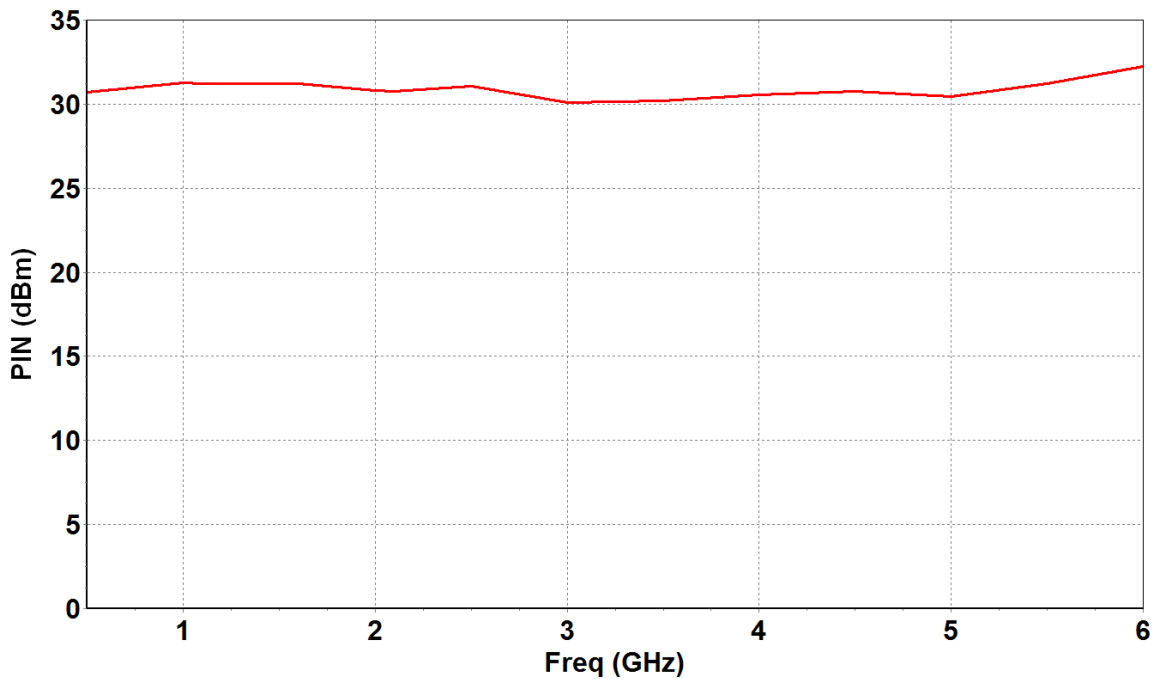
Typical Test Fixture Measurements

Tamb.= +25°C, VL=-5V, VH=0V

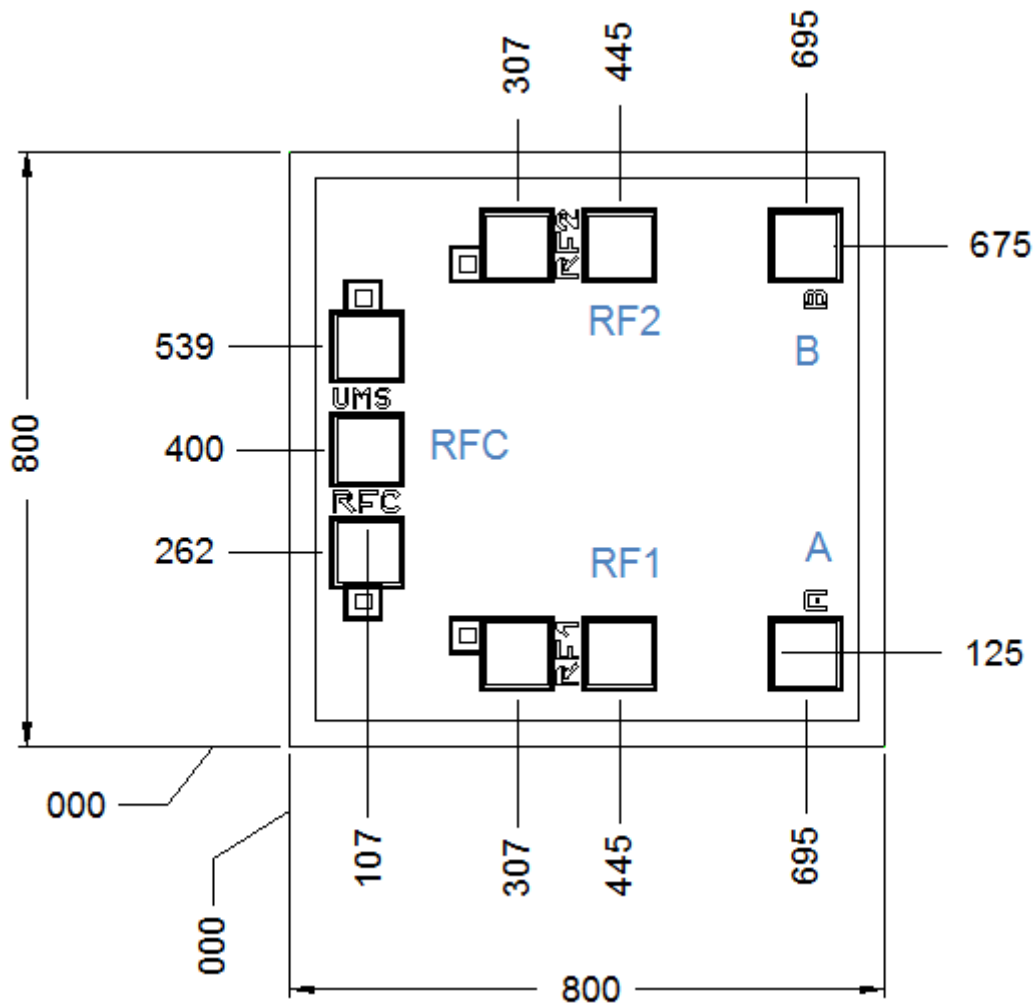
ON state: Input and output return loss versus Frequency



ON state: Input power at 1dB gain compression (VL=-5V / VH=0V)

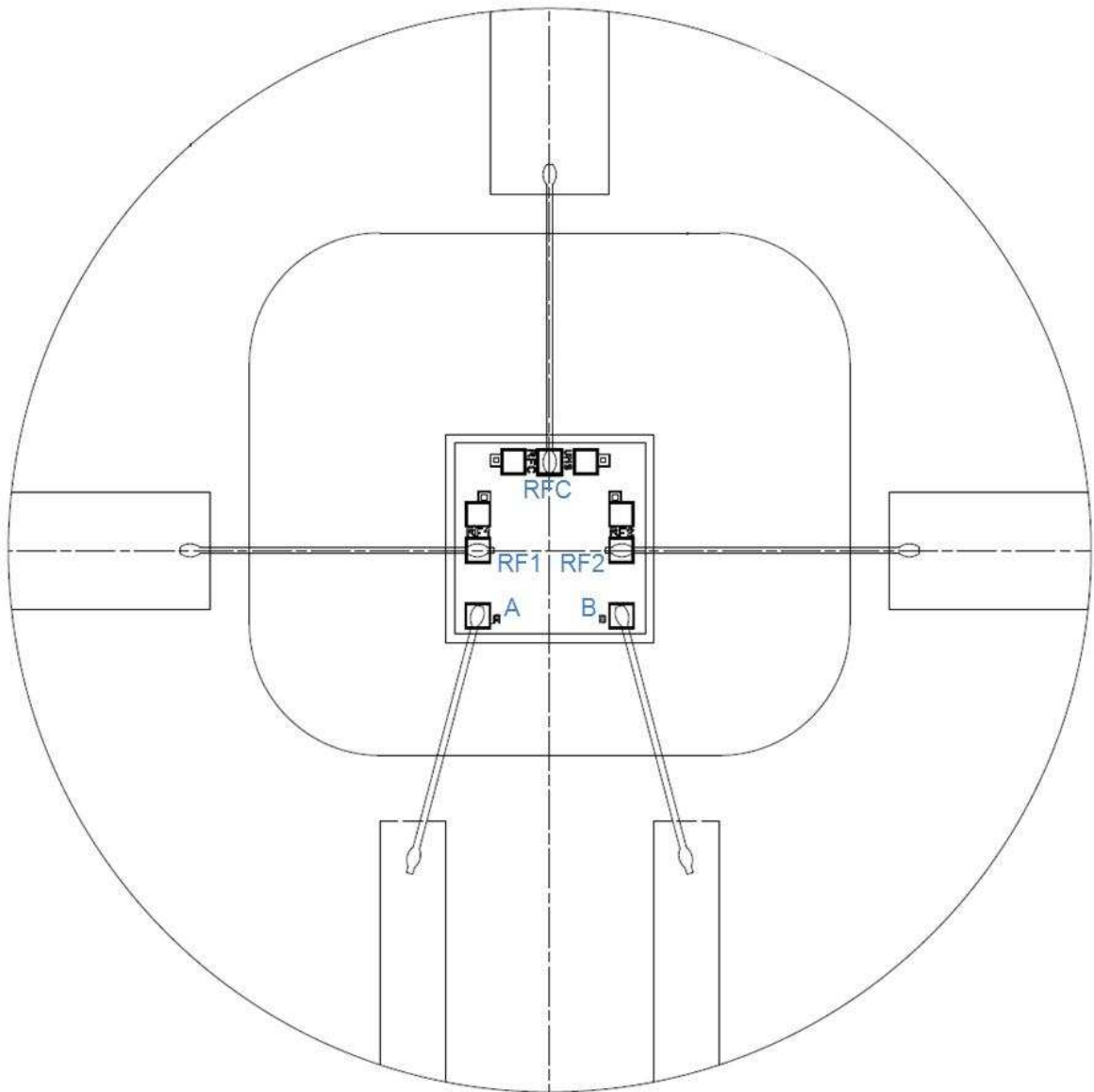


Mechanical data



Chip thickness: 70µm.
 Chip size: 800x800 ±35µm
 All dimensions are in micrometers

Recommended assembly plan



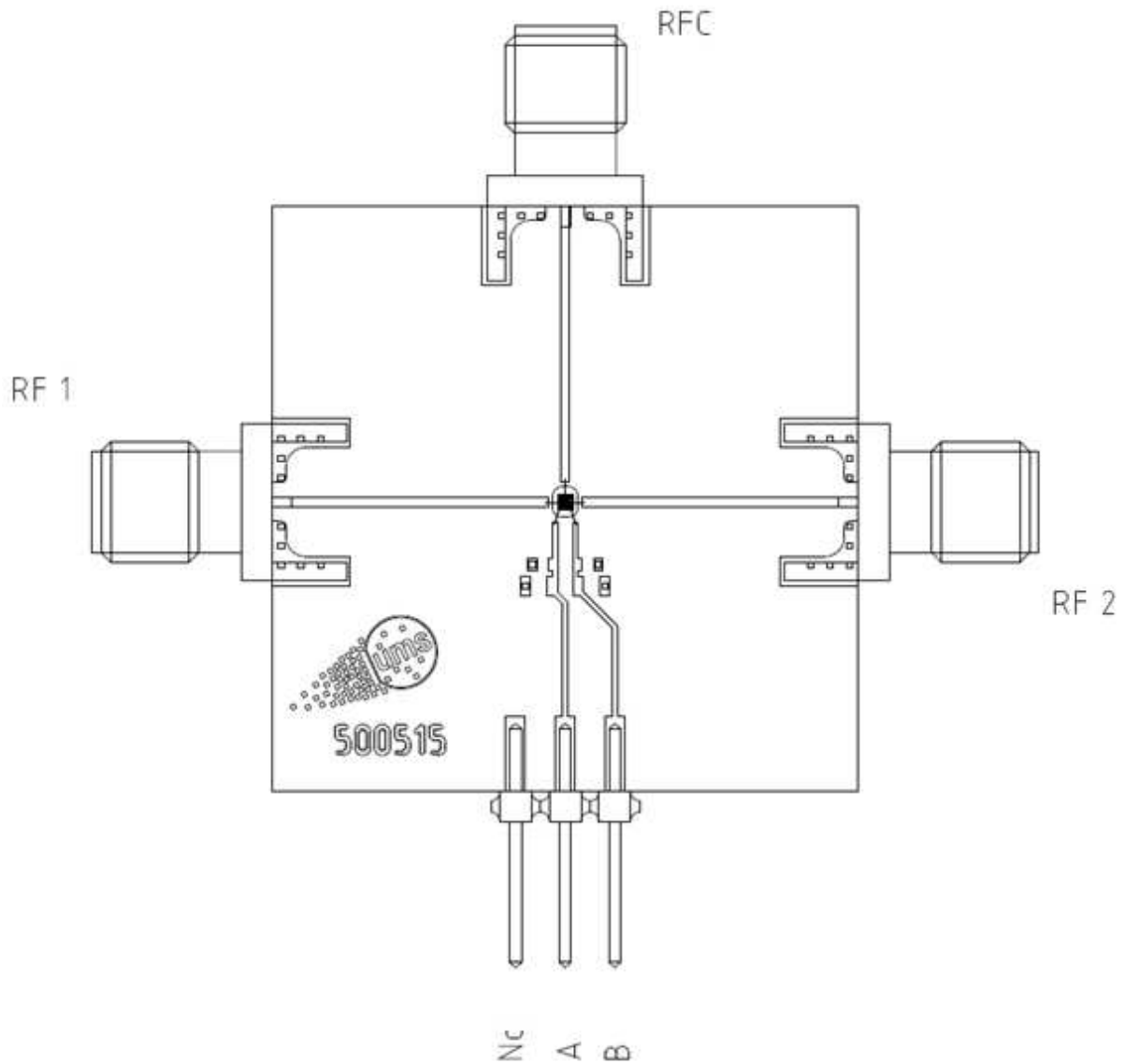
Recommended RF bonding wires: length=1.1mm / \varnothing 25 μ m

Recommended circuit bonding table

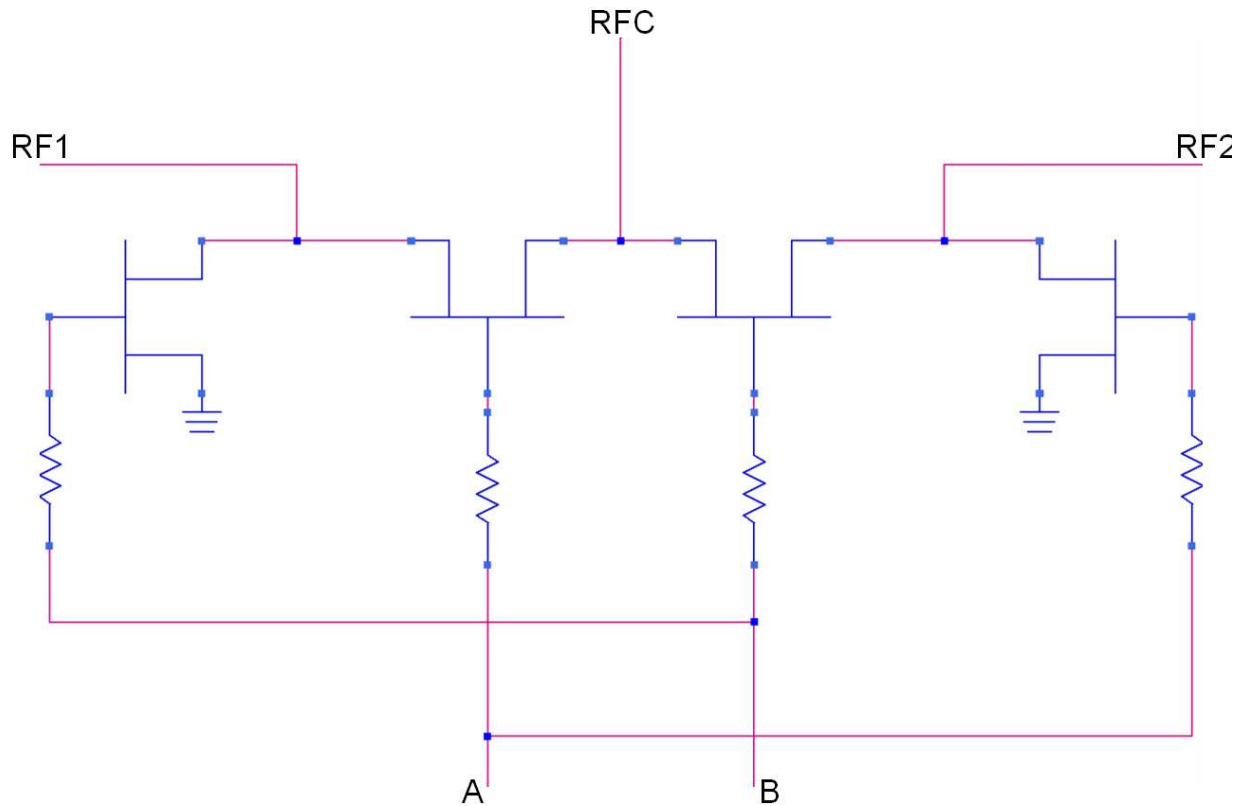
Label	Type	Decoupling	Comment
A, B	Control voltage	Not required	SPDT switch pad control
RFC, RF1, RF2	RF access	External DC block must be used to ensure DC decoupling	The MMIC is DC coupled

Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- No decoupling capacitor used on control access



DC Schematic



Note: to ensure DC decoupling on RF accesses, DC block must be added outside the MMIC

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Ordering Information

Chip form:

CHS5104-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**