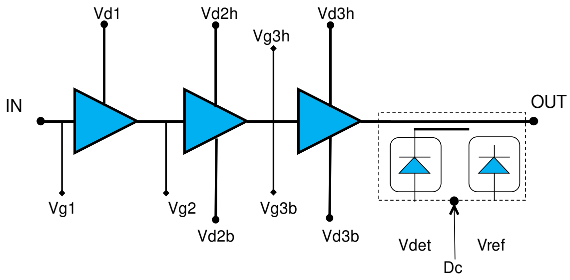
71-76GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

Description

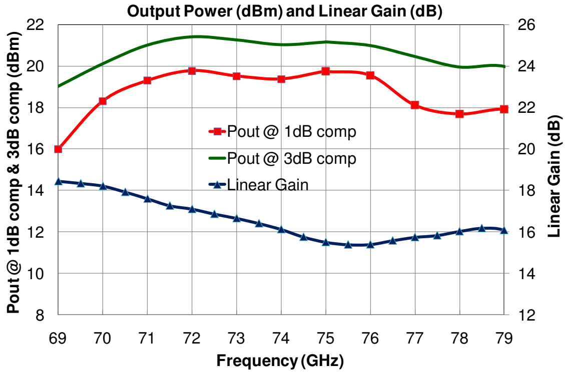
The CHA3080-98F is a three-stage monolithic Medium Power Amplifier. This circuit includes a power detector which integrates a directional coupler, a detection diode and a reference diode to be used in differential mode.
It is dedicated to E-band telecommunication, particularly well suited for the new generation of high capacity Backhaul.
The circuit is manufactured with a pHEMT process, 0.1µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form with BCB layer protection.



Functional diagram

Main Features

- ■ Broadband performances: 71-76GHz
- ■ 16dB linear gain
- ■ 19dBm power at 1dB compression
- ■ 20dB power detector dynamic range
- ■ BCB layer protection
- ■ DC bias: Vd=3.5V@Id=280mA
- ■ Chip size 3.96x1.78x0.07mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	71		76	GHz
Gain	Linear Gain		16		dB
P1dB	Output Power @1dB comp.		19		dBm
Psat	Saturated Output Power		21		dBm
Dr	Detection dynamic range (for output power detection up to Psat)		20		dB

Electrical Characteristics

Tamb.= +25℃, Vd = Dc = 3.5V, Id (quiescent) = 280mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	71		76	GHz
Gain	Linear Gain		16		dB
P1dB	Output power @ 1dB compression		19		dBm
Psat	Saturated Output Power		21		dBm
Dr	Detection dynamic range (for output power detection up to Psat)		20		dB
Vdetect	Voltage detection Vref-Vdet up to Psat		50 to 1400		mV
RLin	Input Return Loss		12		dB
RLout	Output Return Loss		12		dB
Gain ctrl	Gain control range with Vg1&Vg2 tuning (with Vd fixed at 3.5V)		10		dB
NF	Noise Figure		4.0		dB
Vd1, Vd2h, Vd3h, Vd2b, Vd3b	Drain supply voltage		3.5		V
Id	Supply quiescent current		280		mA
Vg1, Vg2, Vg3b, Vg3h	Gate supply voltage		0.15		V
Dc	Detector supply voltage		3.5		V
IDc	Detector bias current		240		µA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports but with 10kΩ resistor in parallel on pads Vdet and Vref.
A ribbon (75µm wide) connection at the input and the output of the MMIC amplifier (See chapter recommended chip assembly) should improve the performances.

Absolute Maximum Ratings (1)

Tamb.= +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4V	V
Id	Drain bias current	350	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum continuous input power	+12	dBm
Tj	Junction temperature	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +150	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.

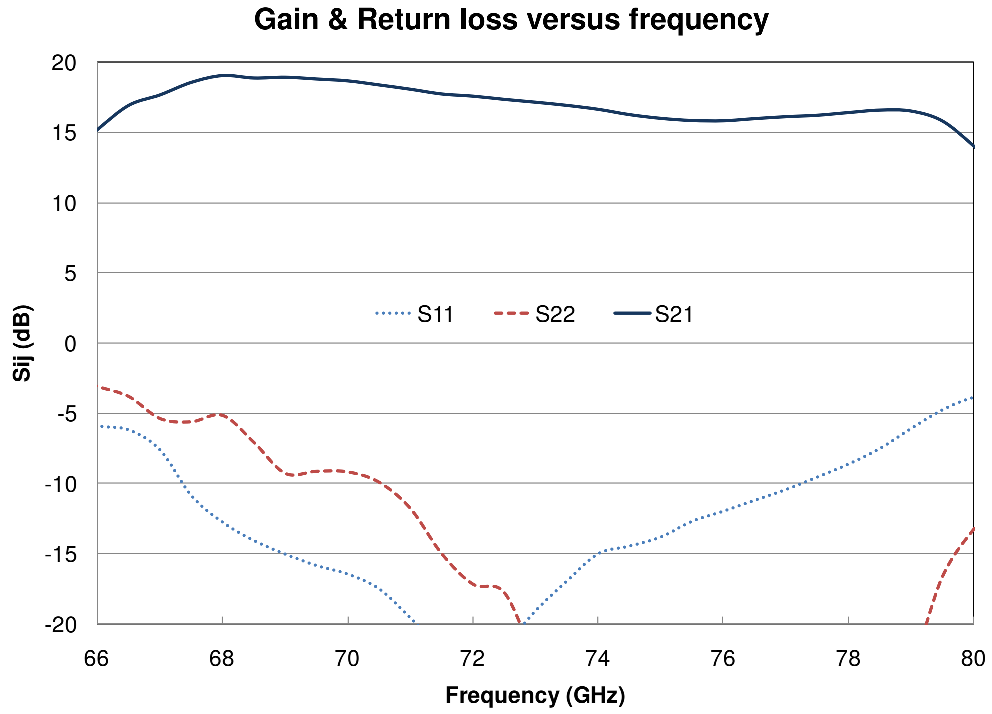
Typical on-wafer Sij parameters

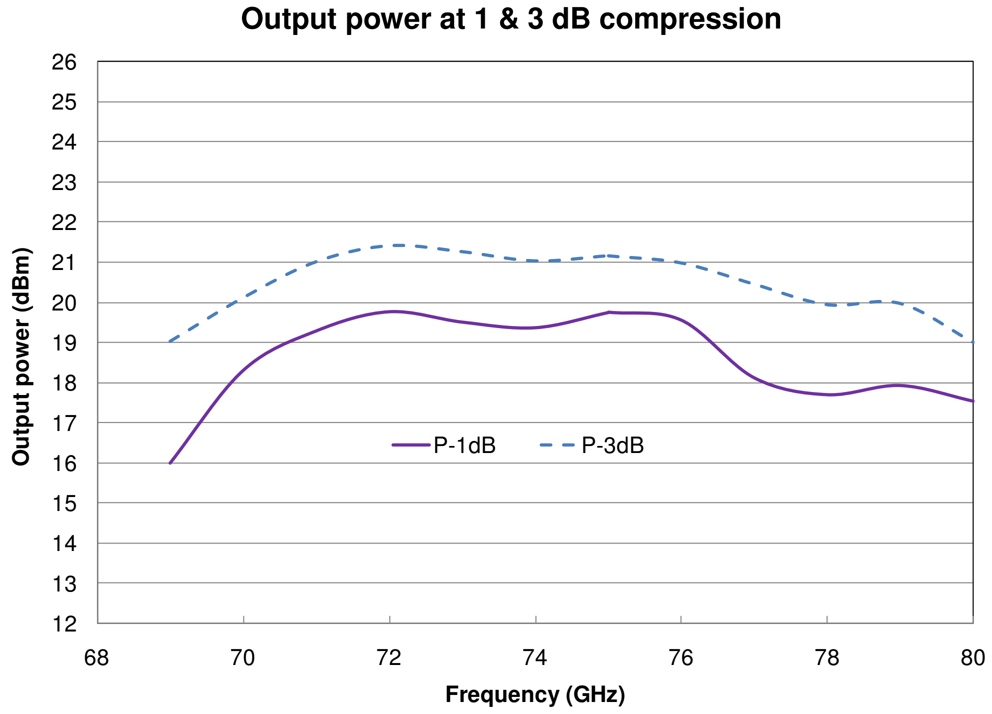
Tamb.= +25°C, Vd = Dc = 3.5V, Id (quiescent) = 280mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
55	-2.46	132.0	-18.06	88.2	-38.27	-59.1	-3.1	154.1
56	-2.15	130.4	-14.57	64.0	-46.79	-110.3	-3.86	136.3
57	-2.08	124.3	-10.74	45.9	-47	-90.7	-5.15	120.0
58	-2.11	117.7	-6.58	16.0	-56.14	173.2	-8.11	96.1
59	-2.24	109.3	-3.93	-17.5	-48.75	-83.7	-13.05	55.6
60	-2.46	100.8	-1.3	-49.8	-44.01	179.0	-18.18	-34.7
61	-2.70	93.3	1.51	-84.4	-47.31	-144.5	-12.31	-109.5
62	-2.97	80.9	3.03	-112.9	-48.68	-148.7	-8.32	-135.7
63	-3.10	59.9	5.28	-144.3	-44.74	147.4	-6.44	-155.0
64	-4.00	37.4	7.81	-176.8	-58.68	41.4	-5.04	-175.9
65	-4.79	13.9	11.13	151.2	-46.69	-106.8	-4.4	168.1
66	-5.95	-3.8	14.36	111.5	-43.75	-70.0	-2.98	154.8
67	-7.25	-50.7	16.74	61.9	-39.35	-109.3	-5.84	114.3
68	-12.65	-125.9	18.02	5.0	-37.08	-155.6	-5.06	95.4
69	-15.54	167.5	17.96	-44.2	-36.92	165.9	-9.55	81.9
70	-18.12	116.8	17.84	-89.5	-37.08	130.1	-8.88	53.1
71	-21.43	105.4	17.31	-132.3	-37.51	95.1	-11.49	30.3
72	-23.63	138.6	16.86	-172.1	-38.17	56.3	-16.38	-29.7
73	-18.57	150.3	16.32	145.1	-39.03	15.9	-20.6	-72.6
74	-14.93	142.7	15.79	104.0	-39.58	-22.7	-25.62	-167.6
75	-14.01	124.4	15.19	66.1	-40.28	-58.2	-24.88	140.9
76	-11.98	115.7	15.05	29.2	-39.71	-96.2	-25.01	38.3
77	-10.37	102.9	15.43	-12.2	-39.19	-135.3	-24.05	21.1
78	-8.42	88.3	15.76	-59.2	-38.74	-176.8	-23.41	-22.1
79	-5.87	68.3	15.85	-114.1	-38.67	135.9	-24.16	37.4
80	-4.00	36.6	13.32	-178.6	-40.65	81.3	-13.51	21.1
81	-4.09	0.4	8.78	127.1	-45.06	31.7	-9.22	-24.3
82	-5.32	-27.5	3.04	83.7	-50.27	-31.9	-7.24	-49.4
83	-6.17	-53.8	-1.89	53.5	-52.02	-136.3	-6.7	-73.0
84	-7.18	-76.6	-6.21	26.8	-51.33	149.9	-6.31	-91.1
85	-8.67	-97.1	-10.46	5.8	-52.71	100.1	-6.34	-105.9
86	-9.94	-116.1	-13.65	-12.5	-52.42	90.9	-6.78	-115.8
87	-11.29	-131.7	-15.77	-35.6	-50.5	36.0	-6.32	-126.7
88	-12.33	-148.4	-18.17	-56.9	-48.64	-30.4	-6.31	-138.3
89	-13.22	-162.5	-19.99	-81.0	-49.99	-117.4	-6.47	-150.8
90	-13.92	-175.1	-21.67	-109.9	-49.76	179.0	-6.82	-164.2
91	-14.52	169.6	-23.45	-140.9	-48.91	148.2	-7.47	-178.6
92	-15.11	154.1	-25.76	-174.2	-48.04	113.4	-8.69	163.1
93	-14.60	141.8	-28.46	151.7	-47.25	86.4	-10.51	136.2
94	-13.52	125.1	-30.15	119.1	-43.54	74.3	-14.36	83.5
95	-12.99	102.5	-30.87	49.4	-36.3	6.8	-14.84	-18.6

Typical on wafer Measurements

Tamb.= +25°C, Vd = Dc = 3.5V, Id (quiescent) = 280mA

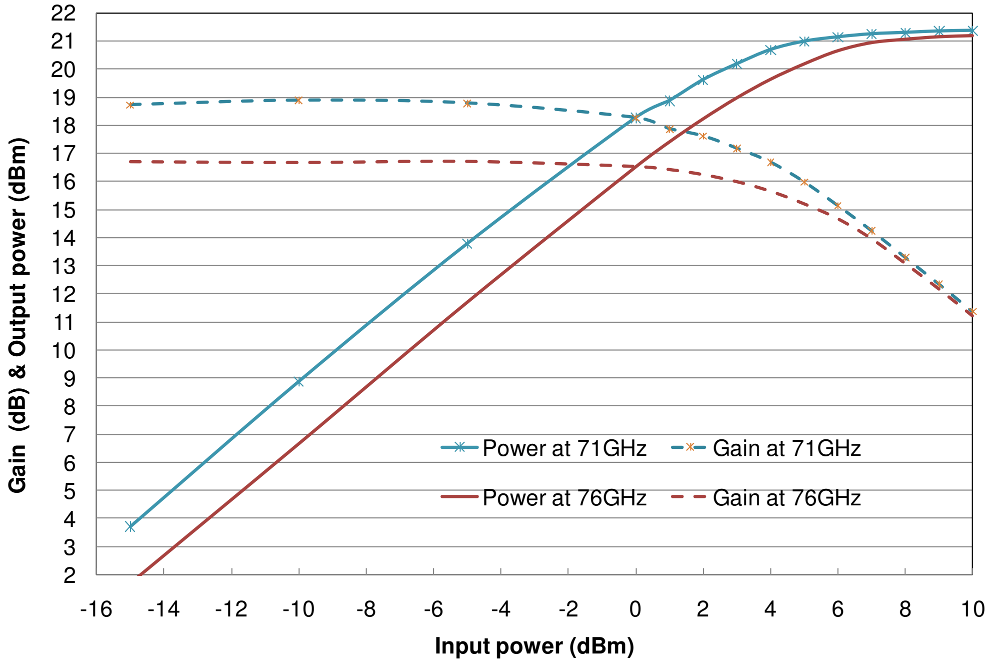




Typical on wafer Measurements

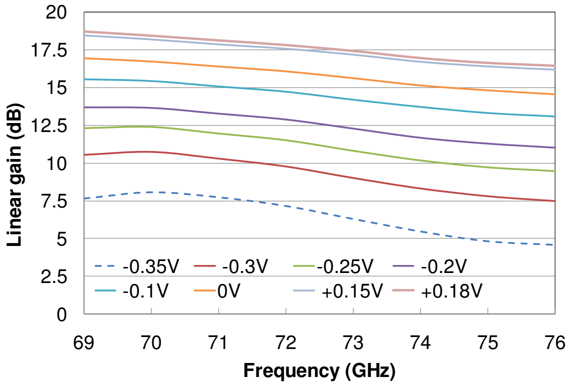
Tamb.= +25°C, Vd = Dc = 3.5V, Id (quiescent) = 280mA

Gain & output power versus input power



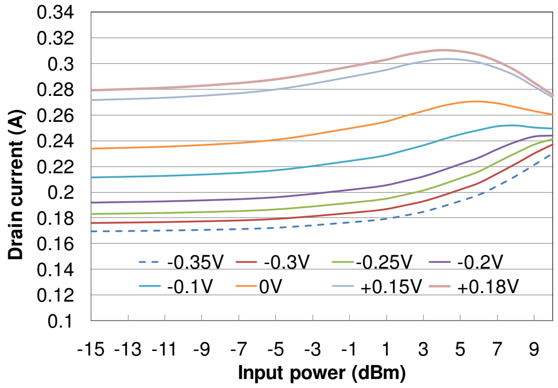
Linear Gain versus gate voltage

Vg3 fixed at +0.18V, Vg1=Vg2 variable



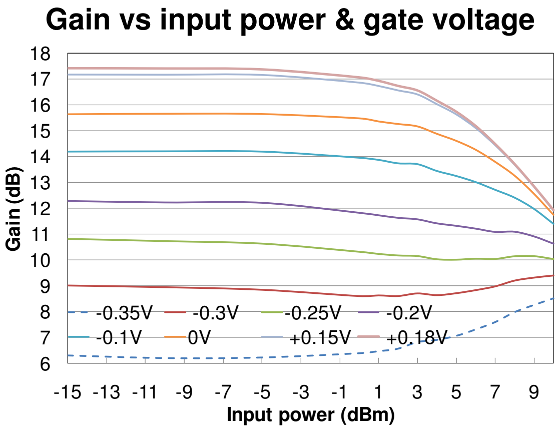
Drain current versus gate voltage & Pin

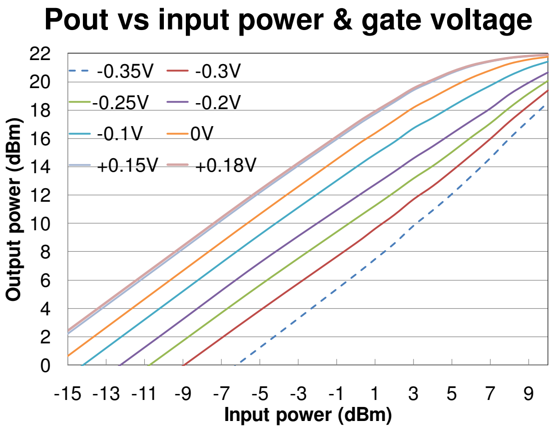
Vg3 fixed at +0.18V, Vg1=Vg2 variable

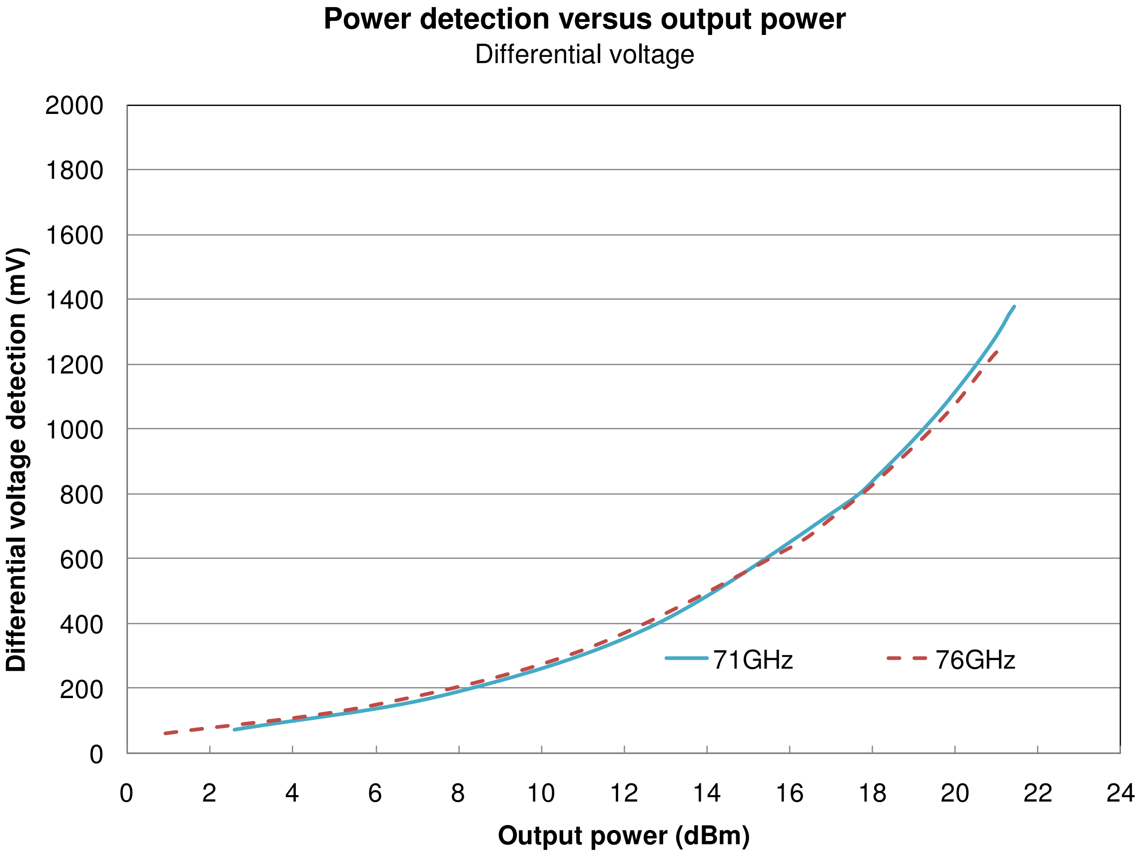


Typical on wafer Measurements

Tamb.= +25°C, Vd = Dc = 3.5V, Id (quiescent) = 280mA



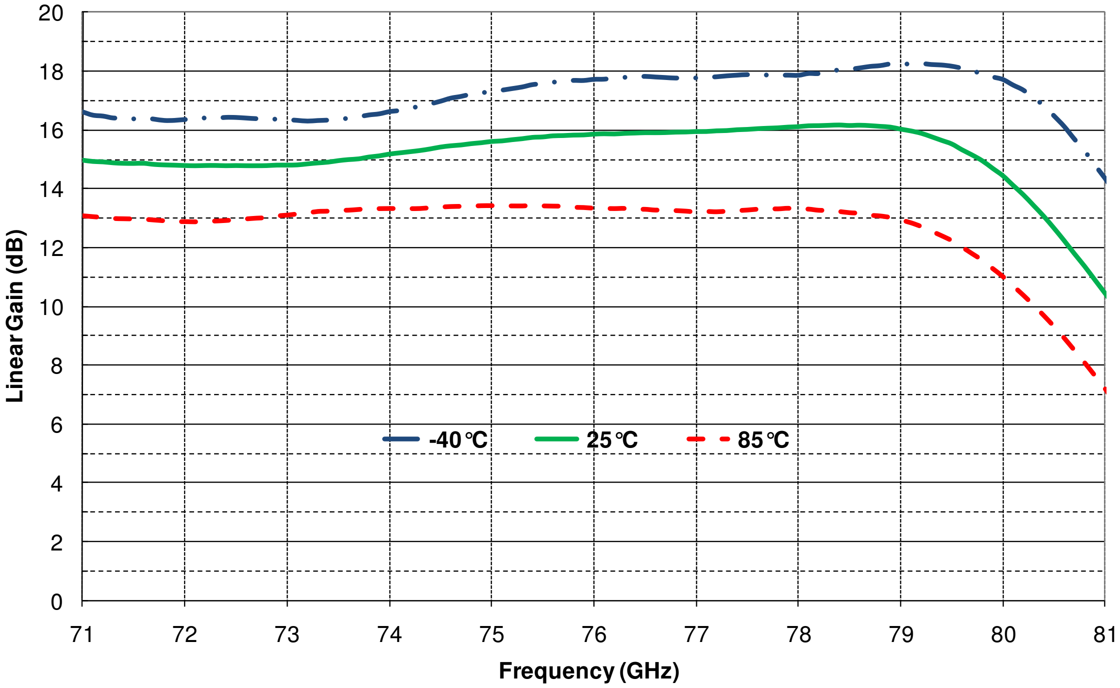




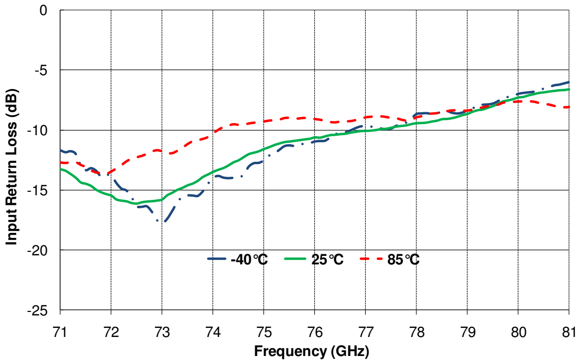
Typical Test Fixture Measurements

Tamb.= -40°C / +25°C / +85°C, Vd = +3.5V, Vg = +0.15V
Id= 340 mA @ -40°C / 280 mA @ +25°C / 250mA @ +85°C
Measurements are given in the test fixture access plans

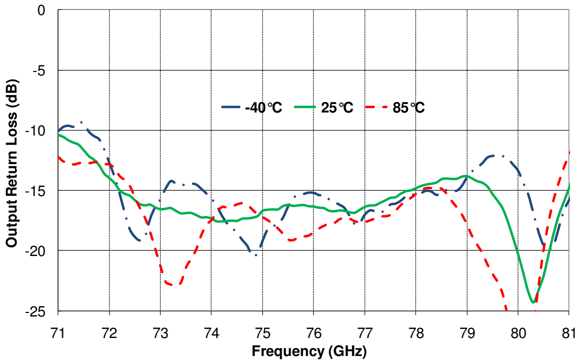
Linear Gain versus Temperature



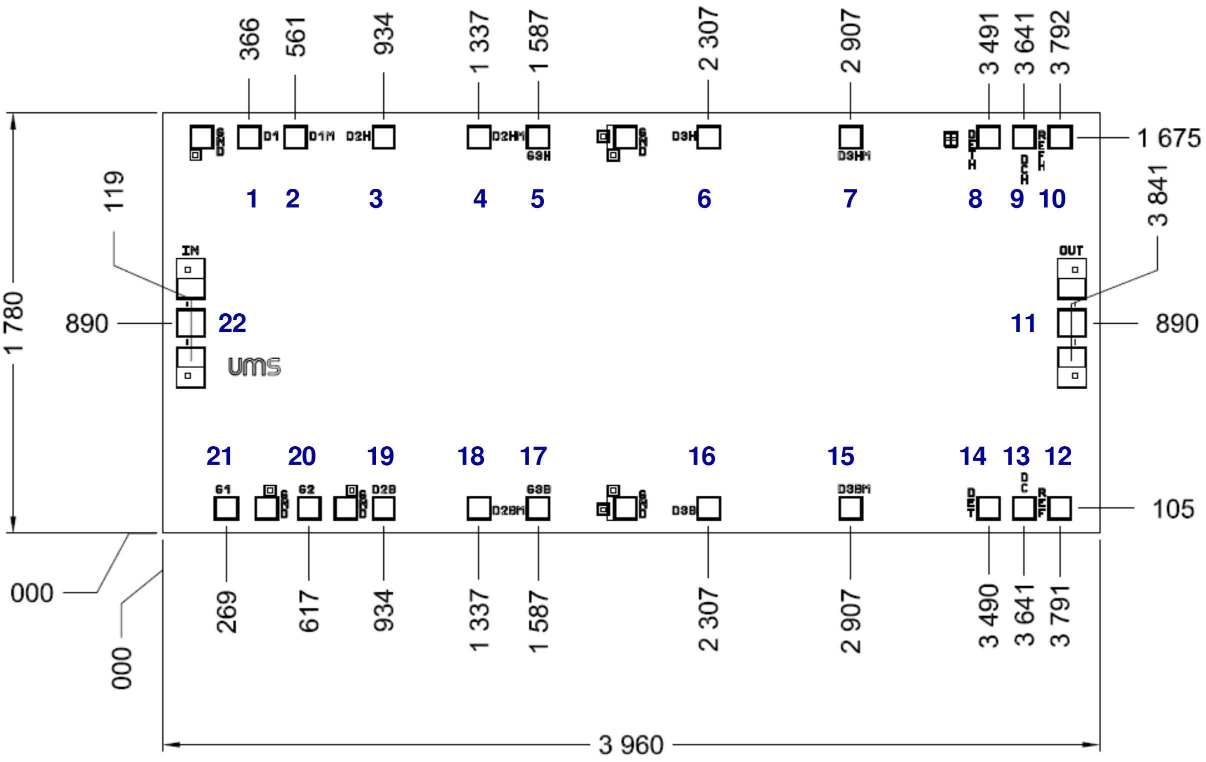
Input Return Loss versus Temperature



Output Return Loss versus Temperature



Mechanical data



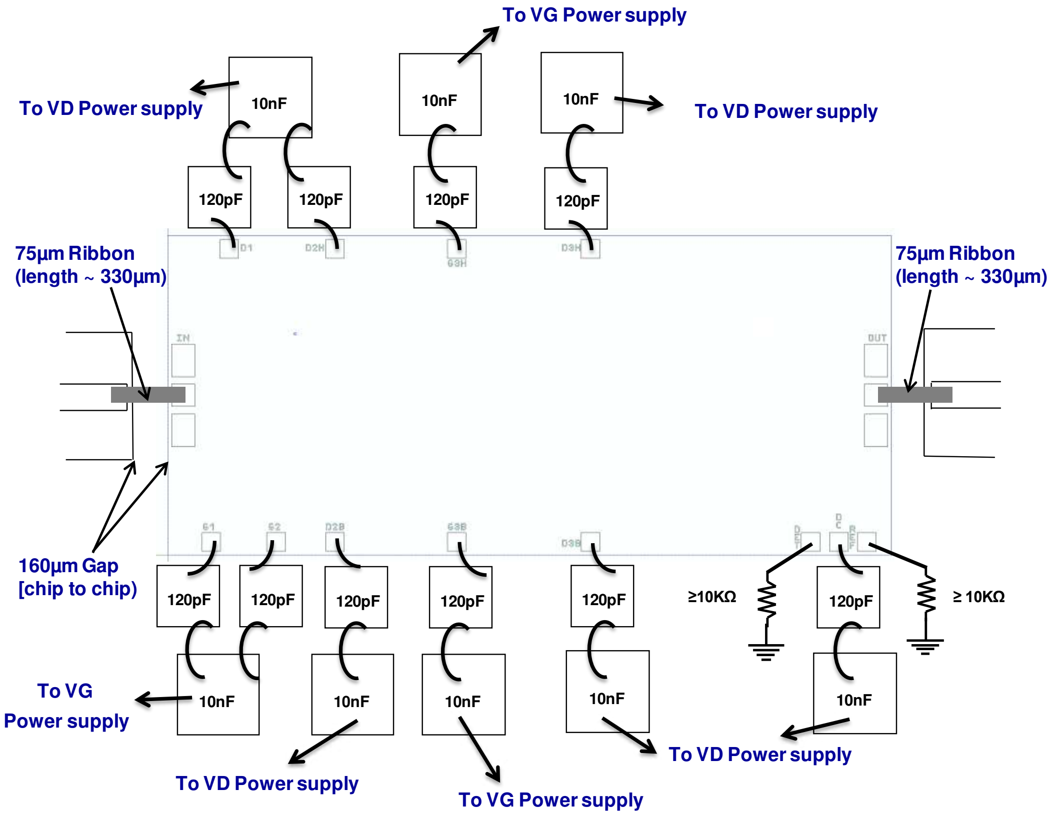
Chip thickness: 70µm.
Chip size: 3960x1780 ±35µm
All dimensions are in micrometers

RF Pads = 108 x 106 (BCB opening)
DC Pads = 86 x 83 (BCB opening)

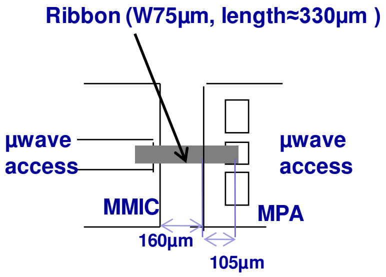
Recommended circuit bonding table

Pad number	Pad name	Description
1, 3, 6	D1; D2H; D3H	Drain voltage (3.5V, 160mA)
16, 19	D3B, D2B	Drain voltage (3.5V, 120mA)
5	G3H	Gate voltage (0.15V)
17, 20, 21	G3B, G2, G1	Gate voltage (0.15V)
14	DET	Detector output
12	REF	Detector reference output
13	DC	DC voltage detector (3.5V, 240µA)
22	IN	RF in
11	OUT	RF out
2, 4, 7	D1M; D2HM; D3HM	Not connected
15, 18	D3BM, D2BM	Not connected
8, 9, 10	DETH, DCH, REFH	Not connected
	GND	Not connected

Recommended assembly plan



The design of the circuit integrates a half ribbon (75µm wide) connection at the input and the output of the MMIC amplifier compliant with a 50 Ohm line on GaAs MMIC.
The circuits have to be as close as possible to each other; the ribbon length must be as short as possible: typically 160µm gap between two chips is considered, and the loop height must also be the smallest possible (80µm).

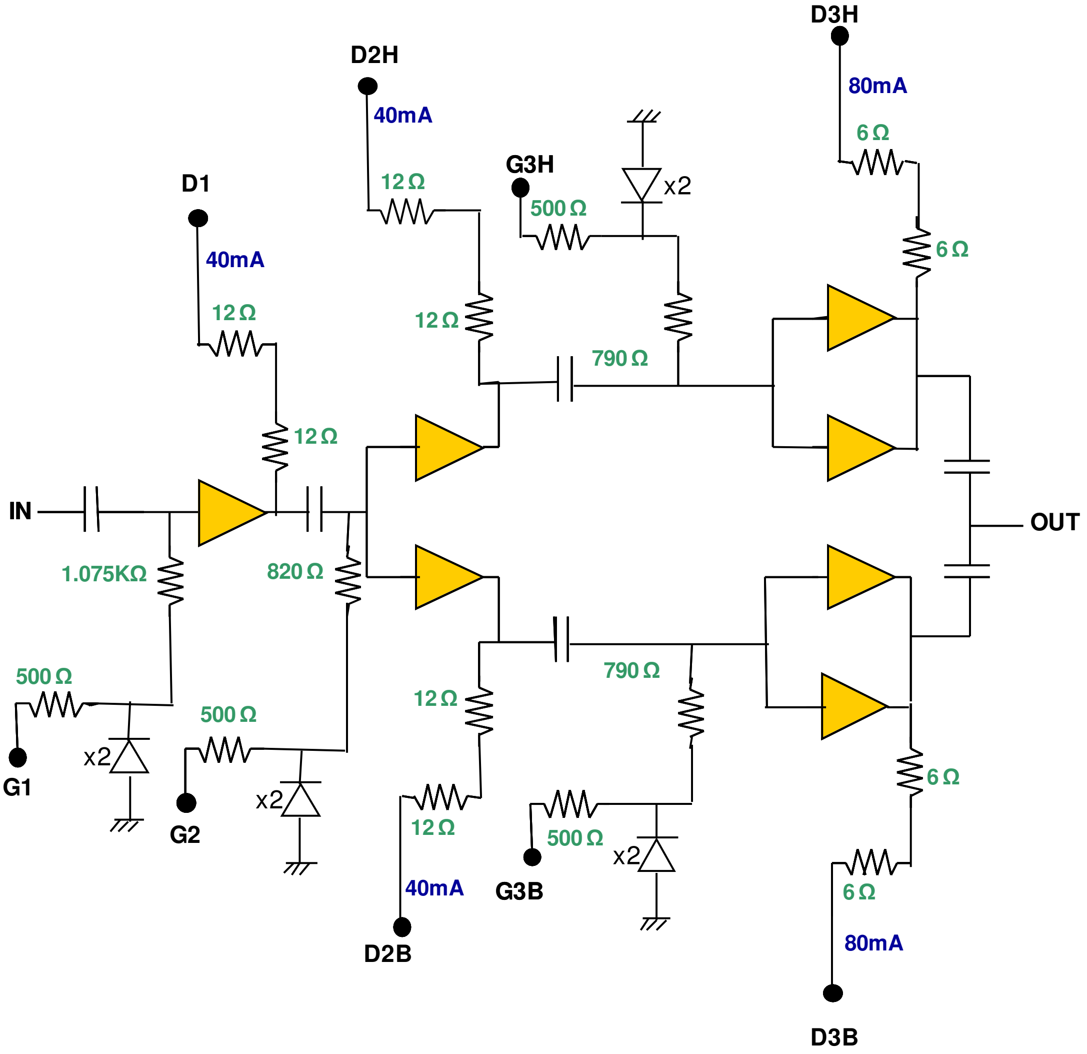


A second solution is to use wires (Ø 25µm). In this case a minimum of two wires together with the same chip to chip distance mention above are necessary to reduce the inductance effect. Nevertheless, simulations show an improvement of RF performance for E-band frequency range with the use of ribbon connection instead of wire.

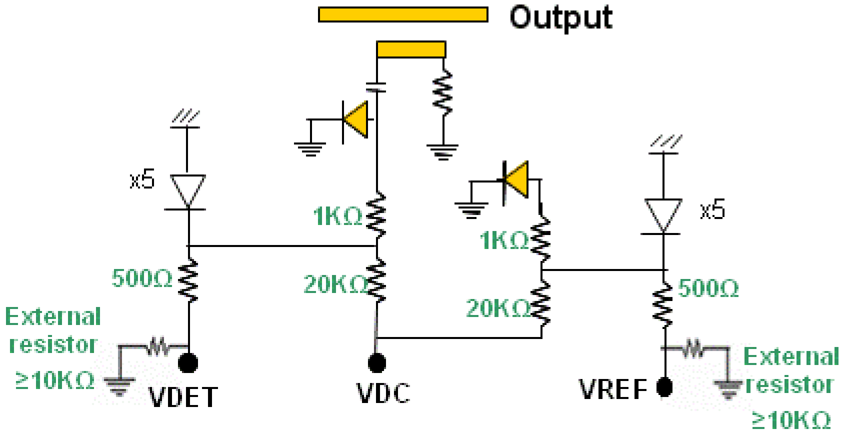
For DC connection (DC pads), a 25µm bonding is preferred.
Due to BCB coating on the chip, qualification domain requires the chip to be glued.

DC Schematic

3.5V, 280mA



Detector



Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA3080-98F/00