

20-40GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

Description

The CHA3093c is a high gain broadband four-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

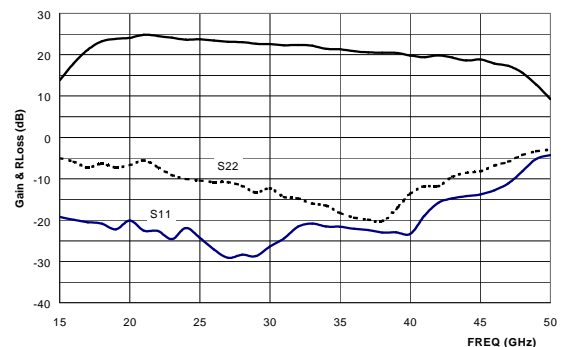
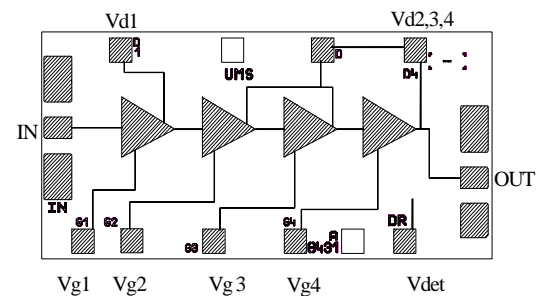
A B.I.T. (Build In Test) monitors a DC voltage that is representative of the microwave output power.

The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.

Main Features

- Broadband performances: 20-40GHz
- 20dBm output power
- 22dB gain
- Very good broadband input matching
- On chip output power level DC detector
- Low DC power consumption, 330mA @ 3.5V
- Chip size: 0.83 X 1.72 X 0.10mm



Input RLoss: solid line & output RLoss: dash line

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	20		40	GHz
G	Small signal gain	18	20		dB
P03	Output power at 3dB gain compression	20	22		dBm
Id	Bias current		330	400	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions

Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd1,2,3,4 = 3.5V Id=330mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	20		40	GHz
G	Small signal gain [20GHz to 35GHz](1)	20	22		dB
G	Small signal gain (1)	18			dB
ΔG	Small signal gain flatness (1) (Any 1GHz BW)		±0.5		dB
Is	Reverse isolation (1)		50		dB
P1dB	Pulsed output power at 1dB gain compression (1)	18	20		dBm
P3dB	Pulsed output power at 3dB gain compression (1)	20	22		dBm
IP3	3 rd order intercept point		29		dBm
PAE	Power added efficiency at saturation		10		%
VSWRin	Input VSWR (1)		1.2:1	2.0:1	
VSWRout	Output VSWR (1)		2.0:1	3.0:1	
NF	Noise figure		8.0	10.0	dB
Vdet	Detected voltage : at 25GHz @ Pout=20dBm (2)		0.65		V
	Detected voltage : at 38GHz @ Pout=20dBm (2)		0.45		V
Id	Bias current (small signal)		330	400	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) In the case of a jig or a module CW mode operation, the typical output power may be around 2dB less.

(2) Voltage across an external 10kOhm parallel resistor connected to the voltage detector pad.

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
Vds	Drain bias voltage_small signal (2)	4.0	V
Ids	Drain bias current_small signal	470	mA
Vgs	Gate bias voltage	-2 to +0.4	V
Vdg	Drain Gate voltage (Vds – Vgs)	+5	V
Pin	Maximum continuous input power (2)	+4 (@ 20GHz)	dBm
	Maximum peak input power overdrive	-1 (@ 40GHz) +15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s.

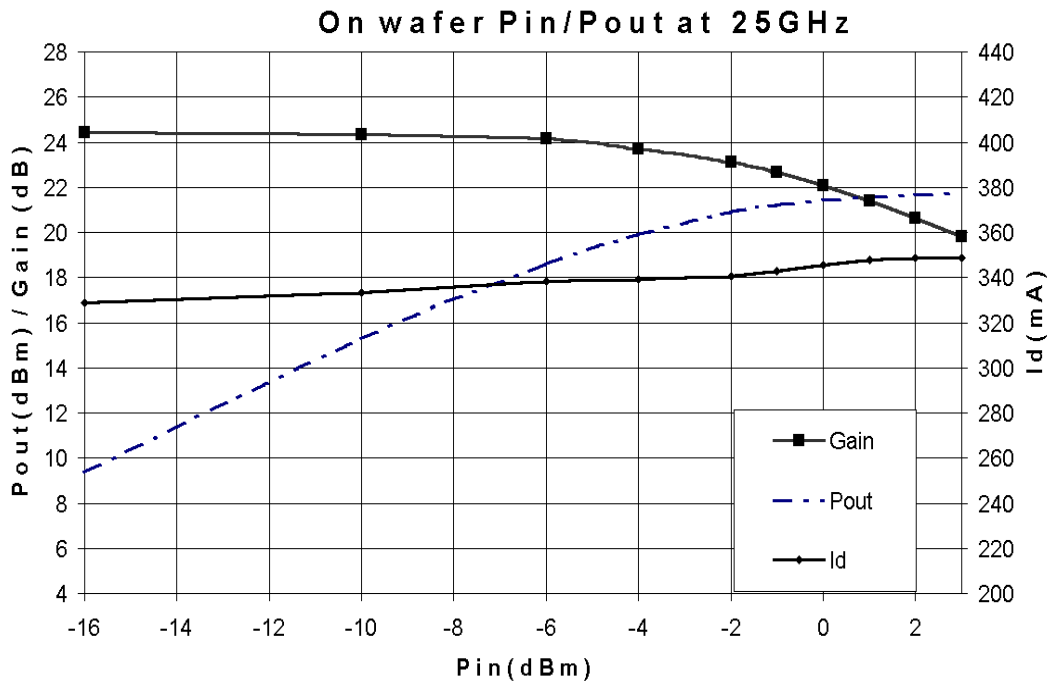
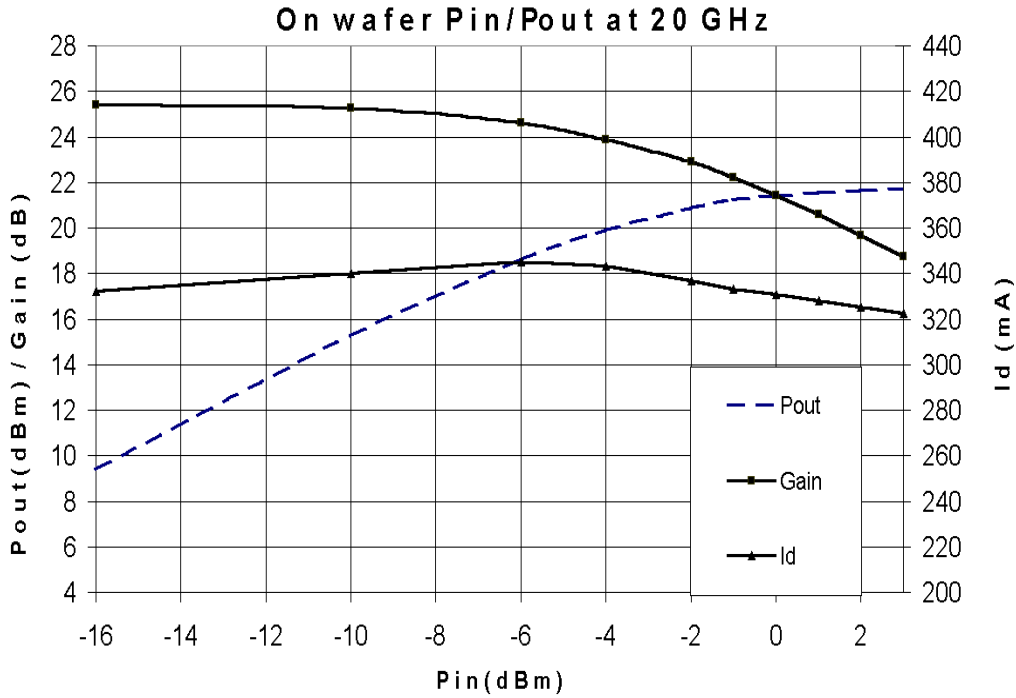
Typical Scattering Parameters (On wafer S_{ij} measurements)

Bias Conditions: $V_{d1,2,3,4} = 3.5\text{Volt}$, $V_{g1}=V_{g2,3,4}$ for $I_d \text{ total} = 330\text{mA}$.

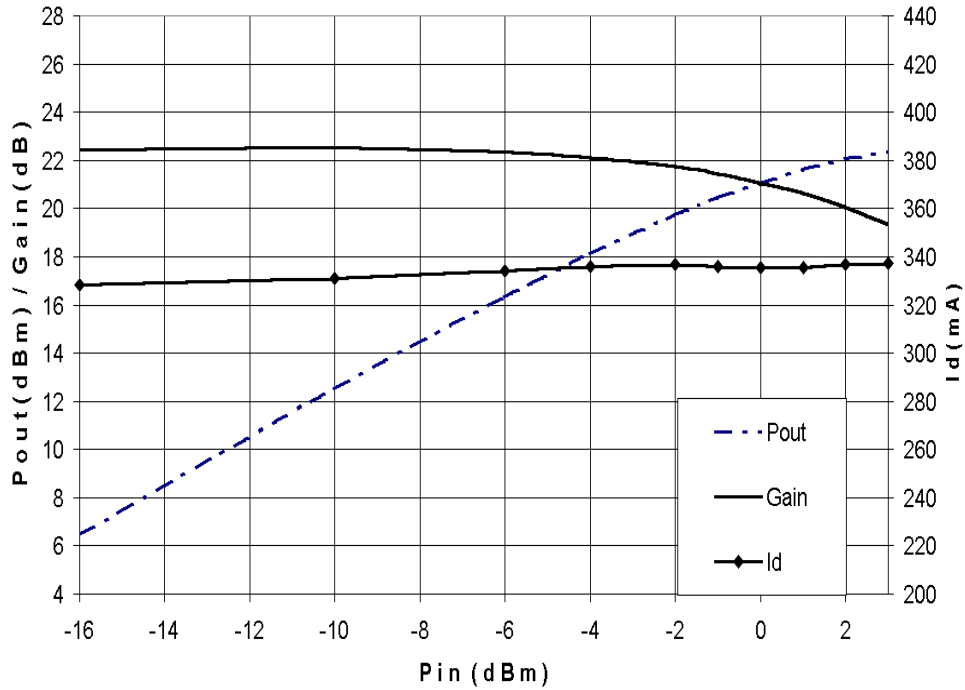
Freq GHz	S11		S12		S21		S22	
	mod dB	pha /°	mod dB	pha /°	mod dB	pha /°	mod dB	pha /°
2,00	-9,77	166,10	-79,63	85,41	-44,50	11,25	-0,06	-16,47
4,00	-9,97	159,94	-78,88	19,46	-45,28	64,07	-0,17	-32,94
6,00	-10,97	144,60	-63,16	-150,36	-32,41	-15,70	-0,26	-48,70
8,00	-12,23	141,58	-67,81	-92,96	-30,97	-73,10	-0,19	-66,41
10,00	-13,30	132,93	-76,00	168,10	-39,55	-81,72	-0,32	-86,37
12,00	-14,19	127,48	-69,79	162,87	-12,99	-8,19	-0,95	-109,99
14,00	-15,25	119,12	-68,09	-141,61	4,59	-92,82	-3,13	-134,29
16,00	-16,90	109,51	-56,64	151,79	14,64	166,69	-6,28	-148,92
18,00	-18,45	101,39	-77,66	-40,17	20,56	66,78	-12,44	-152,39
20,00	-18,27	99,66	-54,79	30,38	23,06	-25,87	-11,02	-127,42
21,00	-20,55	75,06	-69,47	-61,55	23,87	-67,24	-8,60	-138,79
22,00	-20,72	49,52	-57,54	-51,49	24,20	-106,39	-7,90	-148,31
23,00	-29,56	58,15	-54,03	-168,51	23,40	-146,58	-10,21	-167,46
24,00	-23,58	58,28	-56,11	107,75	22,98	-173,95	-10,20	-161,72
25,00	-21,33	29,56	-54,05	67,67	22,93	156,61	-10,87	-166,58
26,00	-21,32	-8,76	-62,57	-37,46	23,05	125,30	-11,82	179,69
27,00	-22,06	-29,59	-63,41	-139,56	22,56	96,27	-13,75	179,91
28,00	-22,21	-31,27	-56,43	165,63	21,93	70,69	-13,72	-176,79
29,00	-19,66	-44,67	-59,88	138,12	22,19	43,16	-13,95	168,88
30,00	-17,80	-56,40	-58,46	132,33	21,80	16,81	-15,15	167,61
31,00	-17,46	-61,68	-56,48	154,53	21,36	-6,65	-15,78	157,73
32,00	-15,16	-70,64	-52,06	105,41	21,50	-31,90	-15,57	137,58
33,00	-15,09	-83,96	-56,43	63,48	20,88	-56,82	-20,24	133,08
34,00	-14,57	-89,19	-59,91	89,24	20,82	-81,12	-19,36	132,46
35,00	-13,80	-92,45	-54,72	94,43	20,70	-104,79	-18,36	101,23
36,00	-13,55	-97,98	-54,97	59,43	20,47	-129,10	-20,65	80,50
37,00	-12,80	-102,27	-54,75	93,32	20,11	-154,27	-17,69	61,37
38,00	-12,55	-108,34	-54,06	58,24	19,72	-177,11	-18,18	37,45
39,00	-12,64	-110,41	-53,05	50,25	19,84	159,83	-15,31	24,91
40,00	-12,53	-108,87	-50,99	30,11	19,49	133,90	-13,49	5,75
41,00	-11,23	-110,01	-52,73	3,78	19,40	108,31	-11,73	-9,23
42,00	-10,73	-118,61	-56,04	22,66	18,88	81,37	-11,60	-21,67
43,00	-10,79	-124,01	-56,86	-6,86	18,38	56,83	-10,29	-23,61
44,00	-10,93	-121,39	-52,92	-31,58	18,36	32,20	-8,52	-33,55
45,00	-10,92	-125,62	-52,23	-85,31	18,33	-0,36	-7,30	-45,47
46,00	-11,37	-121,74	-60,67	-166,71	17,03	-37,26	-7,39	-51,37
48,00	-8,41	-103,89	-53,21	-121,20	13,67	-104,46	-4,69	-68,35
50,00	-5,96	-119,91	-58,10	116,39	6,60	-158,83	-3,75	-85,06
52,00	-3,89	-131,50	-52,69	160,04	-0,07	156,43	-3,23	-99,24
54,00	-2,88	-146,98	-60,21	15,97	-7,50	118,68	-2,74	-112,94
56,00	-2,21	-160,52	-52,63	159,63	-16,29	95,16	-2,57	-124,78
58,00	-2,02	-173,49	-55,84	-175,77	-29,86	112,18	-2,56	-135,15
60,00	-1,87	175,37	-49,76	95,59	-23,82	170,18	-2,53	-145,16

Typical On wafer Power CW Measurements

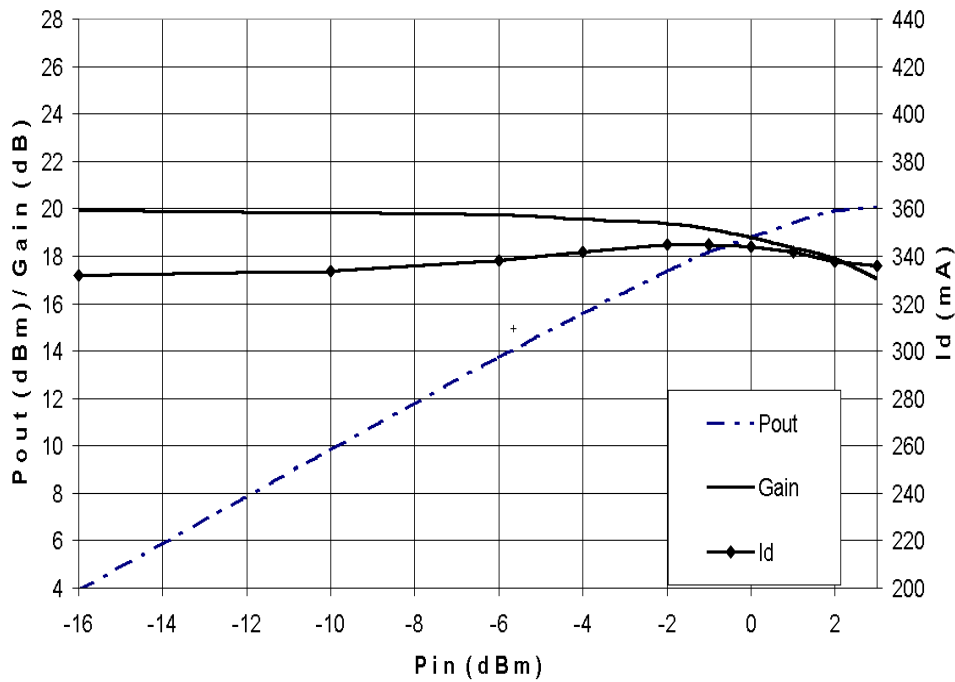
Bias Conditions: $V_{d1,2,3,4} = 3.5\text{V}$, $V_{g1,2,3,4}$ for $I_d = 330\text{mA}$



On wafer Pin/Pout at 30 GHz



On wafer Pin / Pout at 40GHz

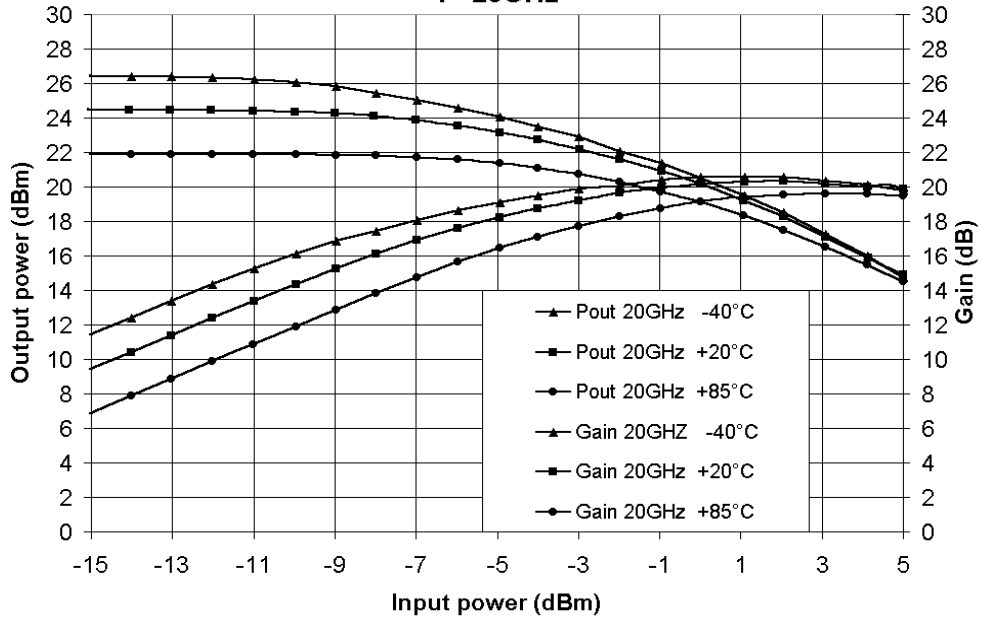


Typical IN TEST JIG Power Measurements in temperature

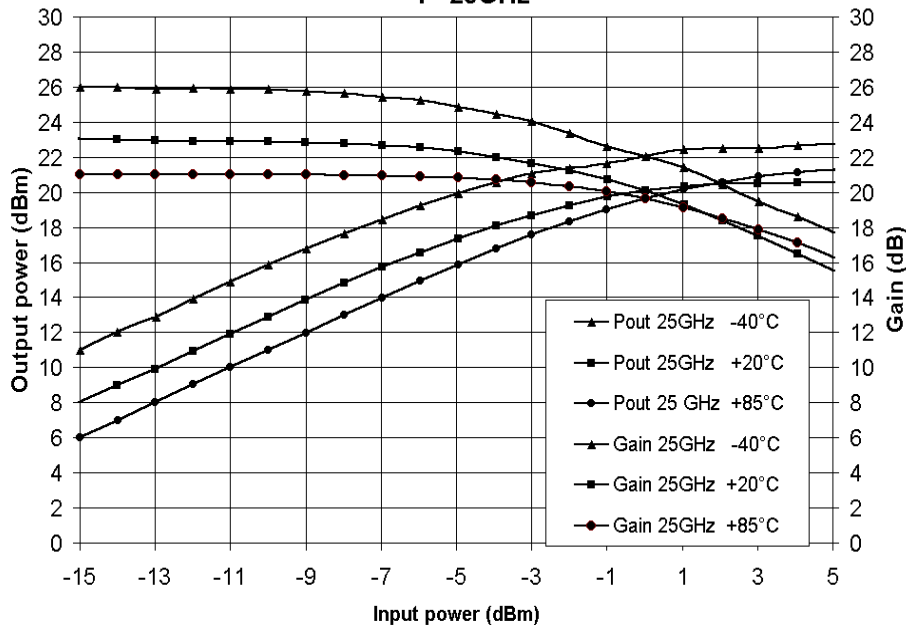
Note: Jig losses included (1 dB)

Bias Conditions: $V_{d1,2,3,4} = 3.5\text{Volt}$, $V_{g1,2,3,4}$ for $I_d = 330\text{mA}$

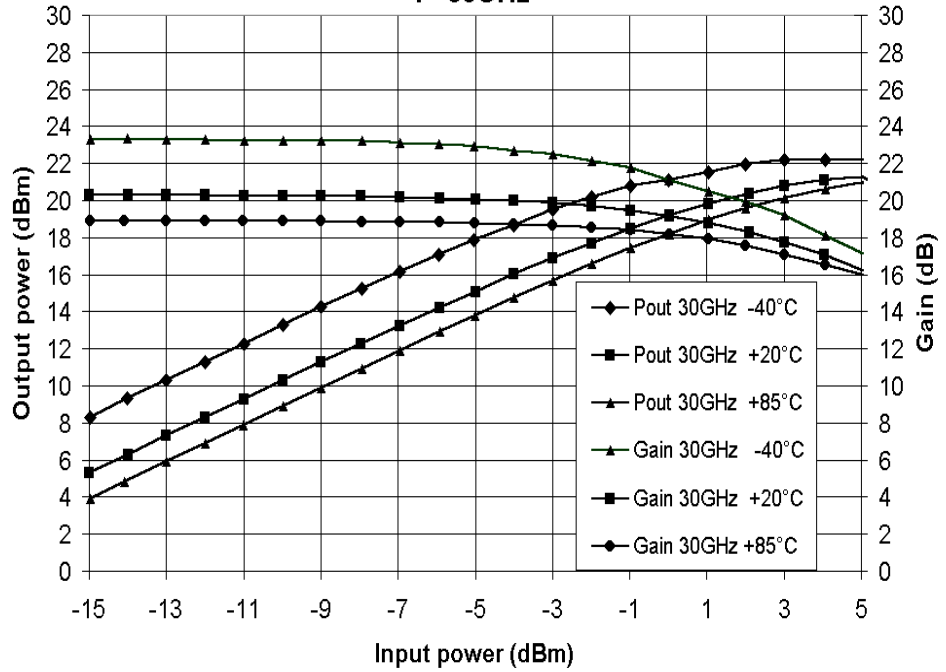
**OUTPUT POWER TEMPERATURE MEASUREMENTS IN TEST JIG
F=20GHz**



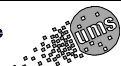
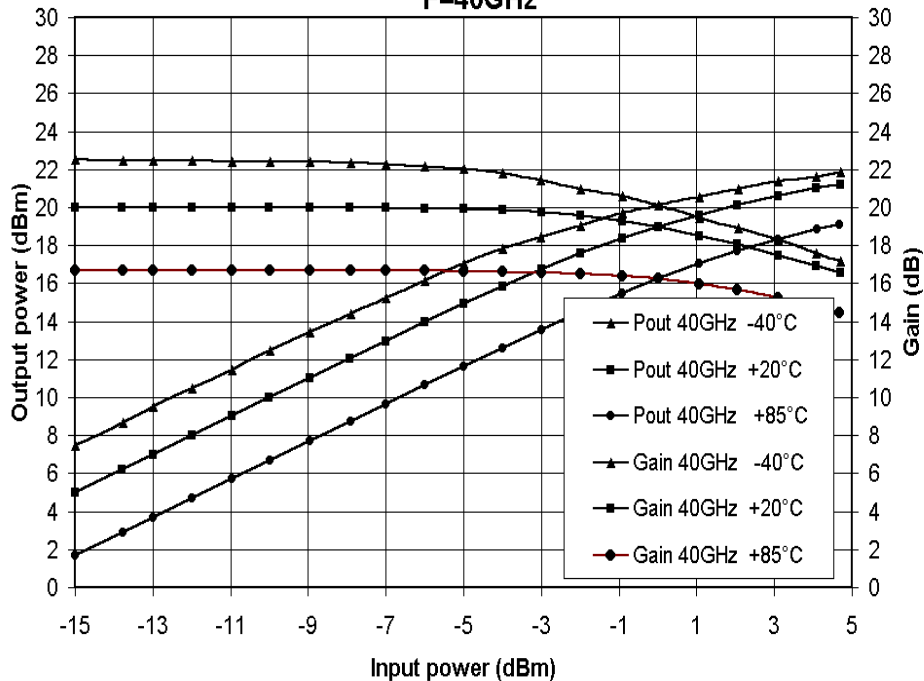
**OUTPUT POWER TEMPERATURE MEASUREMENTS IN TEST JIG
F=25GHz**



OUTPUT POWER TEMPERATURE MEASUREMENTS IN TEST JIG
F=30GHz

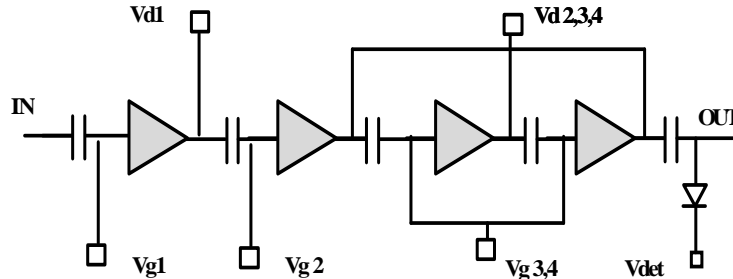


OUTPUT POWER TEMPERATURE MEASUREMENTS IN TEST JIG
F=40GHz



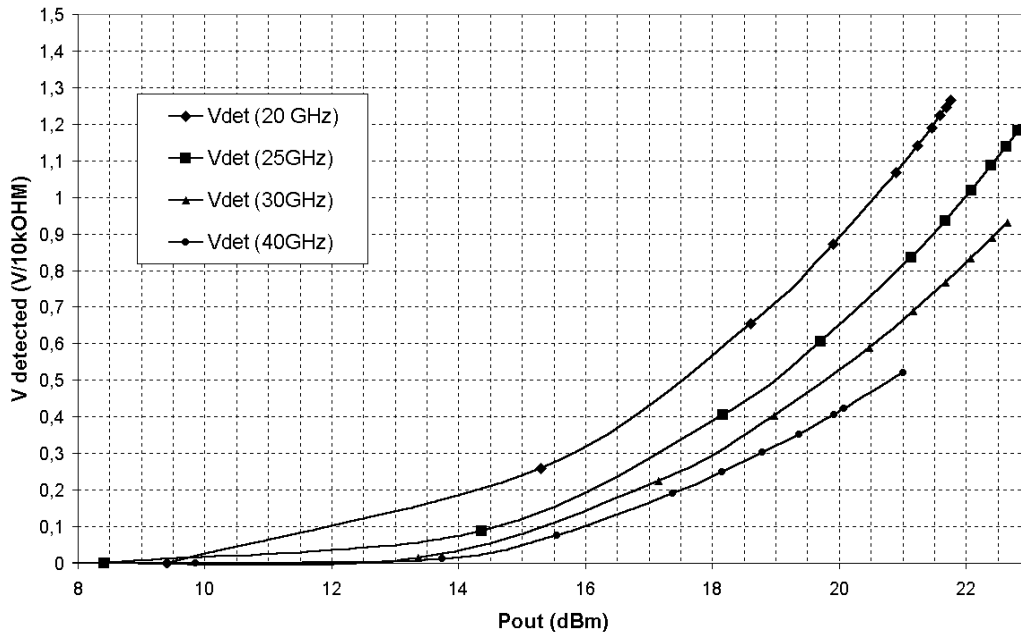
Typical Bias Tuning

The circuit schematic is given below:



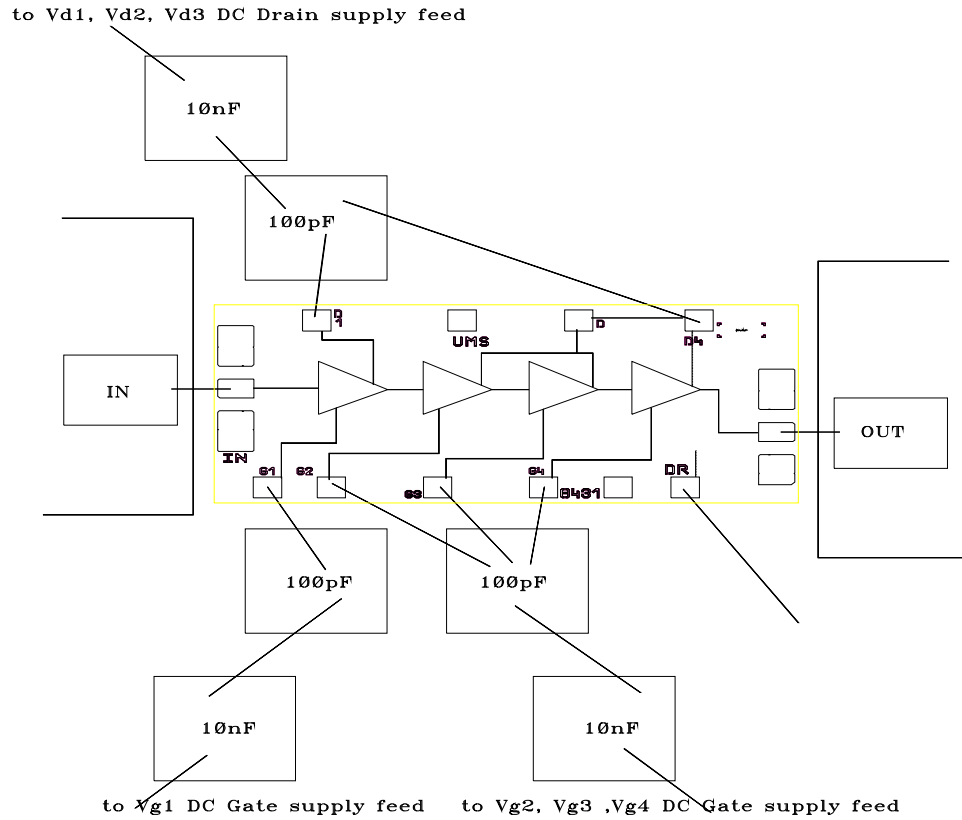
For medium power operation, the four drain biases are connected altogether. In a same way, all the gate biases are connected together at the same power supply, tuned to drive a small signal operating current of 300mA. A separate access to the gate voltages of the two first stages (Vg1, 2) is provided in order to be able to tune the first stages for the application, as a lower noise amplifier or a multiplier.

An additional pad is provided for monitoring the output power, using the Build In Test. This access, when connected to an external resistor of 10Kohm (typical value) provides a DC voltage which follows the output power level.

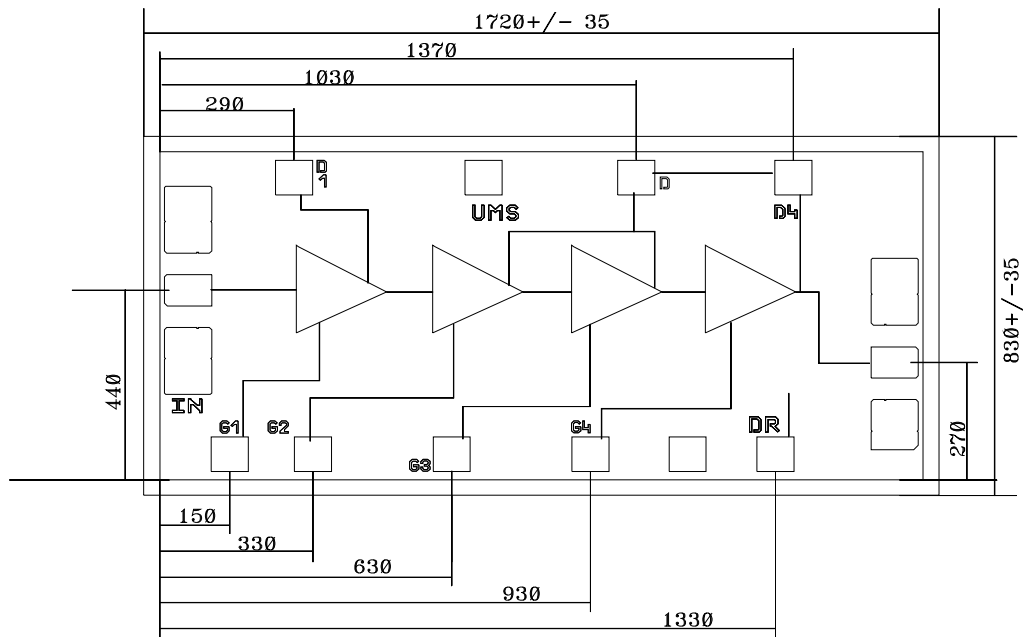


On wafer power measurements versus output power

Chip Assembly and Mechanical Data



Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions

(Chip thickness: 100µm. All dimensions are in micrometers)

Ordering Information

Chip form : CHA3093c99F/00

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