20-40GHz High Gain Buffer Amplifier

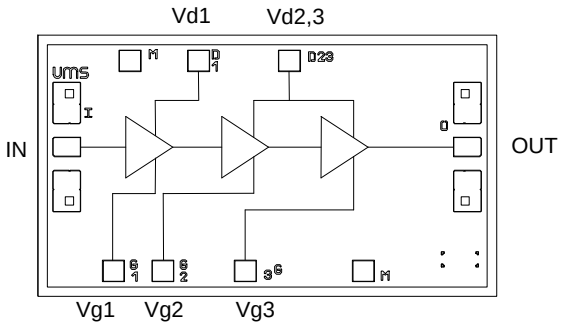
GaAs Monolithic Microwave IC

Description

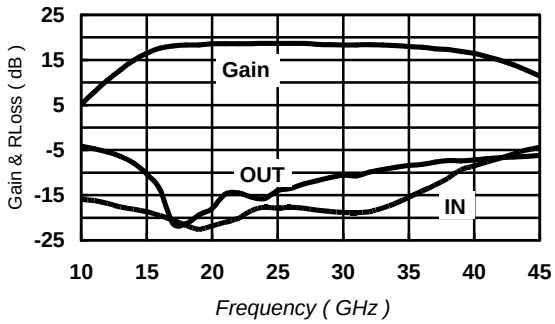
The CHA2098b is a high gain broadband three-stage monolithic buffer amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on-wafer results



Main Features

- Broadband performances: 20-40GHz
- 16dBm output power (1dB gain comp)
- 19dB ±1.5dB gain
- Low DC power consumption, 150mA @ 3.5V
- Chip size: 1.67 X 0.97 X 0.10mm

Main Characteristics

Tamb. = 25℃

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	20		40	GHz
G	Small signal gain	17	19		dB
P1dB	Output power at 1dB gain compression	13	16		dBm
Id	Bias current		150	200	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd1,2,3 = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	20		40	GHz
G	Small signal gain (1)	17	19		dB
ΔG	Small signal gain flatness (1)		±1.5		dB
Is	Reverse isolation (1)		30		dB
P1db	Output power at 1dB gain compression (1)	13	16		dBm
P03	Output power at 3dB gain compression	15	16		dBm
VSWRin	Input VSWR (1)			3.0:1	
VSWRout	Output VSWR (1)			3.0:1	
NF	Noise figure			10.0	dB
Id	Bias current		150	200	mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	200	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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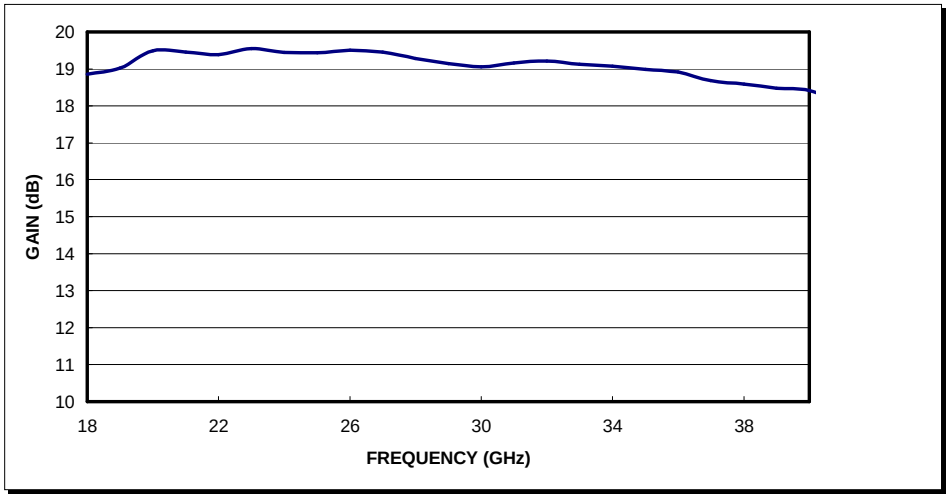
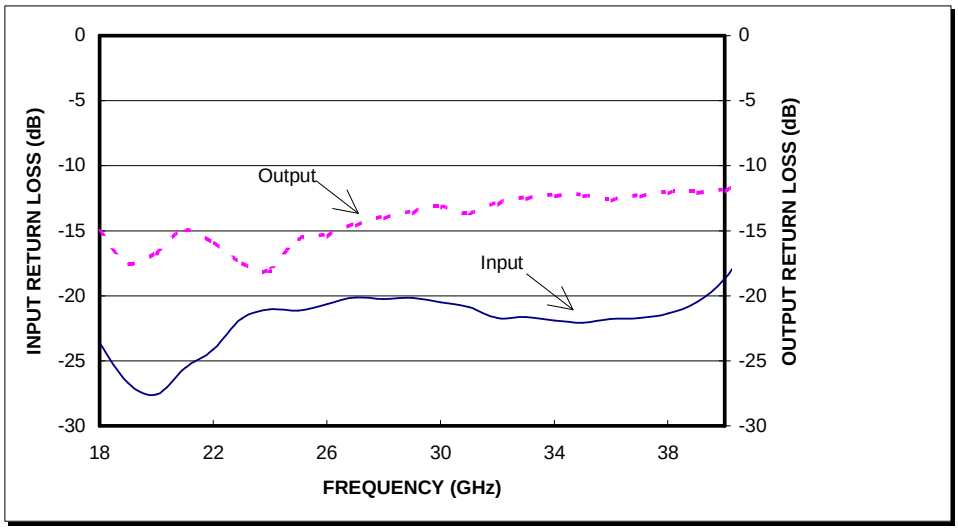
Typical Performance

Tamb=+25°C, Vd=3.5V, Vg=-0.1V



Gain vs Frequency



Input and Output Loss vs. Frequency

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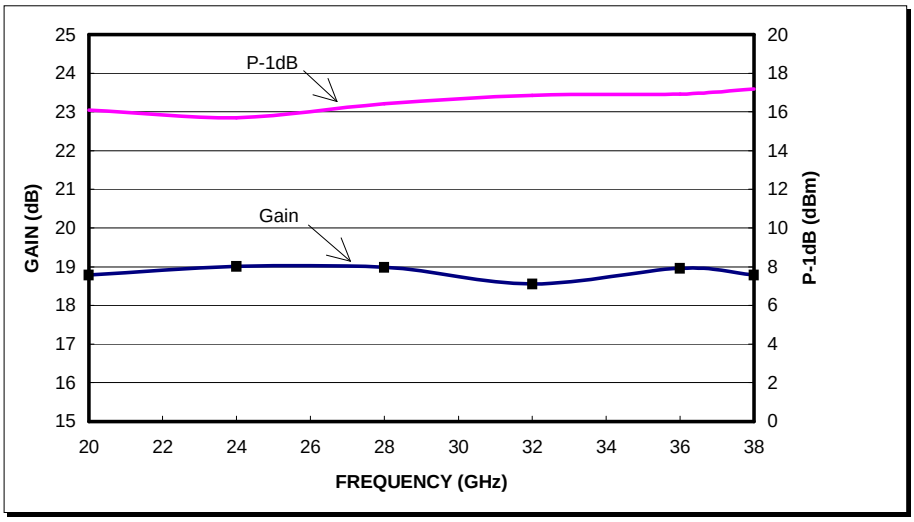
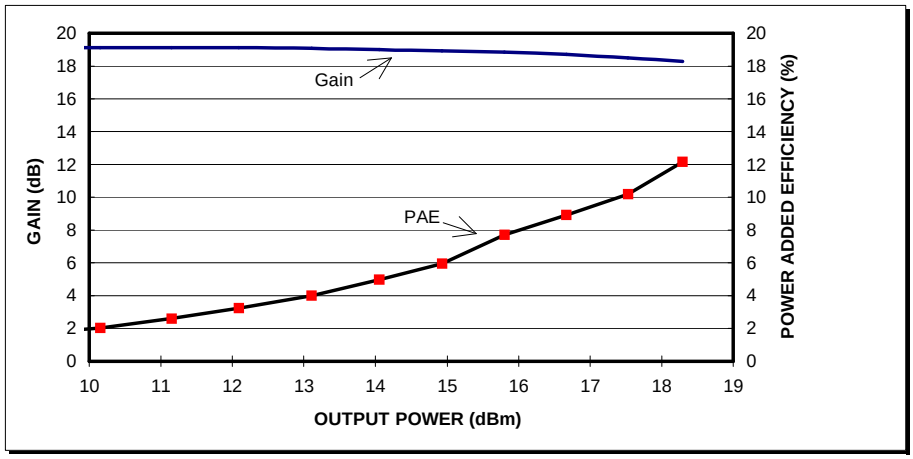
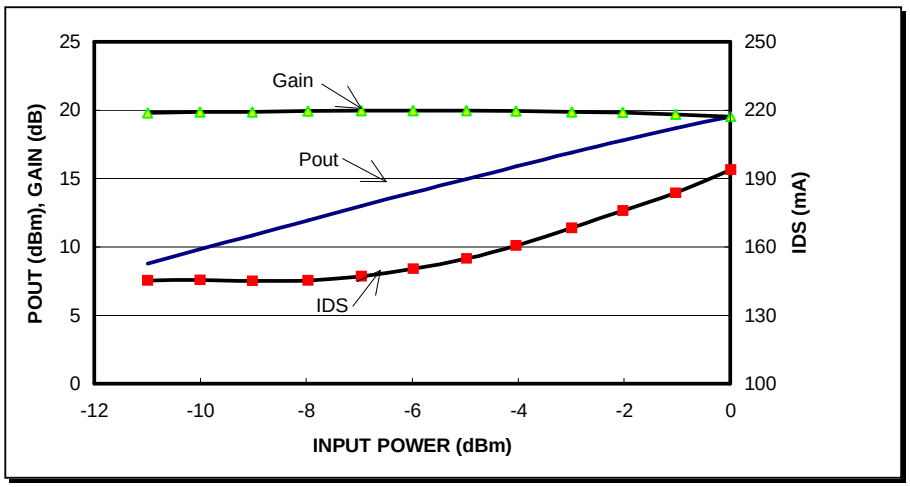


Gain and Compressed Power vs. Frequency



Gain and Efficiency Vs Output Power (F=30GHz)



Gain, Output Power and IDS vs. Input Power (F=38GHz)

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Typical Scattering Parameters (on Wafer)

Bias conditions: Vd=3.5V Vg=0V

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
15	-18.37	116.1	-69.59	148.0	16.72	130.6	-7.99	77.7
16	-19.49	113.8	-65.95	154.4	18.13	102.0	-10.02	51.4
17	-20.63	113.4	-65.20	-158.1	18.90	73.7	-13.84	20.3
18	-22.15	114.4	-60.58	155.1	19.31	46.4	-16.29	-13.8
19	-24.36	120.5	-58.79	155.7	19.42	22.3	-19.17	-64.4
20	-26.49	140.0	-54.42	136.8	19.97	-1.6	-18.06	-99.8
21	-24.05	163.8	-51.83	127.3	19.63	-27.5	-16.16	-138.5
22	-22.26	156.6	-52.04	81.3	18.79	-46.8	-16.79	-168.8
23	-21.20	159.0	-60.55	107.0	18.65	-57.2	-17.79	168.2
24	-20.46	150.9	-54.03	100.6	19.86	-80.0	-18.36	-171.8
25	-20.57	148.8	-50.49	90.6	19.82	-102.7	-15.84	175.6
26	-20.37	145.4	-49.95	75.8	19.89	-121.3	-15.59	171.0
27	-20.01	141.8	-49.48	67.0	19.82	-142.0	-14.72	159.9
28	-20.38	136.9	-48.65	53.7	19.60	-161.3	-14.17	154.0
29	-20.51	132.4	-48.33	37.5	19.53	-179.4	-13.37	144.0
30	-21.26	127.2	-49.24	25.1	19.45	162.3	-12.84	131.6
31	-21.82	125.6	-47.95	22.8	19.64	144.2	-13.15	123.6
32	-22.62	129.0	-47.60	3.6	19.53	123.6	-12.50	114.6
33	-21.97	127.4	-48.30	-3.7	19.28	104.7	-12.28	102.1
34	-22.69	118.7	-45.57	-22.6	19.27	86.4	-11.93	93.5
35	-23.12	114.3	-47.53	-45.6	19.15	66.9	-11.82	79.2
36	-22.50	103.9	-48.92	-49.1	18.96	46.8	-12.13	67.7
37	-22.15	91.0	-48.07	-69.1	18.52	28.3	-12.07	58.5
38	-20.65	71.9	-49.33	-67.4	18.36	10.1	-11.87	47.6
39	-18.94	39.2	-46.75	-105.6	18.43	-9.4	-10.98	36.1
40	-17.28	8.4	-47.08	-108.5	18.34	-31.1	-10.60	19.8
41	-14.60	-18.5	-48.00	-134.6	17.82	-53.7	-10.11	6.4
42	-12.20	-40.3	-47.52	-160.4	17.39	-76.8	-9.83	-7.0
43	-10.21	-59.7	-46.21	160.6	16.75	-99.2	-9.28	-20.8
44	-8.25	-80.9	-49.74	147.7	15.88	-123.1	-8.54	-37.0
45	-6.83	-97.6	-48.99	136.5	14.64	-145.6	-8.12	-50.7
46	-5.68	-113.3	-53.12	32.5	13.15	-167.2	-7.61	-62.9
47	-4.73	-129.1	-50.08	-34.8	11.65	172.2	-7.25	-77.1

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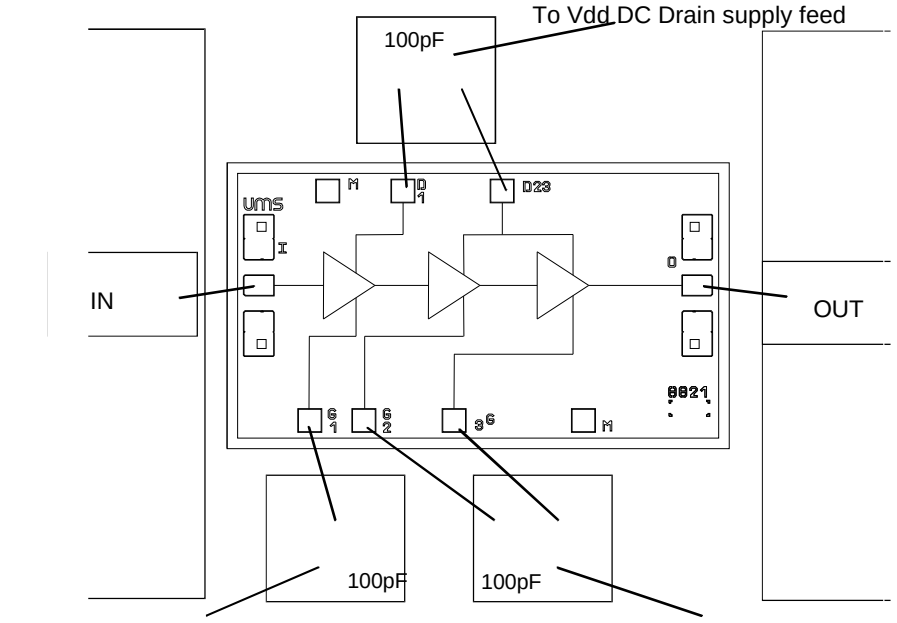
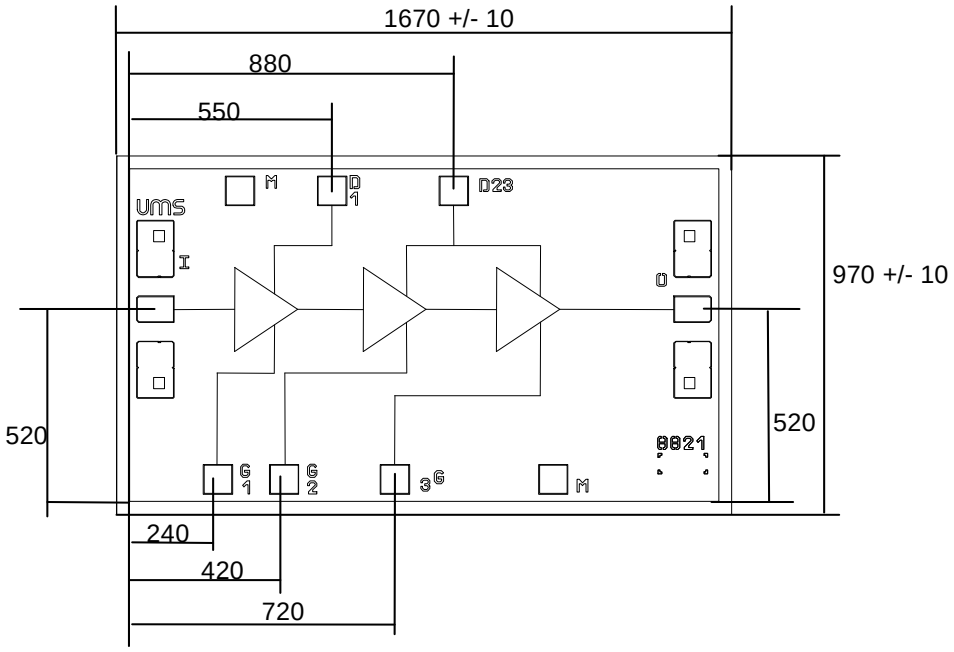
Chip Assembly and Mechanical Data



Note: Supply feed should be capacitively bypassed.



Bonding pad positions.
(Chip thickness : 100µm. All dimensions are in micrometers)

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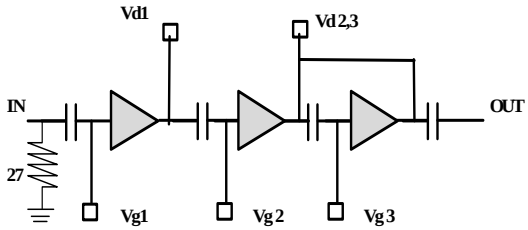
Typical Bias Tuning

The circuit schematic is given below:



For typical operation, the three drain biases are connected altogether. In a same way, all the gate biases are connected together at the same power supply, tuned to drive a small signal operating current of 130mA. A separate access to the gate voltages of each stage (Vg1,2 & 3) is provided for the fine tuning of the stages regarding the application.

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Ordering Information

Chip form : CHA2098b99F/00

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