

17- 24GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA4253-QQG is a 4stage monolithic circuit, which delivers 24dBm for a gain at 23dB.

It is designed for a wide range of applications, from military to commercial communication systems.

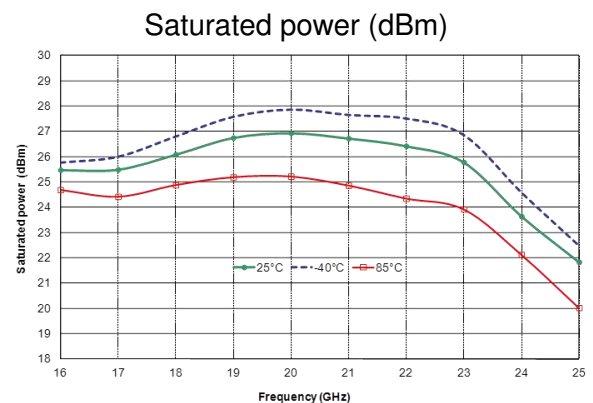
The circuit is manufactured with a pHEMT process, 0.15µm gate length.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 17- 24GHz
- 24dBm Pout for 1dB compression
- 23dB gain
- 33dBm OTOI
- DC bias: Vd= 5.0V, Id= 270mA
- QQG- QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25 °C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		24.0	GHz
Gain	Linear Gain		23		dB
P-1dB	Output Power @1dB comp.		24		dBm
OTOI	3 rd order Intercept point		33		dBm

Electrical Characteristics

Tamb.= +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		24.0	GHz
Gain	Linear Gain		23.0		dB
ΔG	Gain variation in temperature		0.06		dB/°C
OTOI	3 rd order Intercept point		33		dBm
P _{-1dB}	Output power @ 1dB compression		24		dBm
Psat	Saturated Output Power		25		dBm
RLin	Input Return Loss		12		dB
RLout	Output Return Loss		8		dB
NF	Noise figure		9.5		dB
Id	Quiescent Drain current		270		mA
Vg	Gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6V	V
Id	Drain bias quiescent current	320	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum input power	10	dBm
Tj	Junction temperature ⁽²⁾	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

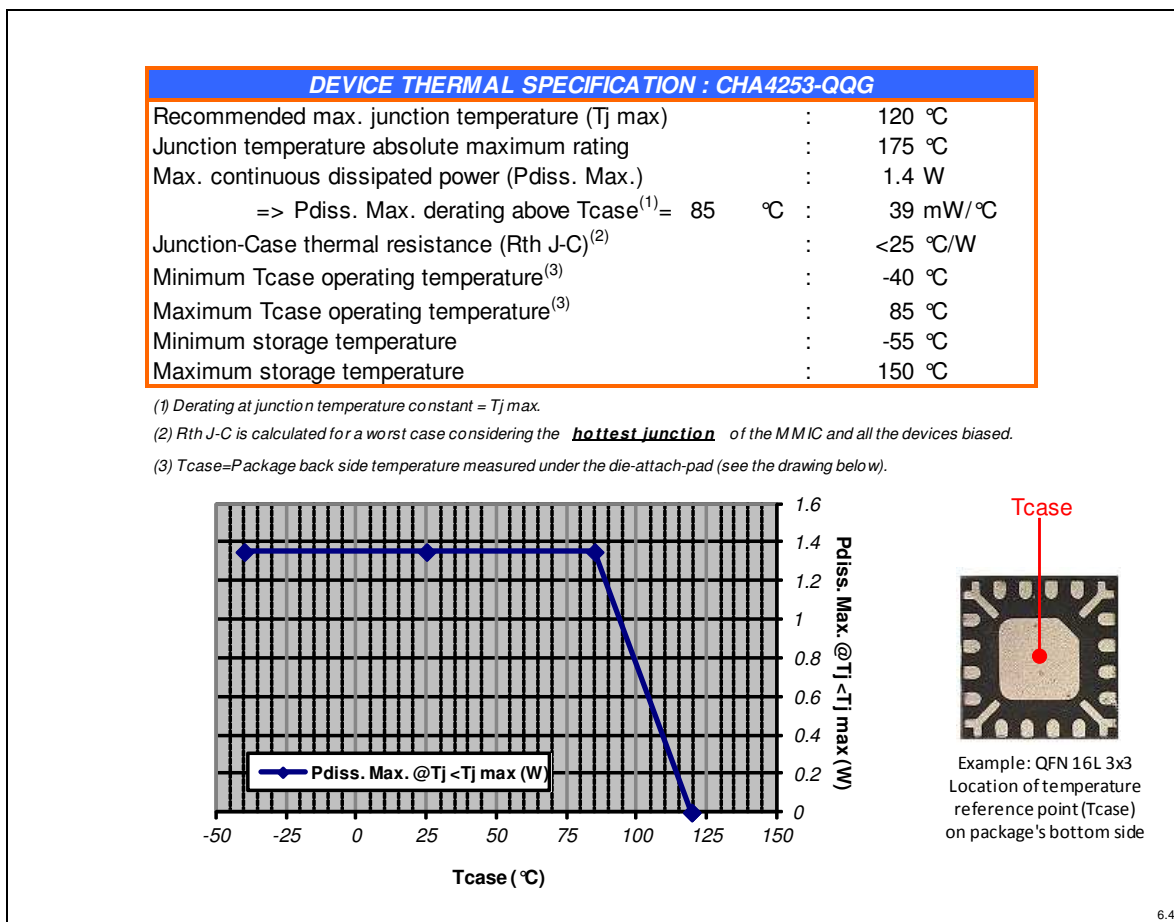
Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd123	6	DC Drain voltage 1 st , 2 nd & 3 rd stage	5	V
Vd4	7	DC Drain voltage 4th stage	5	V
Vg12	16	DC Gate voltage 1st & 2 nd stage	-0.7	V
Vg34	14	DC Gate voltage 3rd & 4th stage	-0.7	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below the maximum temperature specified (see the curve $P_{diss. Max}$) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters

Tamb.= +25°C, Vd = +5.0V, Id = 270mA

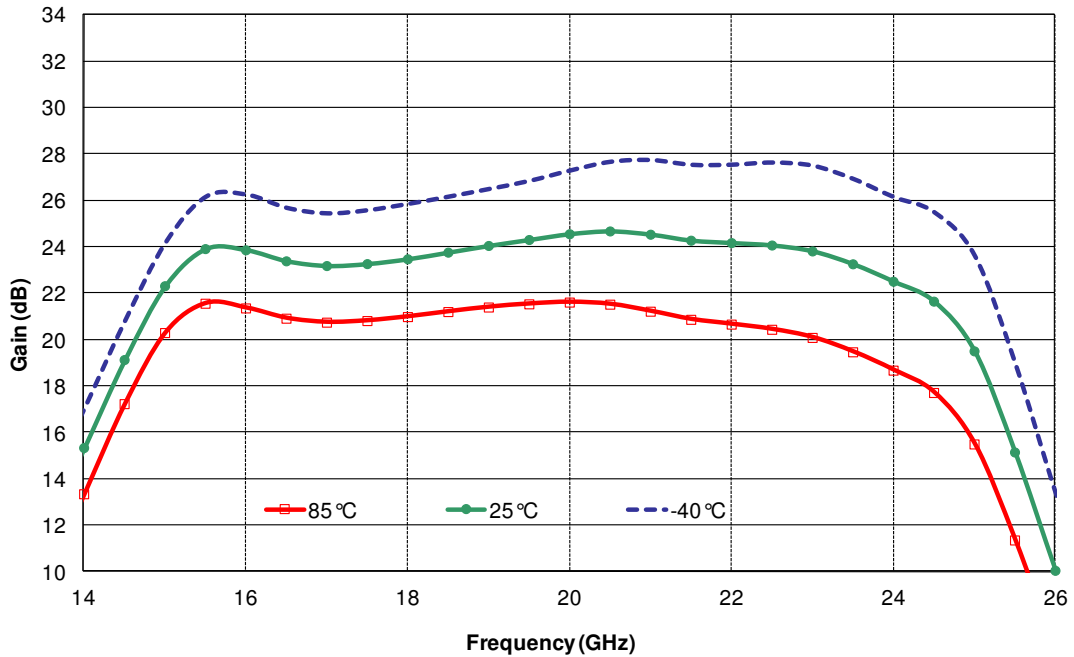
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2	-0.232	-41.4	-73.099	-138.9	-24.507	-105.6	-0.666	-142.0
2.5	-0.200	-51.0	-74.772	-162.1	-21.191	-148.6	-0.859	-163.5
3	-0.199	-61.1	-71.509	143.2	-20.151	115.6	-0.467	179.8
3.5	-0.214	-70.8	-68.453	148.3	-24.105	40.6	-0.434	162.7
4	-0.239	-80.5	-67.406	120.1	-29.123	-31.2	-0.412	147.2
4.5	-0.299	-90.0	-68.024	117.4	-35.234	-101.3	-0.418	132.6
5	-0.440	-99.3	-67.281	124.4	-43.427	-115.6	-0.432	118.8
5.5	-0.491	-107.8	-63.840	128.5	-30.860	-152.2	-0.462	105.1
6	-0.464	-116.7	-62.635	86.9	-26.570	147.1	-0.507	91.7
6.5	-0.353	-126.7	-59.993	98.7	-23.658	100.9	-0.616	77.9
7	-0.470	-135.5	-58.460	89.2	-21.153	63.8	-0.699	65.2
7.5	-0.503	-146.9	-55.613	70.9	-18.936	26.5	-0.721	52.0
8	-0.339	-157.6	-54.294	55.8	-16.180	-6.5	-0.881	38.9
8.5	-0.615	-167.5	-52.732	16.0	-13.947	-39.8	-1.208	26.5
9	-1.033	175.4	-51.962	-12.3	-11.674	-72.7	-1.339	12.7
9.5	-0.894	163.9	-53.032	-50.2	-9.242	-105.0	-1.542	1.5
10	-1.225	149.0	-52.969	-86.7	-6.627	-135.0	-1.812	-11.9
10.5	-2.115	131.4	-55.294	-131.9	-4.168	-167.6	-2.070	-24.5
11	-2.205	114.4	-55.668	-150.1	-1.466	161.5	-2.268	-37.5
11.5	-3.372	98.0	-57.540	-174.9	1.114	130.1	-2.592	-48.7
12	-4.159	77.4	-57.712	-177.0	3.967	97.0	-3.092	-61.7
12.5	-5.379	56.6	-52.812	168.6	6.904	63.0	-3.568	-74.9
13	-6.882	34.0	-50.050	138.9	9.766	26.6	-4.287	-88.2
13.5	-8.538	11.6	-51.550	104.0	13.151	-11.3	-5.193	-101.4
14	-10.164	-13.2	-54.463	115.5	16.674	-51.6	-6.436	-114.4
14.5	-11.739	-37.5	-49.971	105.4	20.151	-97.3	-8.193	-122.5
15	-13.365	-65.2	-49.325	87.9	22.647	-154.5	-10.355	-119.2
15.5	-15.112	-90.1	-47.508	81.3	23.836	147.3	-9.190	-122.0
16	-15.360	-102.8	-45.529	63.7	23.723	96.7	-8.605	-134.9
16.5	-14.384	-127.8	-47.764	35.2	23.651	50.1	-9.930	-153.2
17	-13.283	-147.6	-48.352	16.4	23.182	6.4	-11.690	-154.1
17.5	-14.749	-176.6	-53.653	-2.4	23.166	-34.9	-12.070	-156.2
18	-14.646	163.9	-59.889	47.5	23.538	-76.7	-11.471	-171.1
18.5	-16.070	144.7	-53.968	78.5	23.934	-118.8	-13.205	175.8
19	-17.953	117.2	-49.590	84.5	24.053	-158.1	-14.217	179.6
19.5	-22.563	110.2	-47.464	68.7	24.401	156.1	-11.852	177.8
20	-28.117	132.9	-44.697	55.3	24.598	110.4	-10.251	151.6
20.5	-23.594	139.6	-45.854	39.3	24.163	65.8	-10.488	123.3
21	-25.405	121.6	-43.872	41.1	24.438	21.7	-10.111	101.2
22	-28.865	132.3	-45.308	24.7	24.140	-69.1	-9.618	66.7
22.5	-31.230	-110.2	-43.460	24.5	23.554	-120.0	-8.577	48.9
23	-19.201	-171.5	-41.705	20.0	22.788	-169.2	-6.571	33.9
23.5	-14.285	150.3	-40.202	21.0	22.291	143.8	-4.755	18.3
24	-12.411	112.6	-38.470	6.8	21.740	87.7	-2.864	-4.0
24.5	-10.600	70.0	-37.283	-16.3	19.773	26.3	-2.042	-28.8
25	-10.244	26.1	-38.202	-32.0	16.115	-33.7	-2.238	-49.7
25.5	-10.312	3.8	-39.102	-43.6	11.482	-82.2	-2.445	-62.1
26	-10.454	-13.4	-40.288	-47.8	6.829	-122.7	-2.182	-74.3
26.5	-9.327	-33.6	-42.149	-42.7	2.194	-159.4	-2.080	-85.5
27	-8.344	-47.6	-40.351	-72.2	-2.142	166.1	-1.960	-98.3

Typical Board Measurements

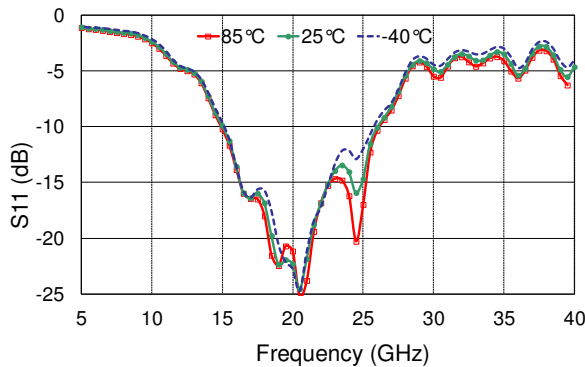
Tamb.= +25°C, Vd = +5.0V, Id = 270mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

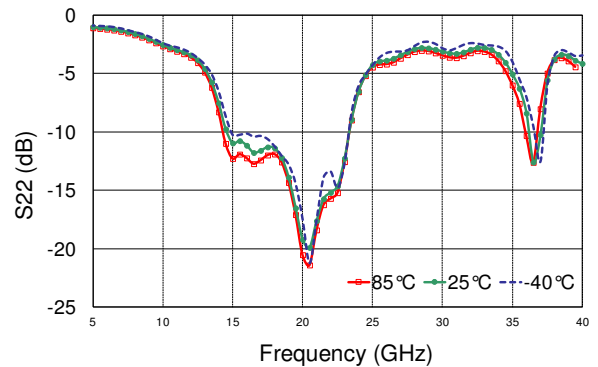
Linear Gain versus frequency in temperature



Input return loss



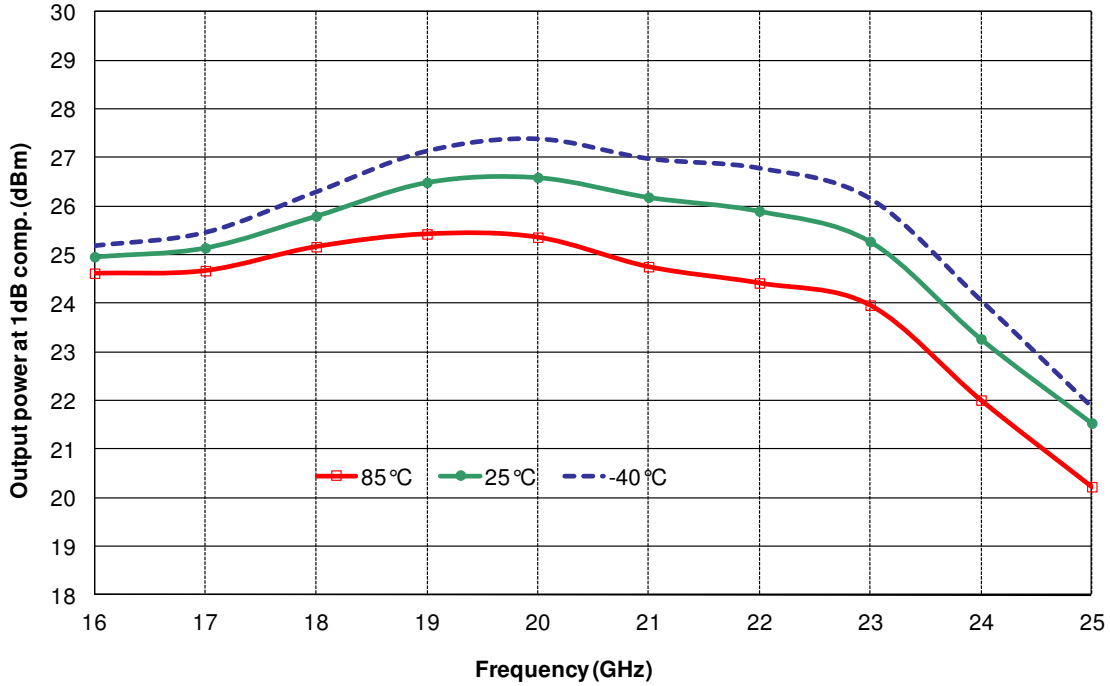
Output return loss



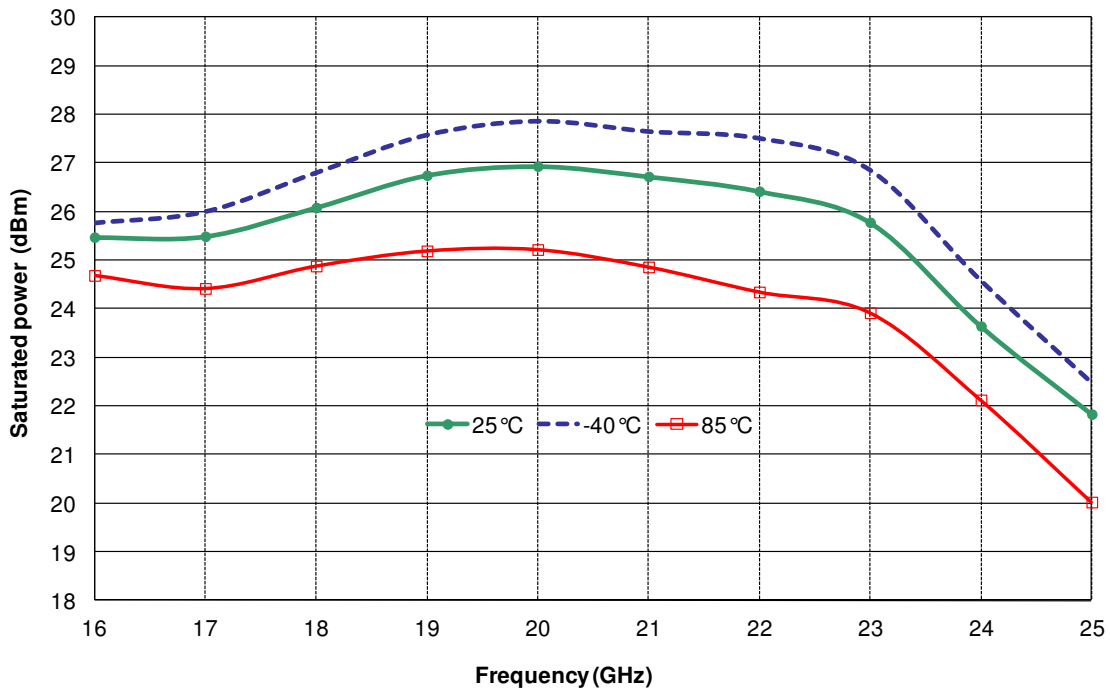
Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 270mA

Output power at 1dB compression versus temperature



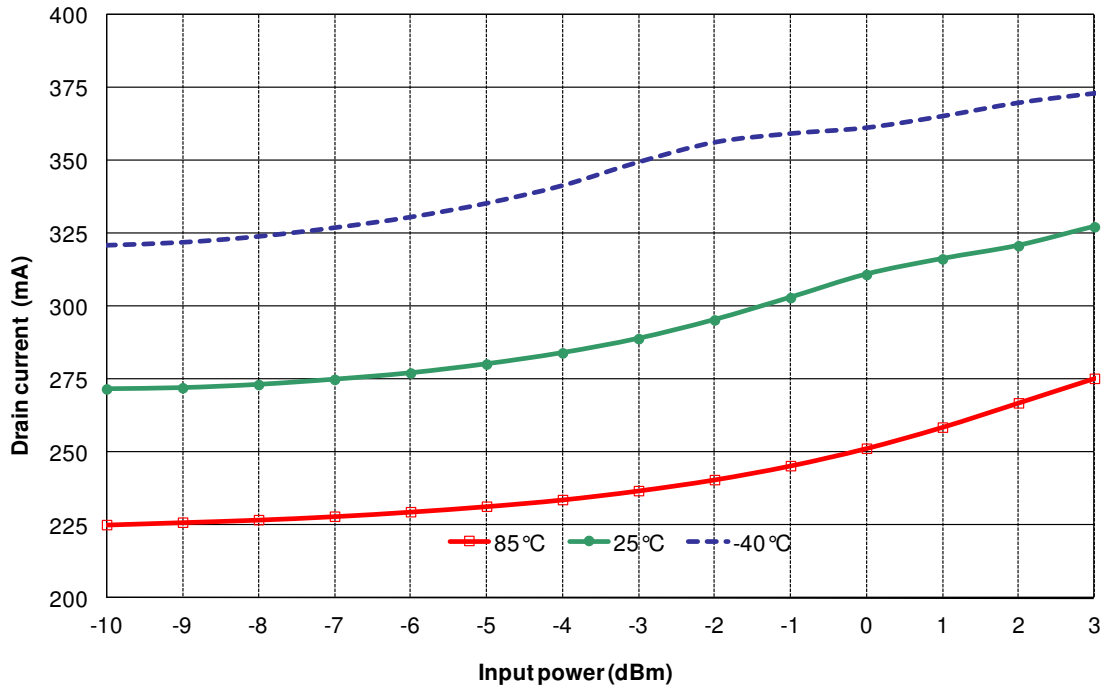
Saturated power versus temperature



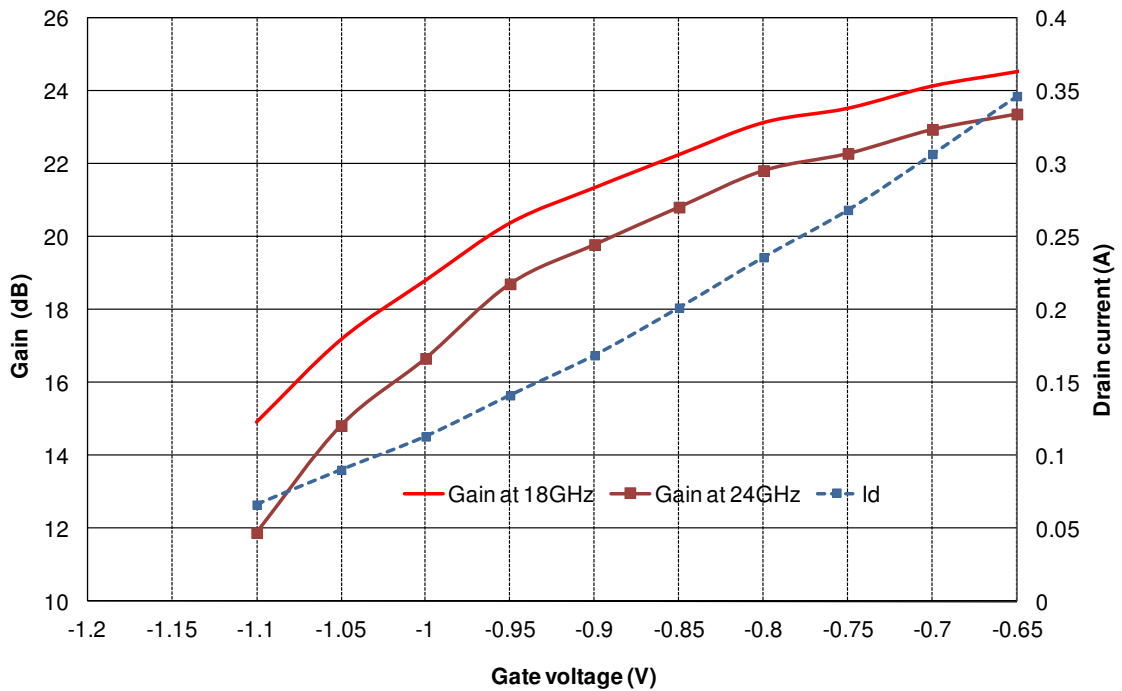
Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 270mA

Drain current versus input power & temperature at 18GHz



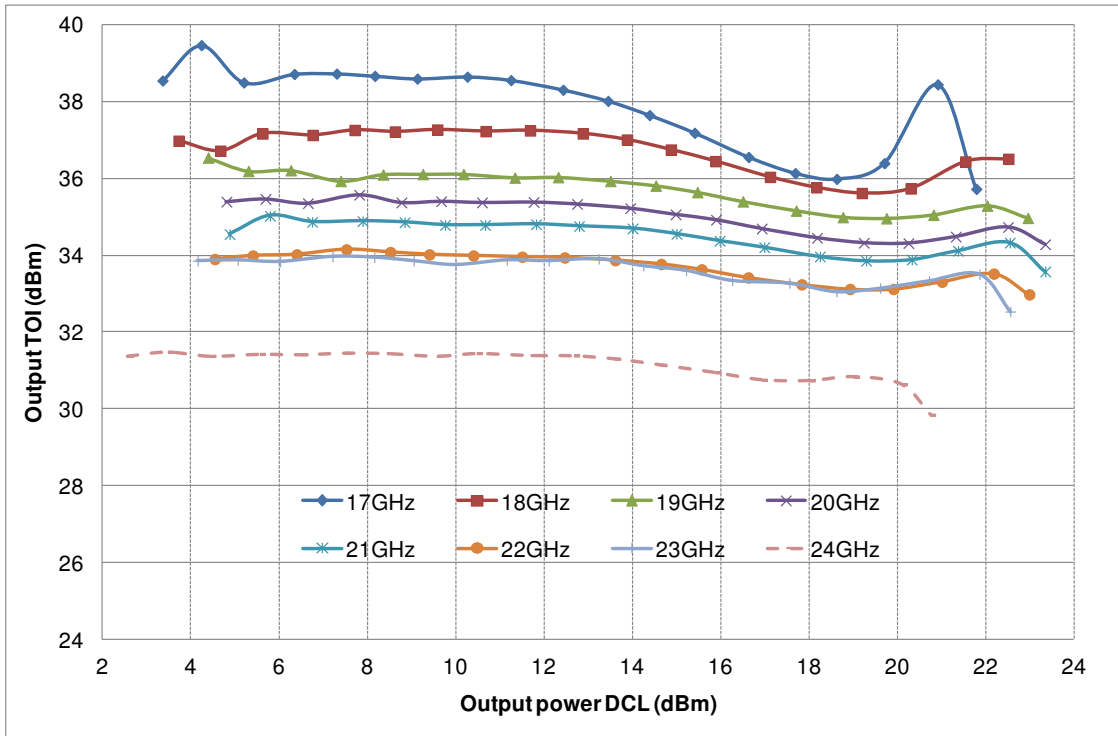
Gain & current variation versus gate voltage



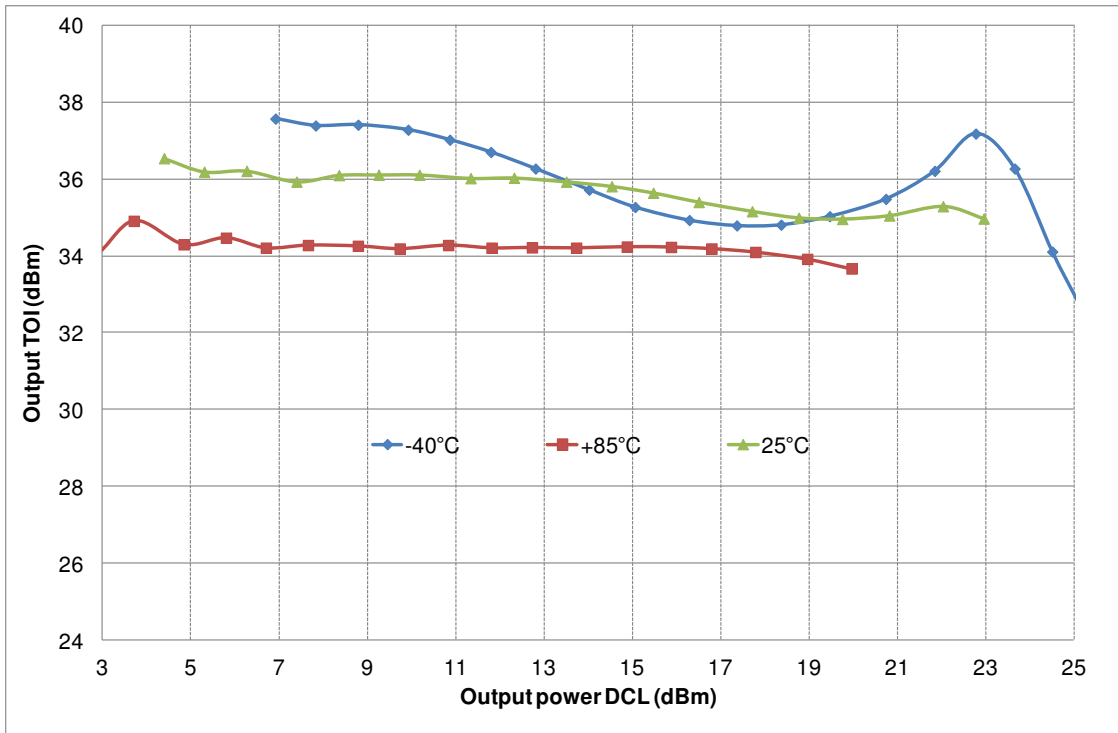
Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 270mA

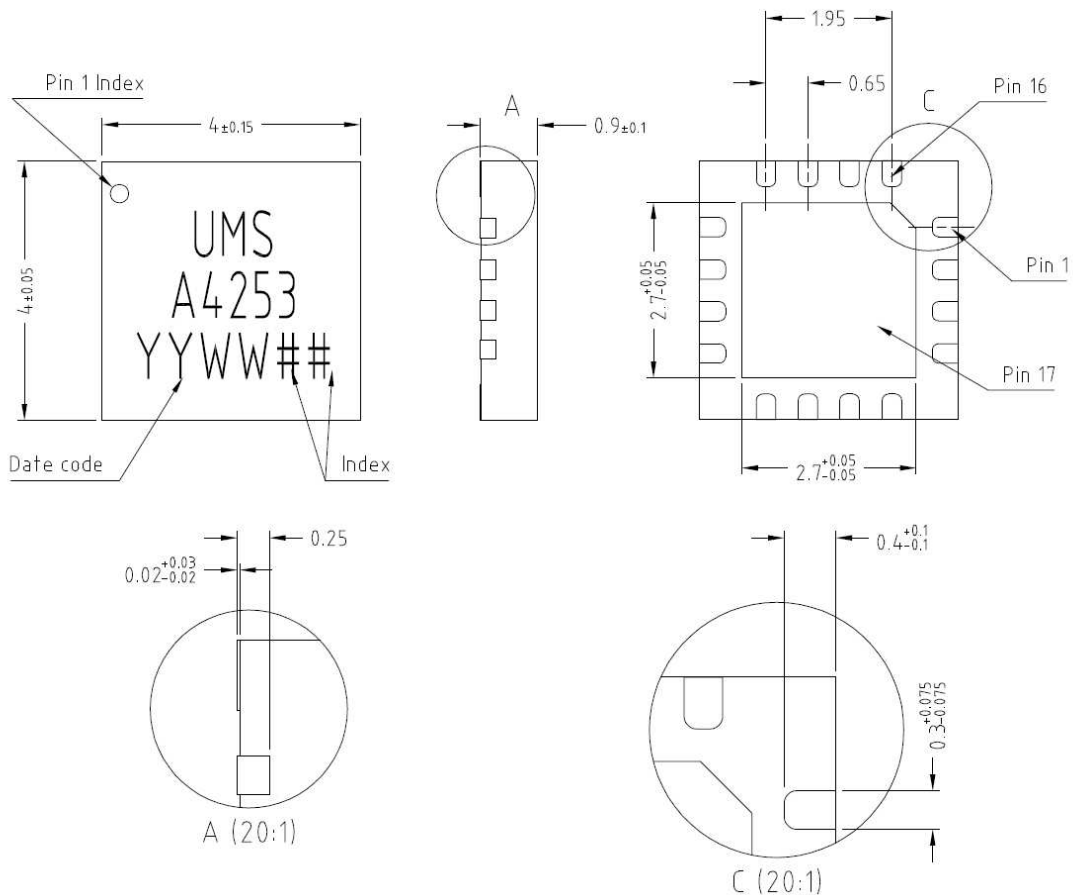
Output TOI versus Output power DCL & Frequency



Output TOI versus Output power DCL & Temperature at 19GHz



Package outline ⁽¹⁾



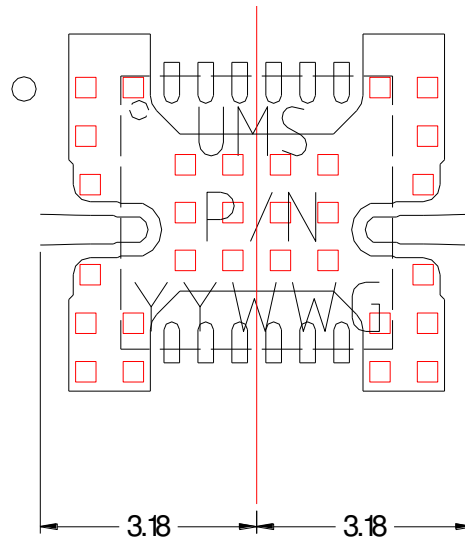
Matt tin, Lead Free	(Green)	1- NC	7- Vd4	13- NC
Units :	mm	2- Gnd ⁽²⁾	8- NC	14- Vg34
From the standard :	JEDEC MO-220	3- RF IN	9- NC	15- Nc
	(VGGD)	4- NC	10- Gnd ⁽²⁾	16- Vg12
	17- GND	5- Gnd ⁽²⁾	11- RF OUT	
		6- Vd123	12- NC	

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



ESD sensitivity

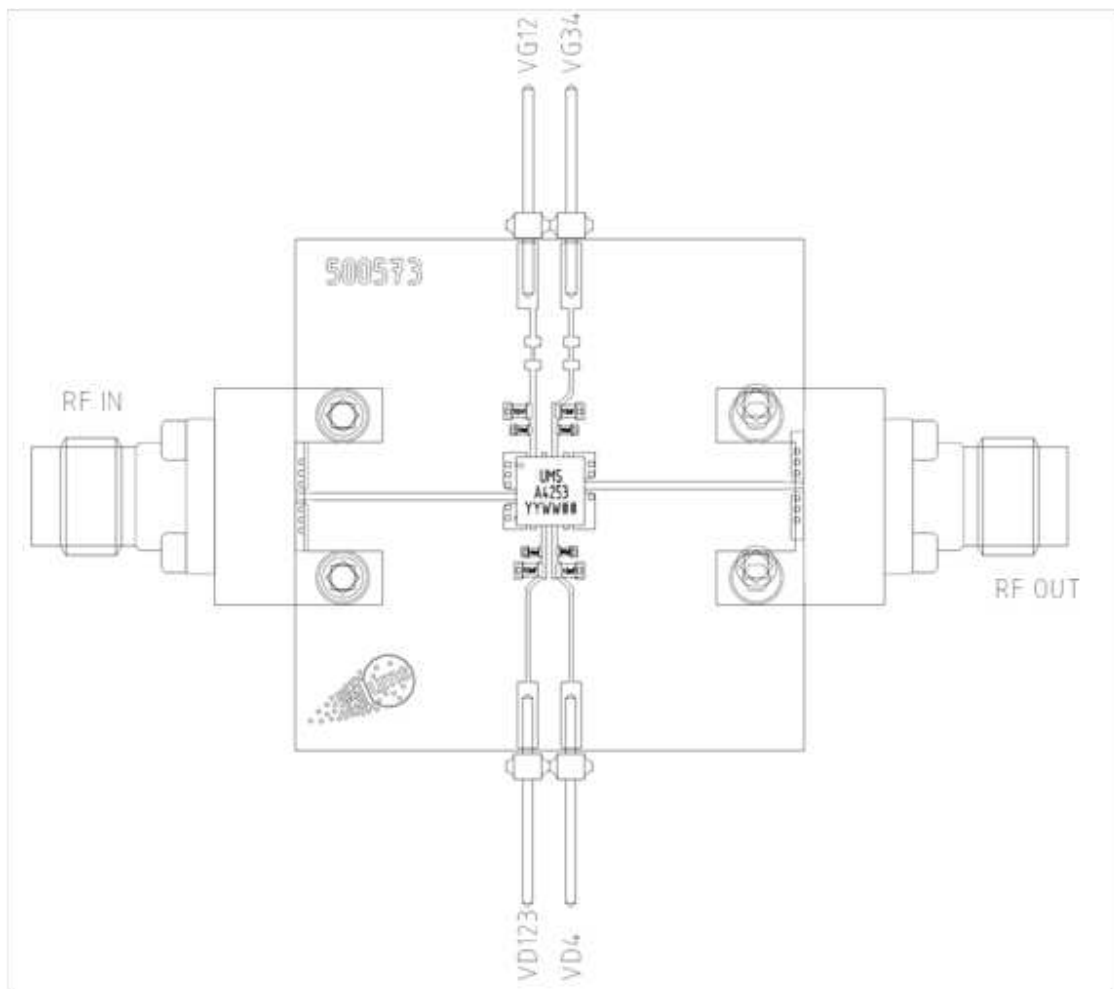
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

Package Information

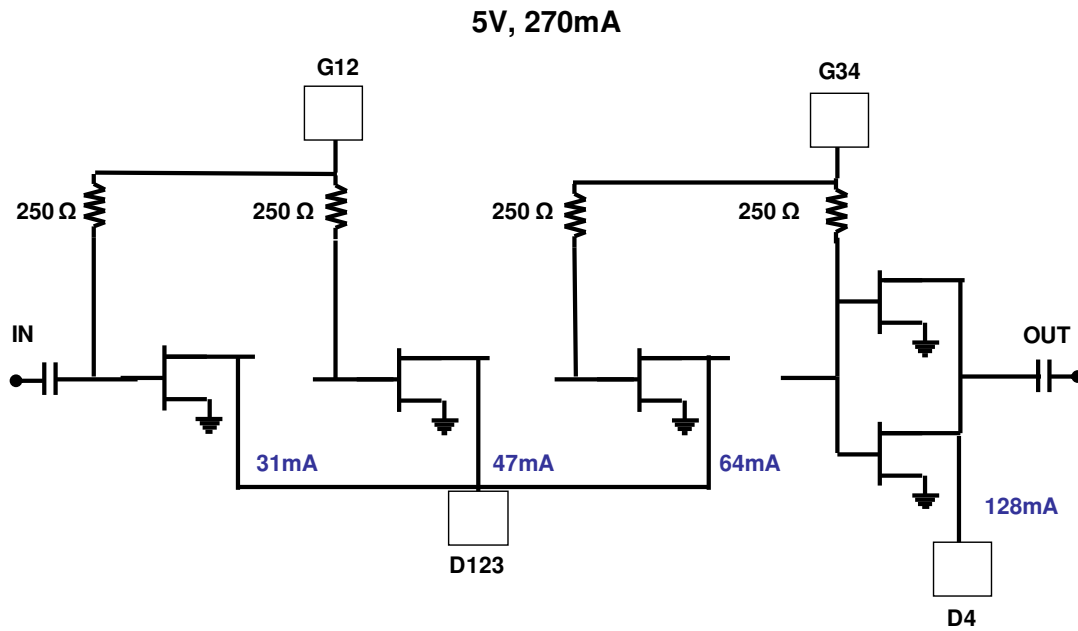
Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF $\pm 5\%$ and 10nF $\pm 10\%$ are recommended for all DC accesses.
- See application note AN0017 for details.



DC Schematic



Note

Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHA4253-QQG/XY

Stick: XY = 20

Tape & reel: XY = 21

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