5.8-17GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

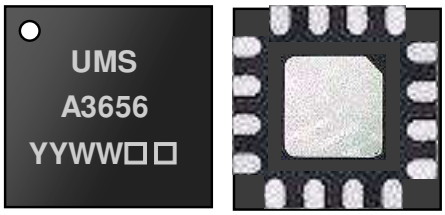
Description

The CHA3656-QAG is a two-stage self-biased wide band monolithic low noise amplifier.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

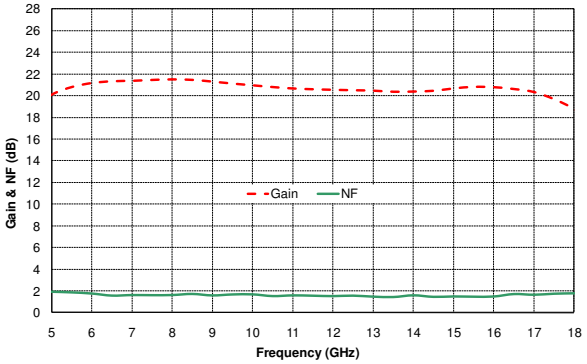
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 5.8- 17GHz
- 1.7dB noise figure
- 24dBm 3rd order intercept point
- 14dBm power at 1dB compression
- 20dB gain
- Low DC power consumption
- 16L-QFN3X3 SMD package

Gain & Noise figure (dB)



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		17.0	GHz
Gain	Linear Gain	18	20.0		dB
NF	Noise Figure		1.7	2	dB
P1dB	Output Power @1dB comp.	13.0	14.0		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +3.0V, P1, N2 = GND [1]

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		17.0	GHz
Gain	Linear Gain	18	20.0		dB
NF	Noise Figure		1.7	2	dB
RL in	Input return loss	7	8		
RL out	Output return loss	9	10		
IP3	3rd order intercept point (Pin DCL = -20 dBm)		24		dBm
P1dB	Output power at 1dB gain comp	13	14		dBm
D1, D2	Drain bias voltage		3	4	V
Id	Drain bias current		68	90	mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".
[1] Pin F1 & P2 are not connected

Absolute Maximum Ratings [1]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Pin	RF input power	10	dBm
Tj	Junction temperature [2]	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
D1	16	DC Drain voltage 2nd stage	3	V
D2	14	DC Drain voltage 1st stage	3	V
P1, N2	5, 8	DC Gate voltage	GND	
F1, P2	6, 7	DC Gate voltage	Not connected	

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

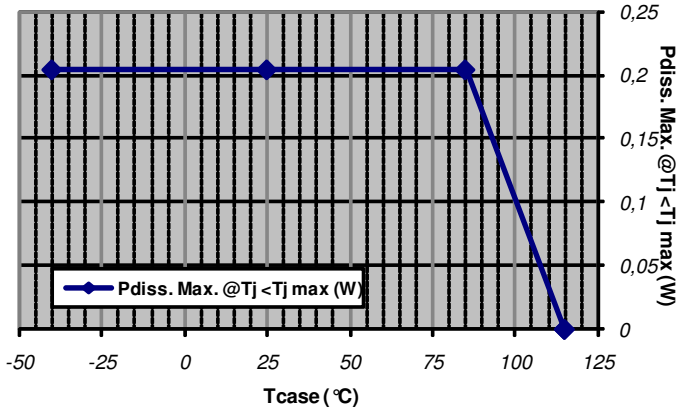
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

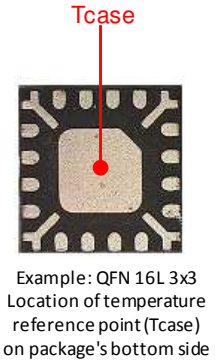
DEVICE THERMAL SPECIFICATION : CHA3656-QAG			
Recommended max. junction temperature (Tj max)	:	115	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	0,2	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	7	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<147	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Temp = +25°C, Vd1=Vd2= +3V, typical Id=68mA P1 , N2 = GND

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2.0	-0.34	-83.2	-28.42	-15.8	-72.11	176.9	-0.49	-80.8
3.0	-1.10	-141.5	1.67	-102.6	-65.37	111.5	-3.57	-127.6
4.0	-5.41	117.5	15.84	139.3	-55.13	-159.3	-7.37	-141.7
5.0	-9.50	-29.6	20.10	33.8	-44.56	123.6	-8.94	-159.4
6.0	-8.96	-91.0	21.15	-44.4	-40.55	68.1	-10.28	-179.7
7.0	-8.15	-123.8	21.35	-107.9	-38.41	20.1	-11.23	151.6
8.0	-7.79	-153.6	21.48	-163.3	-37.55	-22.4	-12.88	112.9
9.0	-7.65	175.0	21.27	145.1	-36.87	-57.8	-15.39	67.6
10.0	-8.40	142.7	20.93	98.1	-36.09	-93.6	-17.45	19.0
11.0	-9.73	110.8	20.64	54.2	-35.53	-130.8	-18.48	-25.3
12.0	-11.45	78.9	20.52	11.7	-35.31	-168.0	-18.95	-58.1
13.0	-12.57	46.2	20.44	-31.3	-35.28	158.3	-20.78	-73.1
14.0	-13.31	8.3	20.36	-72.7	-35.42	118.2	-18.76	-81.3
15.0	-12.31	-31.4	20.65	-115.4	-36.12	81.2	-18.03	-98.3
16.0	-9.92	-123.1	20.76	148.1	-38.53	-10.4	-19.36	-166.6
17.0	-7.86	-171.8	20.31	93.5	-43.59	-46.7	-25.75	-105.7
18.0	-6.76	133.6	18.75	37.2	-48.33	6.2	-13.10	-107.4
19.0	-7.81	74.4	15.93	-16.0	-40.68	-7.4	-8.06	-144.6
20.0	-9.90	-166.9	12.65	-60.6	-38.83	-47.3	-6.55	2.4
21.0	-10.68	125.5	9.55	-101.3	-37.64	-90.5	-5.33	-24.4
22.0	-9.37	63.4	6.39	-138.7	-39.46	-128.6	-4.59	-50.6
23.0	-7.54	17.3	3.76	-169.4	-42.41	-165.0	-4.63	-74.5
24.0	-5.98	-21.0	1.63	156.4	-43.57	158.7	-4.38	-94.4
25.0	-5.00	-54.6	-0.50	126.5	-41.11	111.1	-4.12	-117.2
26.0	-4.48	-86.2	-1.76	96.7	-40.00	52.8	-4.23	-140.4
27.0	-4.57	-118.6	-2.01	63.3	-36.45	-3.5	-4.58	-164.0
28.0	-6.02	-152.7	-0.94	17.2	-32.52	-46.6	-5.05	173.8
29.0	-10.14	-156.2	-1.77	-61.9	-30.56	-107.8	-4.94	148.9
30.0	-6.28	-170.9	-10.00	-126.8	-33.31	-160.3	-5.45	117.7
31.0	-5.52	155.7	-18.14	-161.2	-35.30	-174.5	-6.25	88.5
32.0	-5.71	120.6	-23.23	-171.6	-34.60	165.3	-6.30	58.2
33.0	-6.71	75.3	-22.53	158.7	-29.95	130.6	-5.33	23.1
34.0	-12.87	-17.2	-21.95	73.3	-28.76	46.8	-5.25	-17.5
35.0	-8.31	149.2	-27.40	-31.7	-35.96	-32.7	-5.28	-52.8
36.0	-5.11	75.1	-34.16	-84.5	-38.00	-63.9	-5.40	-84.6
37.0	-7.25	28.9	-40.00	55.5	-38.04	72.4	-5.30	-109.7
38.0	-5.48	-17.3	-27.67	-102.0	-30.98	-111.3	-4.37	-136.1
39.0	-6.02	-79.5	-28.55	-154.0	-33.34	-173.6	-3.62	-162.5
40.0	-6.43	-133.6	-30.94	163.3	-35.78	133.5	-2.91	173.2

Refer to the “definition of the Sij reference planes” section below.

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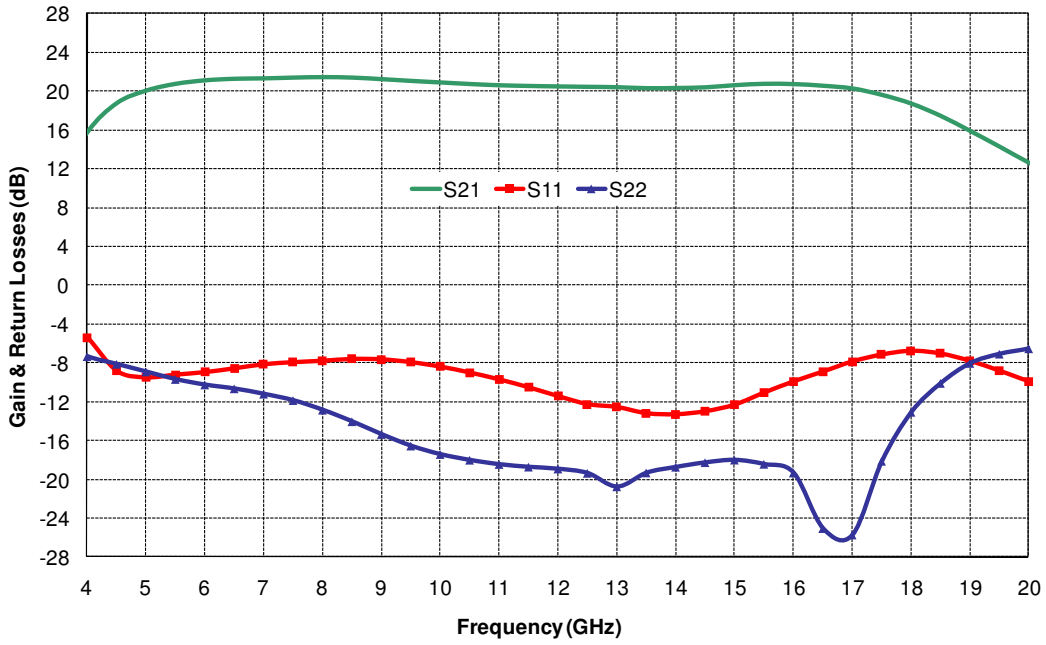
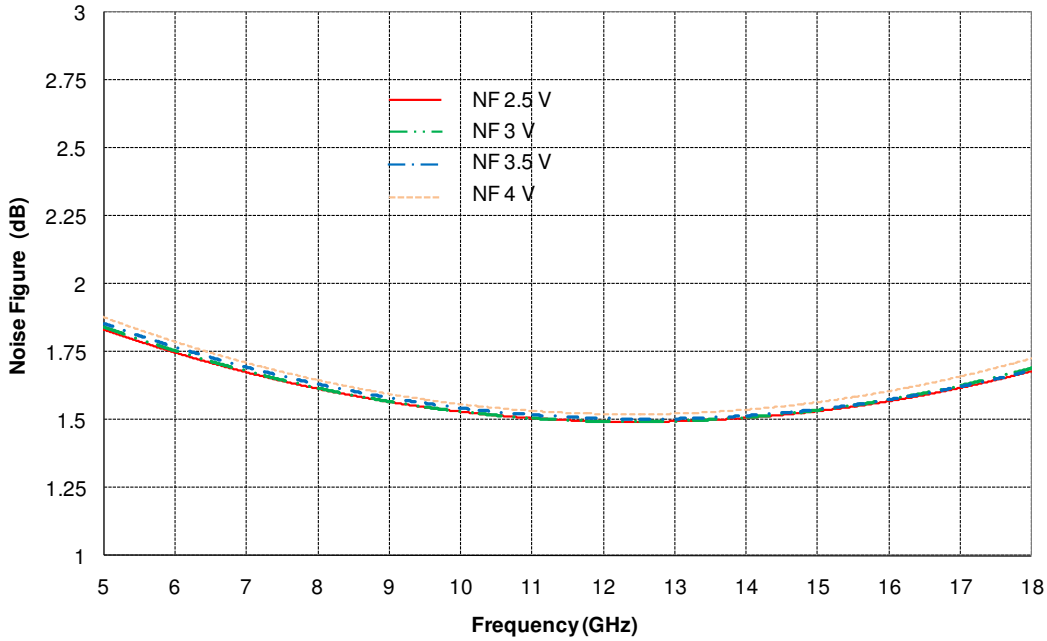
Typical Board Measurements

Tamb.= +25°C, Vd = +3.0V, Id = 68mA, P1 = N2 = GND
Measurement in the package access planes

Linear Gain & Return loss versus frequency



Noise figure versus frequency & Vd



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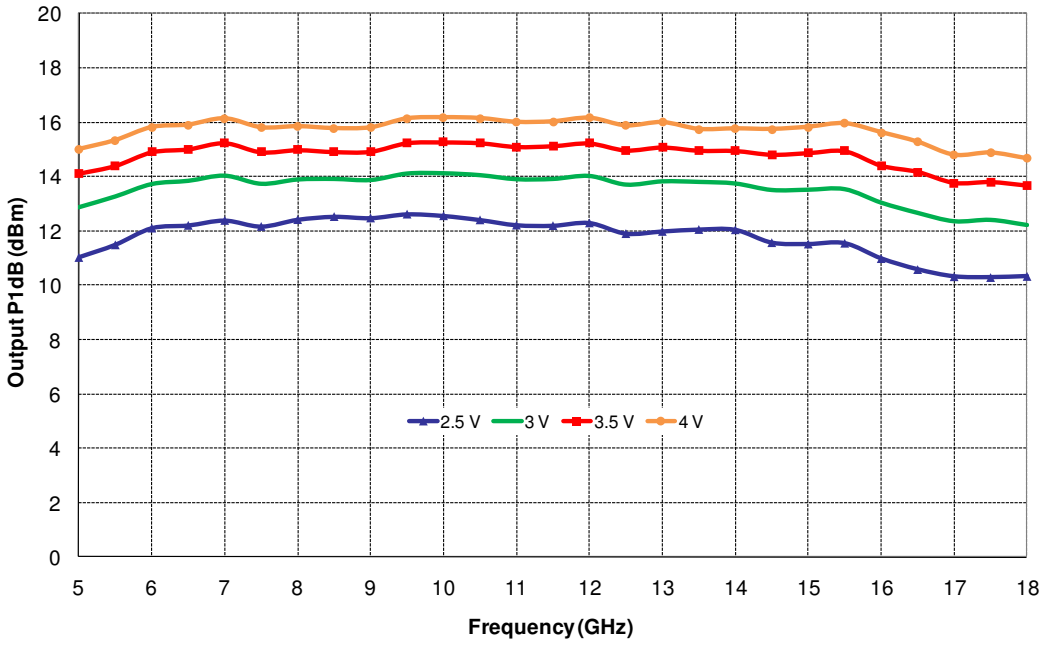
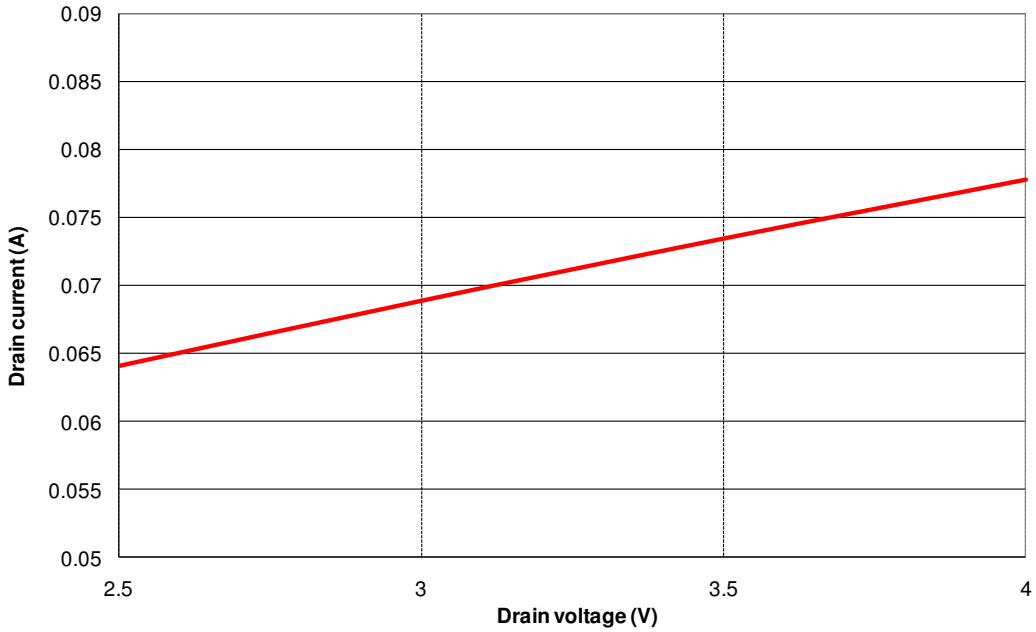
Typical Board Measurements

Tamb.= +25°C, Vd = +3.0V, Id = 68mA, P1 = N2 = GND
Measurement in the package access planes

Output power at 1dB compression versus frequency & Vd



Drain current versus Vd



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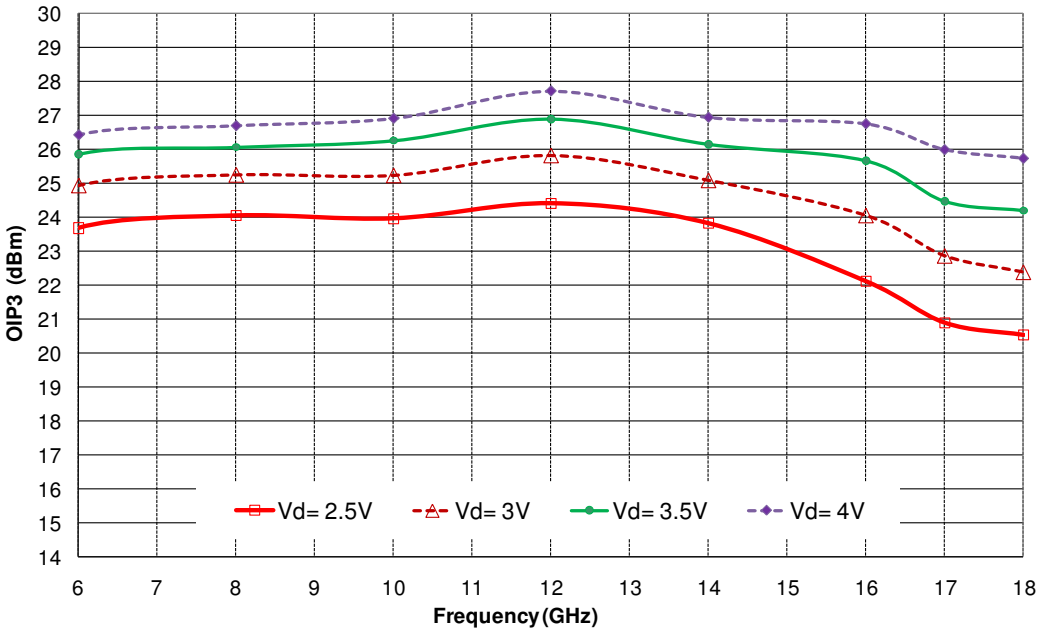
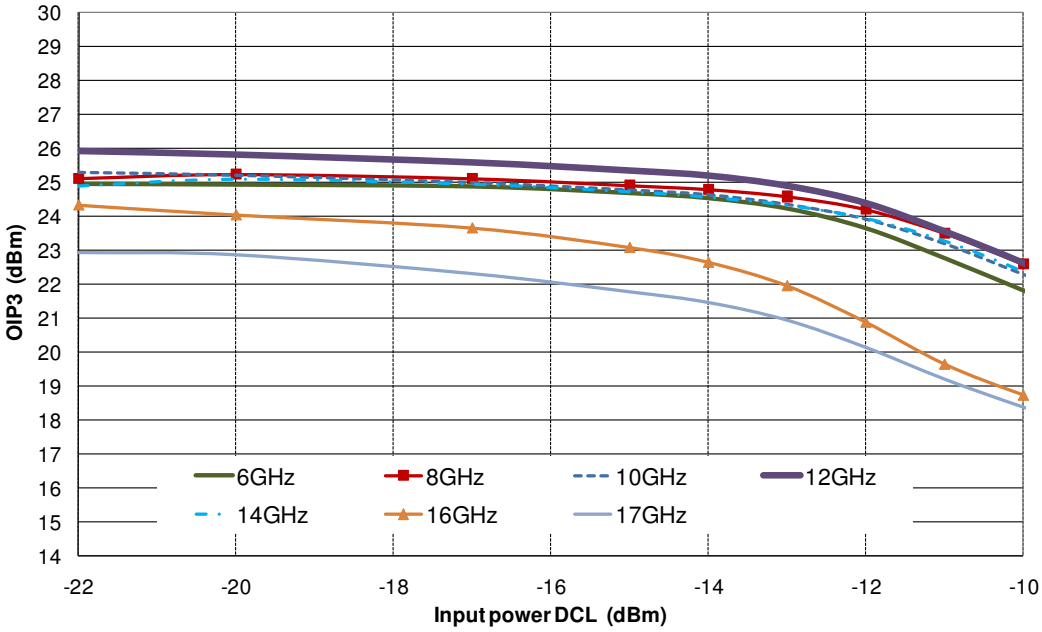
Typical Board Measurements

Tamb.= +25°C, Vd = +3.0V, Id = 68mA, P1 = N2 = GND
Measurement in the package access planes

Output IP3 versus frequency & Vd
Pin (DCL) = -20dBm



Output IP3 versus Pin & frequency
Vd = 3V



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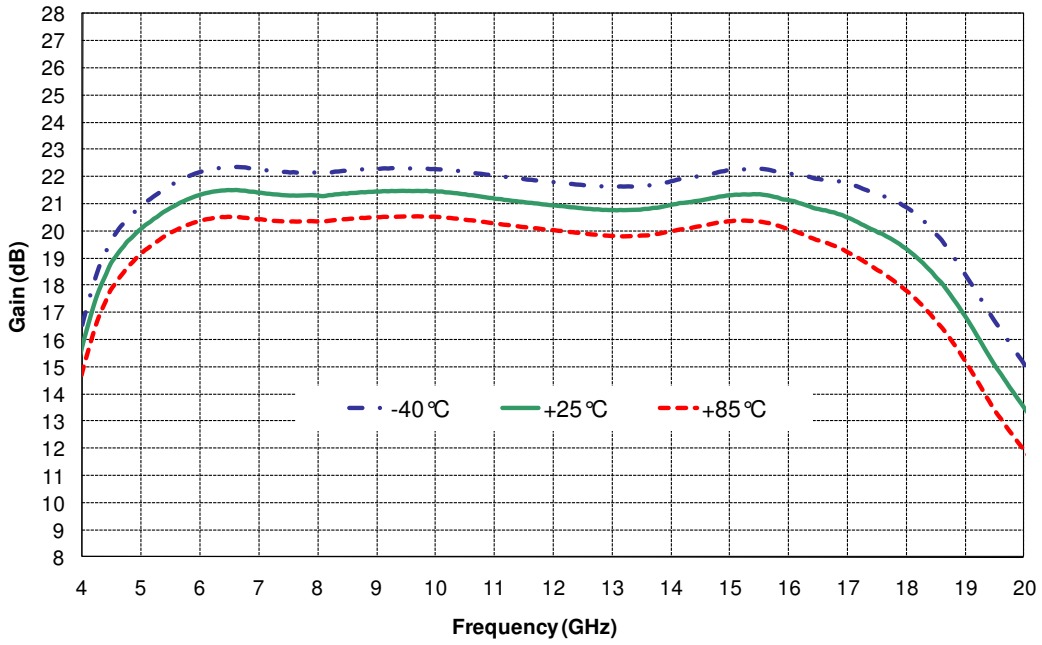
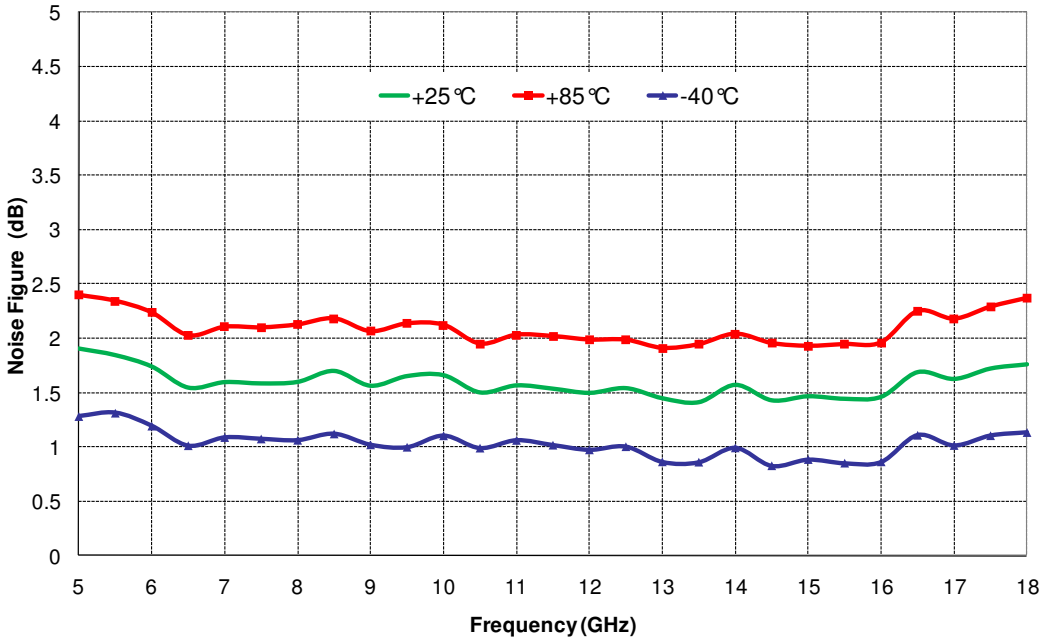
Typical Board Measurements

Tamb.= +25°C, Vd = +3.0V, Id = 68mA, P1 = N2 = GND
Measurement in the package access planes

Linear gain versus frequency & temperature



Noise figure versus frequency & temperature



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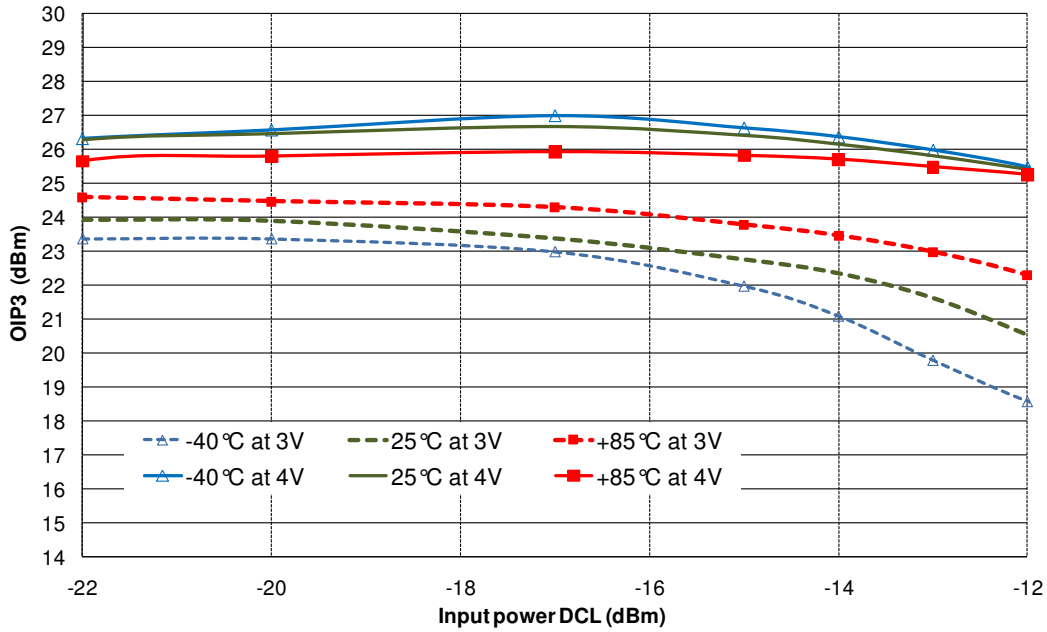
Typical Board Measurements

Tamb.= +25°C, Vd = +3.0V, Id = 68mA, P1 = N2 = GND
Measurement in the package access planes

Output IP3 versus Pin, temperature & Vd
Frequency = 16GHz



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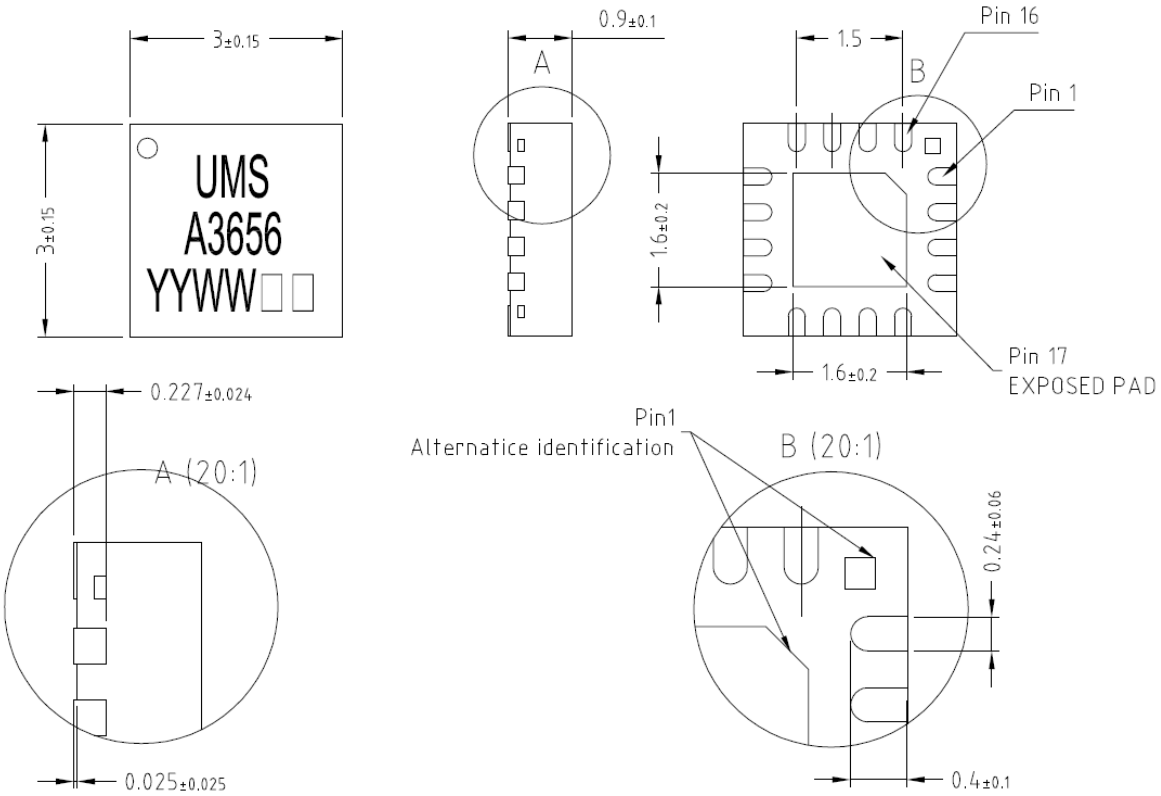
Package outline (1)



Matt tin, Lead Free	(Green)	1- Nc	7- P2	13- Nc
Units :	mm	2- Gnd(2)	8- N2	14- D2
From the standard :	JEDEC MO-220	3- RF IN	9- Gnd(2)	15- Gnd(2)
	(VGGD)	4- Gnd(2)	10- RF OUT	16- D1
17-	GND	5- P1	11- Gnd(2)	
		6- F1	12- Nc	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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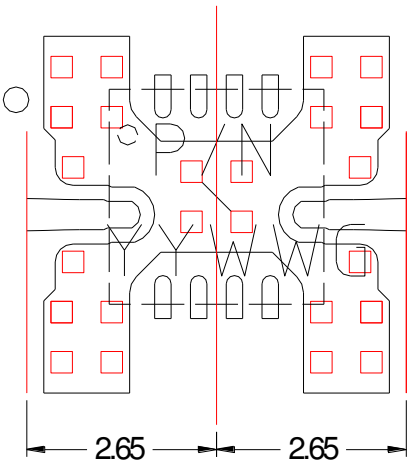
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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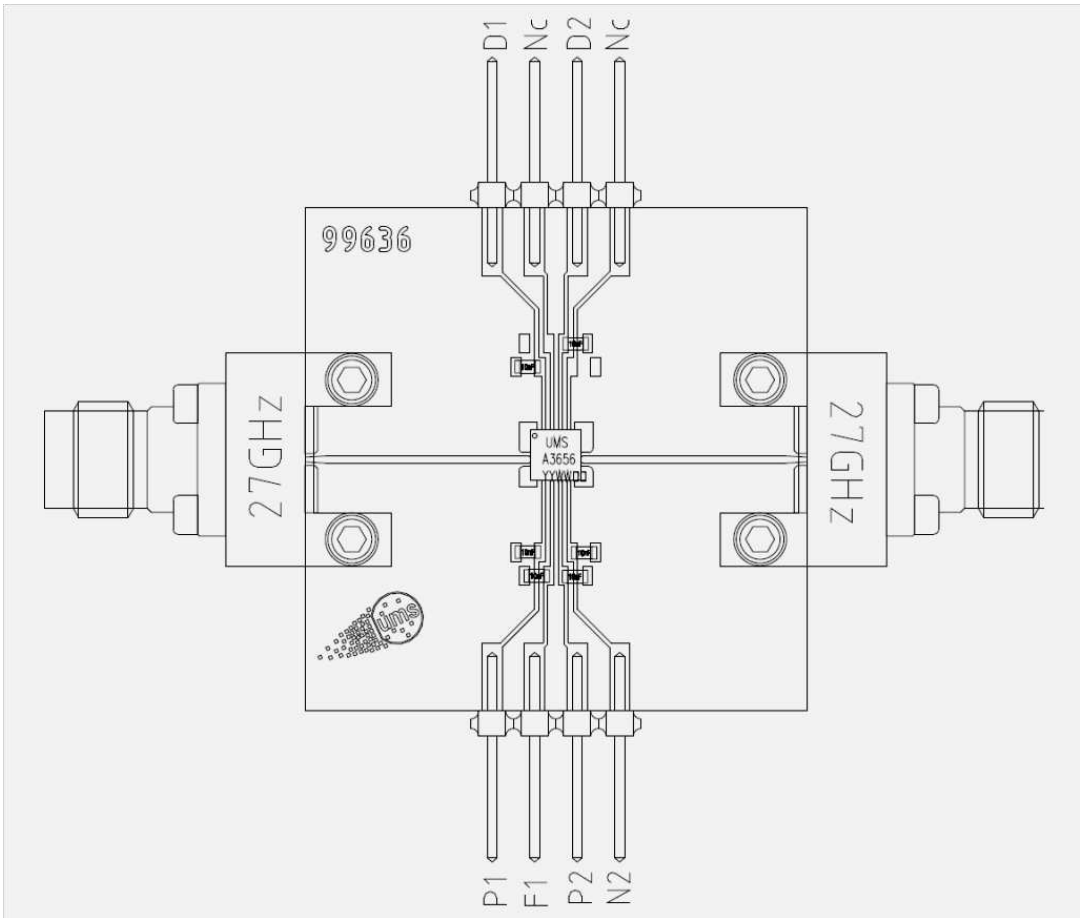
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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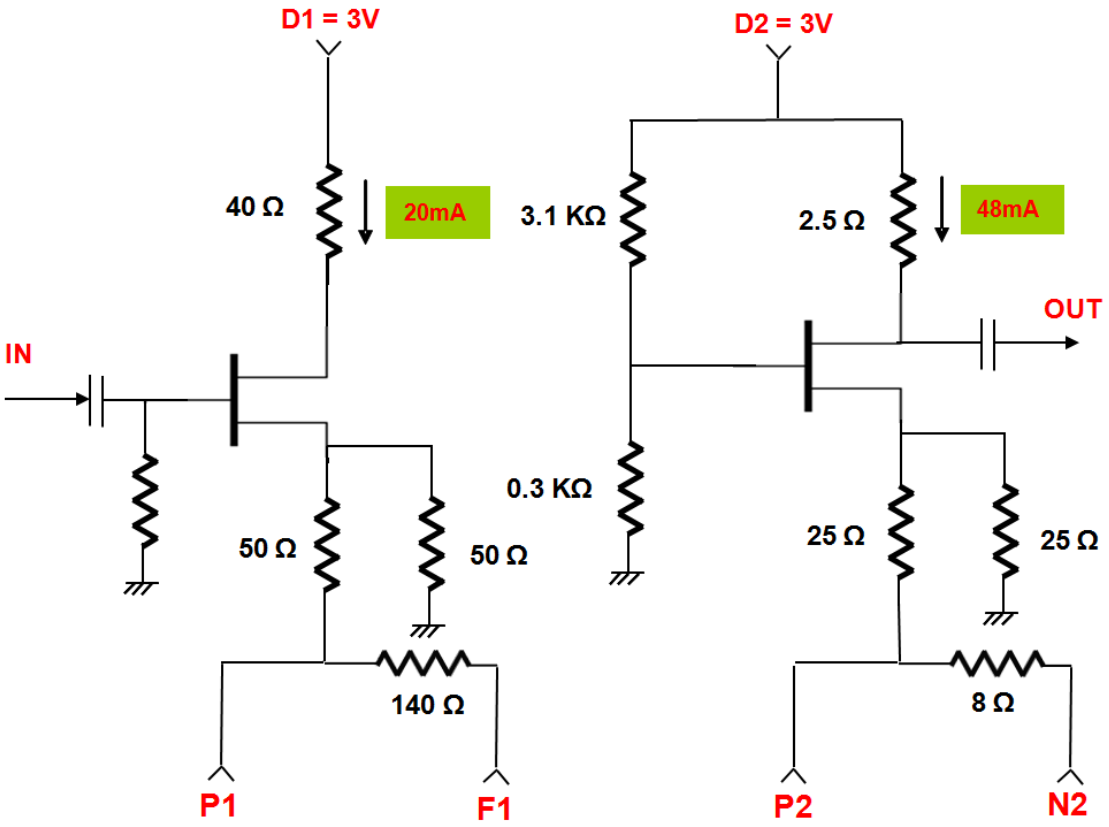
DC Schematic

LNA: 3V, 68mA



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 package:	CHA3656-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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