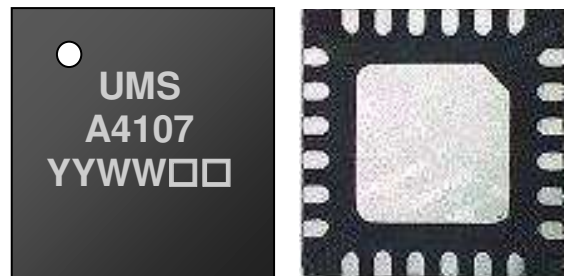


C-band Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

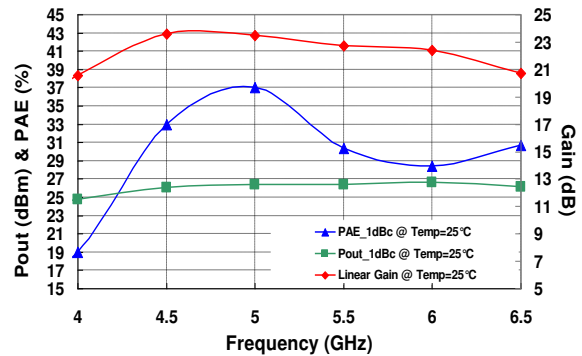
Description

The CHA4107-QDG is a monolithic two-stage GaAs medium power amplifier designed for C-band applications. The MPA provides typically 25.5 dBm output power associated to 30% power added efficiency at 1dB gain compression. It is supplied in RoHS compliant SMD package.



Main Features

- Frequency band: 4.5-6.5 GHz
- Output power: 25.5 dBm @ 1dBcomp
- Linear gain: 22.5 dB
- High PAE: 30% @ 1dBcomp
- Quiescent bias point: $V_d=8V$, $I_d=120mA$
- 24L-QFN4x4
- MSL3



Main Characteristics

$T_{amb} = 25^{\circ}C$, $V_d = 8V$, I_d (Quiescent) = 120mA, Drain Pulse width= 50 μs , Duty cycle = 10%

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|----------------------------------------|-----|------|-----|------|
| Fop | Operating frequency range | 4.5 | | 6.5 | GHz |
| PAE_P-1dB | Power added efficiency @1dBcomp & 25°C | | 30 | | % |
| P-1dB | Output power @ 1dBcomp @ 25°C | | 25.5 | | dBm |

Electrical Characteristics

Tamb = +25 °C,

Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50µs, Duty cycle = 10%

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|-----------------------------------------|-----|------|-----|------|
| Fop | Operating frequency | 4.5 | | 6.5 | GHz |
| G | Small signal gain | | 22.5 | | dB |
| RLin | Input Return Loss | | 14 | 8 | dB |
| RLout | Output Return Loss | | 10 | 8 | dB |
| P _{-1dB} | Output power @ 1dBcomp | | 25.5 | | dBm |
| PAE _{-1dB} | Power Added Efficiency @ 1dBcomp | | 30 | | % |
| Id _{-1dB} | Supply drain current @ 1dBcomp | | 145 | | mA |
| P _{-3dB} | Output power @ 3dBcomp | | 26 | | dBm |
| PAE _{-3dB} | Power Added Efficiency @ 3dBcomp | | 36 | | % |
| Id _{-3dB} | Supply drain current @ 3dBcomp | | 160 | | mA |
| Vd1, Vd2 | Drain supply voltage | | 8 | | V |
| Id | Supply quiescent current ⁽¹⁾ | | 120 | | mA |
| Vg | Gate supply voltage | | -0.8 | | V |

⁽¹⁾ Parameter can be adjusted by tuning of Vg.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25 °C

| Symbol | Parameter | Values | Unit |
|-------------------|----------------------------------|-------------|------|
| Cmp | Compression level ⁽²⁾ | 6 | dB |
| Vd | Supply voltage ⁽³⁾ | 9.5 | V |
| Id | Supply quiescent current | 170 | mA |
| Id _{sat} | Supply current in saturation | 200 | mA |
| Vg | Supply voltage | -0.6 | V |
| Tj | Maximum junction temperature | 175 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |
| Top | Operating temperature range | -40 to +85 | °C |

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ For higher compression the level limit can be increased by decreasing the voltage Vd using the rate 0.5V/dB of gain compression.

⁽³⁾ Without RF input power.

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

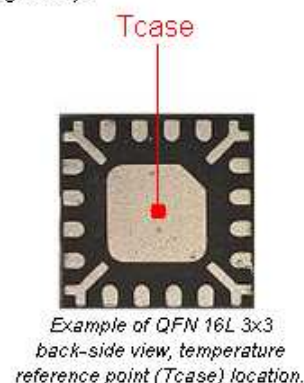
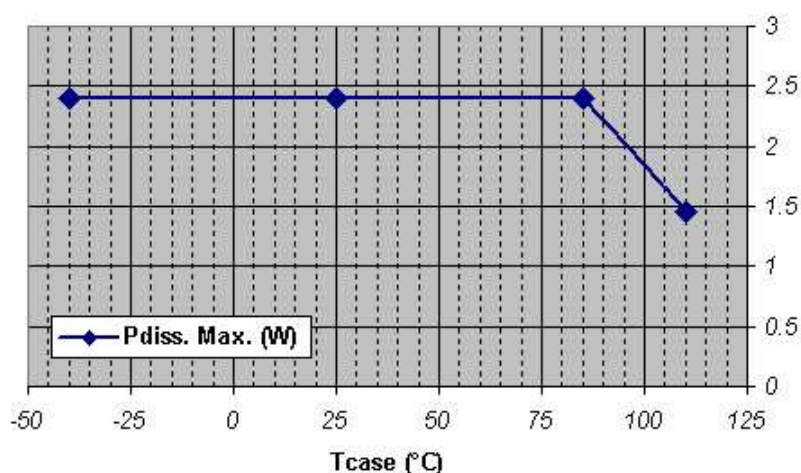
A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max}$) in order to guarantee the nominal device life time (MTTF).

| DEVICE THERMAL SPECIFICATION : CHA4107-QDG | |
|-------------------------------------------------------------|------------|
| Recommended max. junction temperature (T_j max) | : 148 °C |
| Junction temperature absolute maximum rating | : 175 °C |
| Max. continuous dissipated power @ $T_{case} = 85$ °C | : 2.4 W |
| => P_{diss} derating above $T_{case}^{(1)} = 85$ °C | : 38 mW/°C |
| Junction-Case thermal resistance ($R_{th J-C}^{(2)}$) | : <26 °C/W |
| Min. package back side operating temperature ⁽³⁾ | : -40 °C |
| Max. package back side operating temperature ⁽³⁾ | : 85 °C |
| Min. storage temperature | : -55 °C |
| Max. storage temperature | : 150 °C |

(1) Derating at junction temperature constant = T_j max

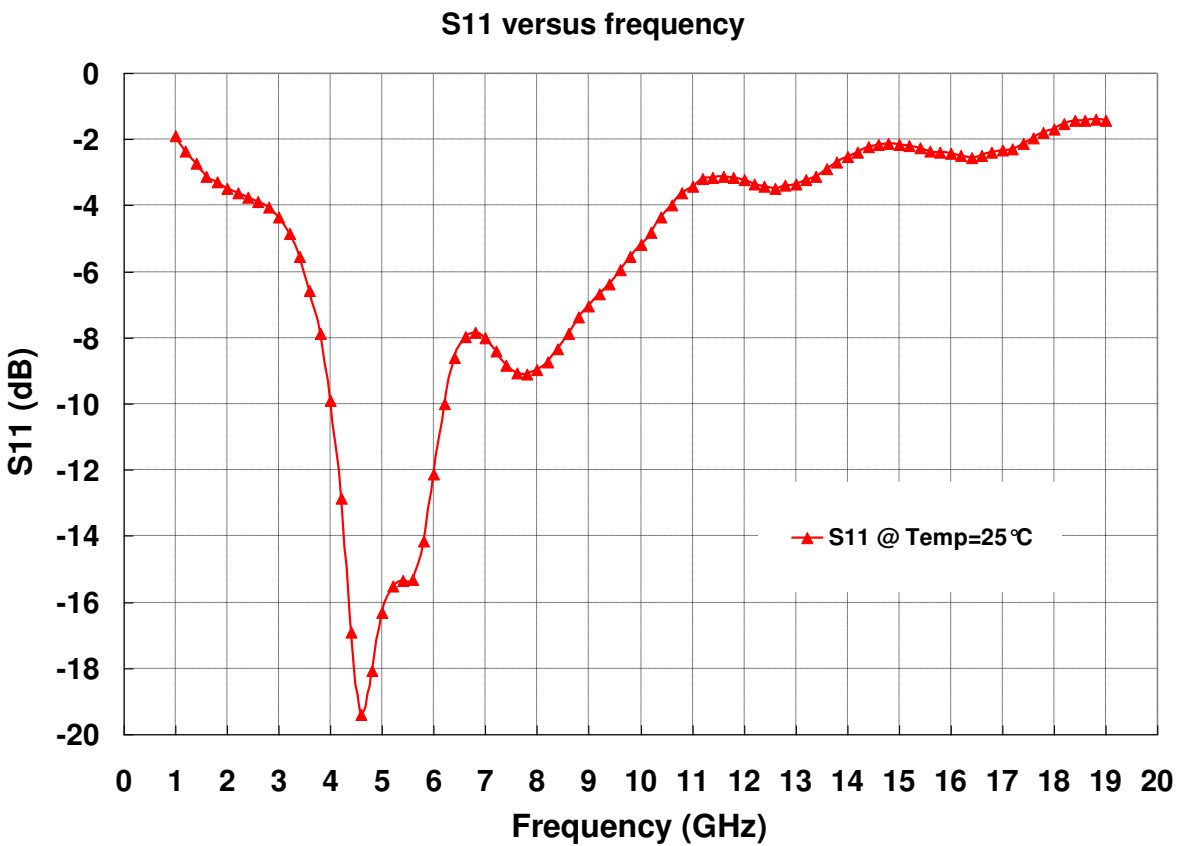
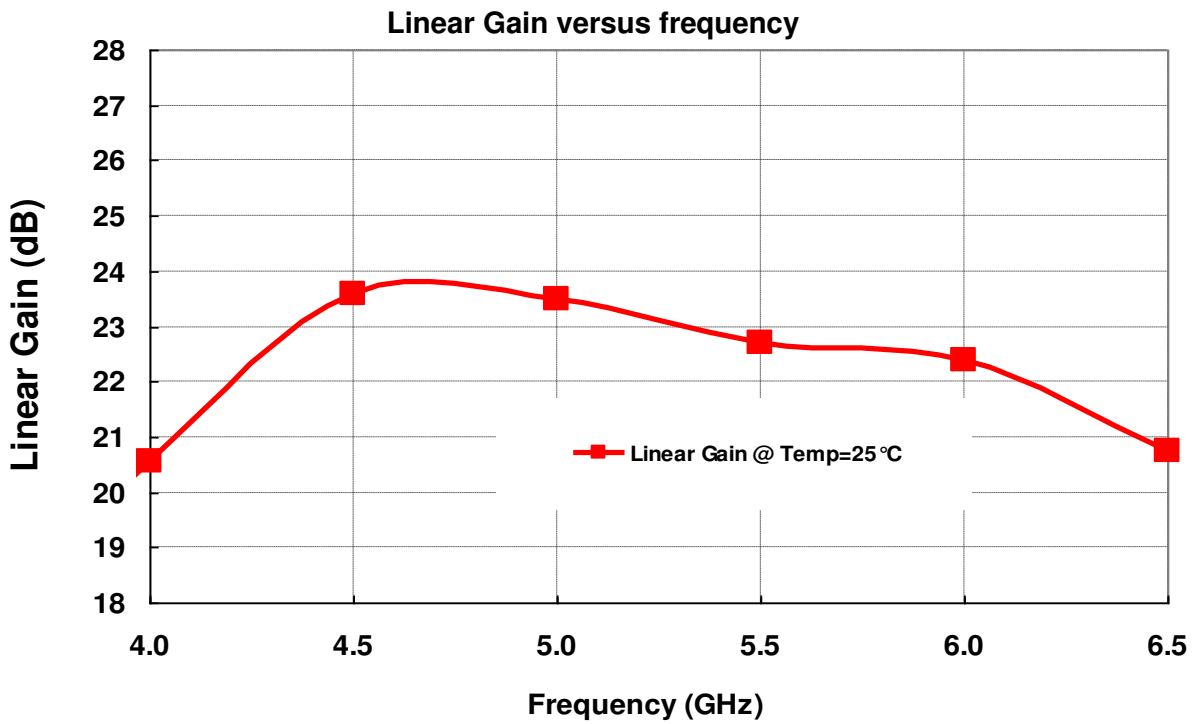
(2) $R_{th J-C}$ is calculated for a worst case where the **hottest junction** of the MMIC is considered.

(3) T_{case} = Package back side temperature measured under the die-attach-pad (see the drawing below).



Typical Board Measurements

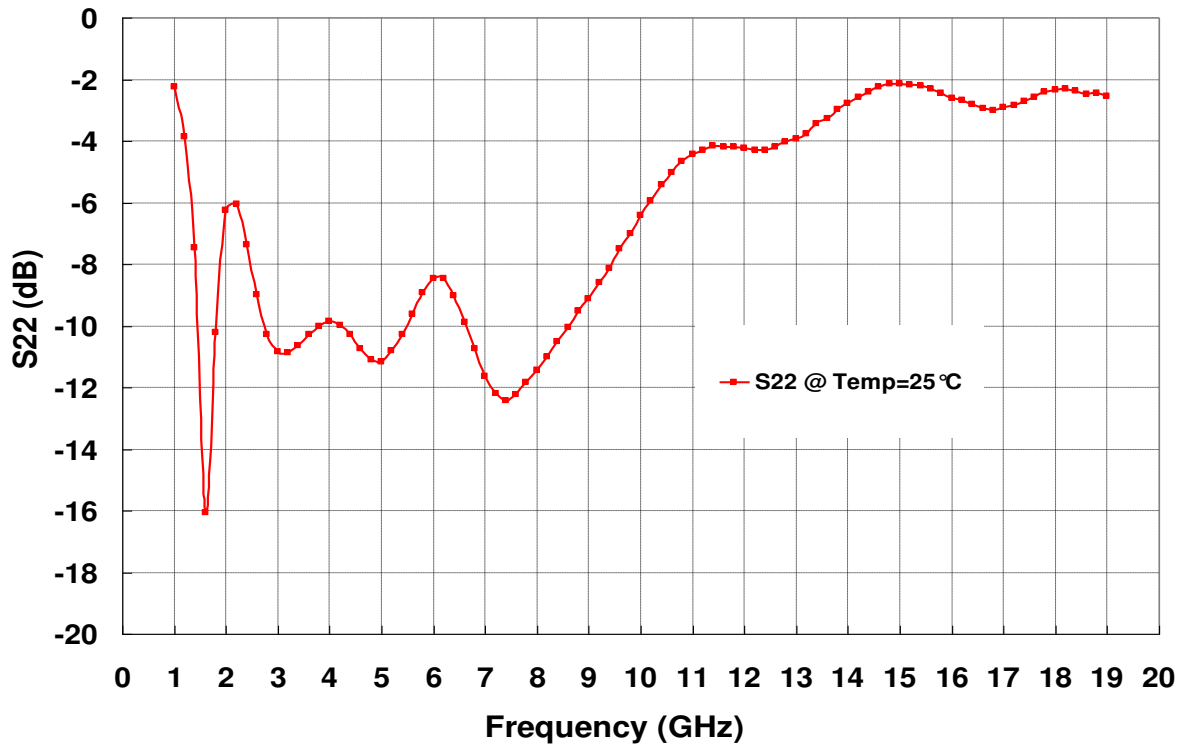
Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50µs, Duty cycle = 10%



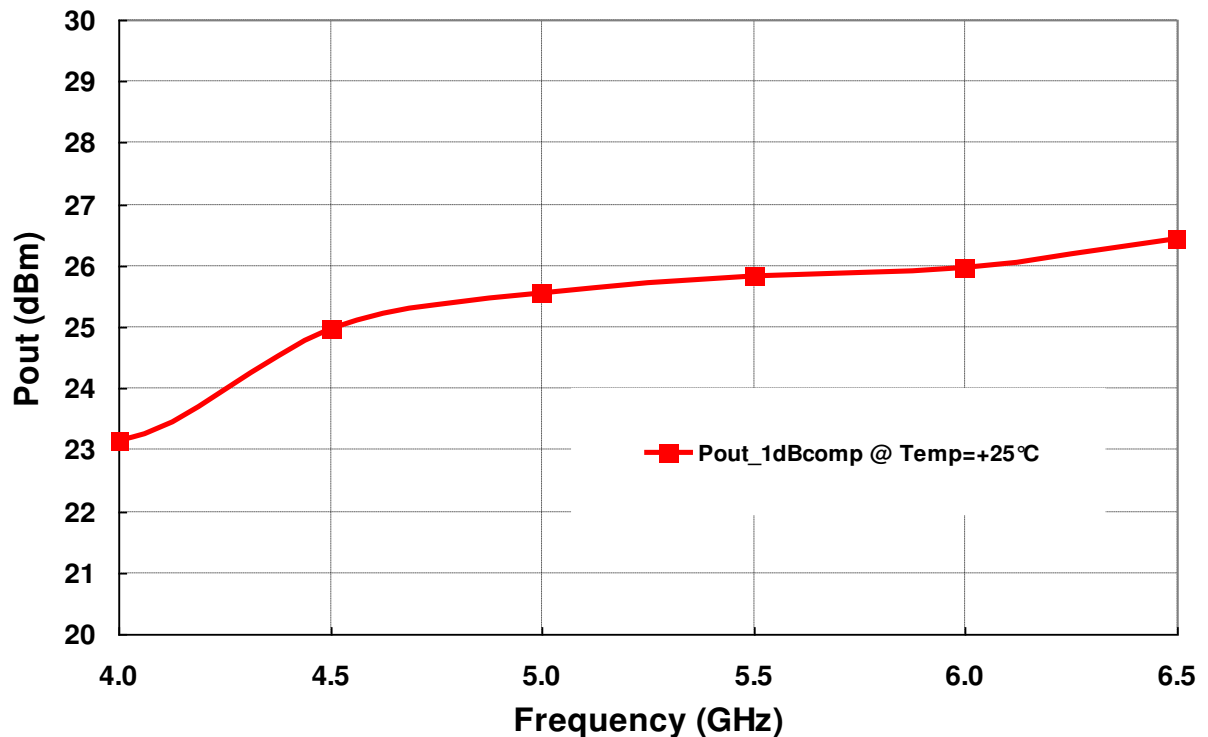
Typical on board Measurements

Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50µs, Duty cycle = 10%

S22 versus frequency



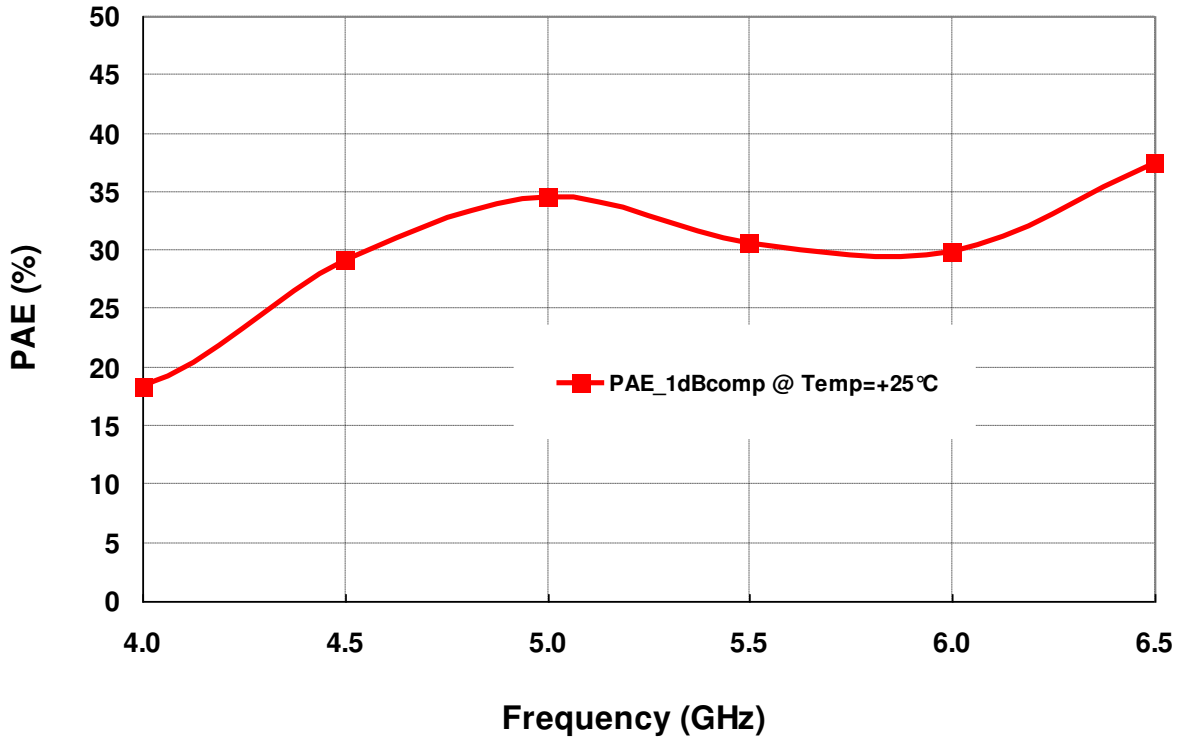
Output power @ 1dBcomp versus frequency



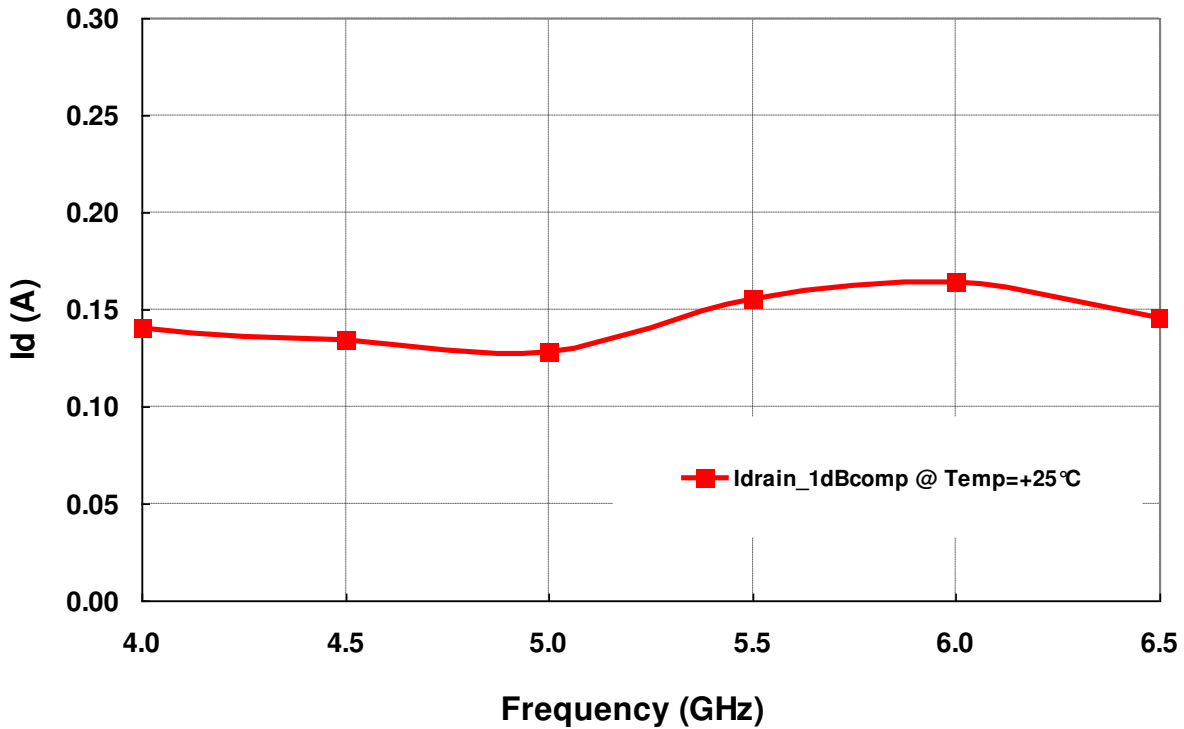
Typical on board Measurements

Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50μs, Duty cycle = 10%

Power added efficiency @ 1dBcomp versus frequency

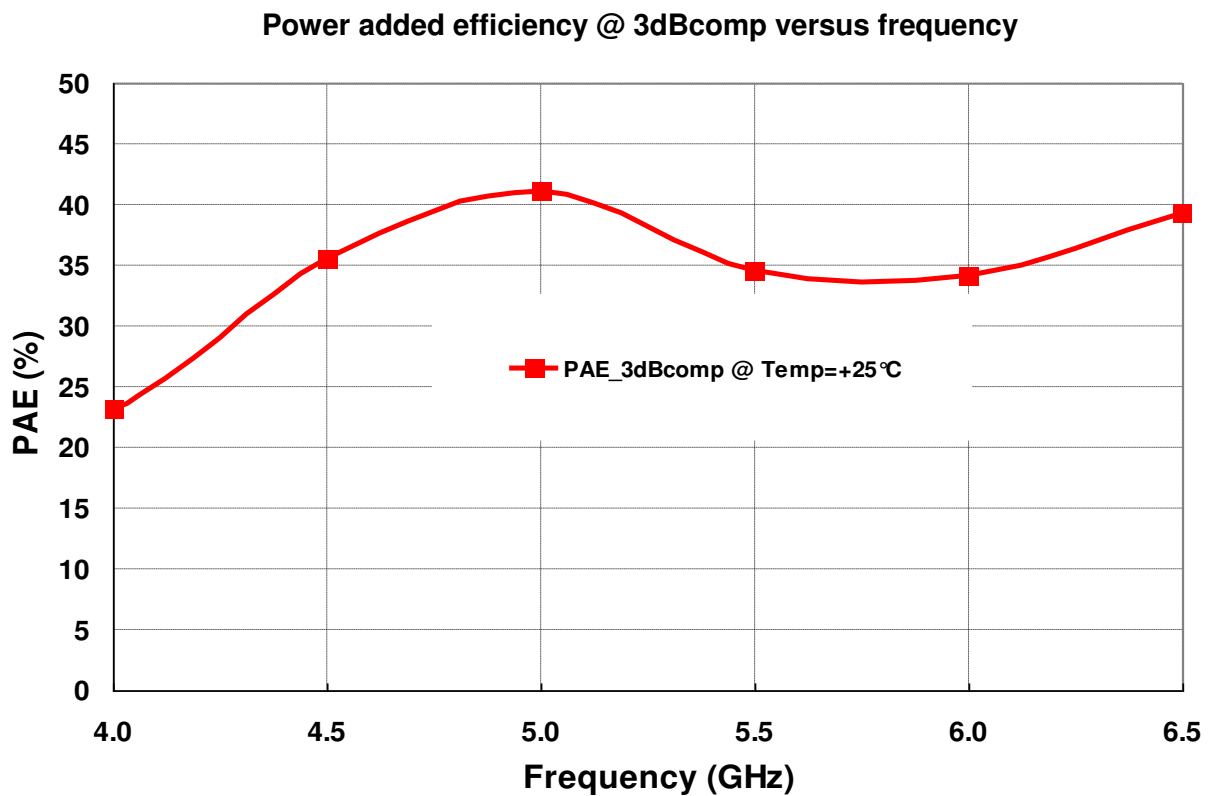
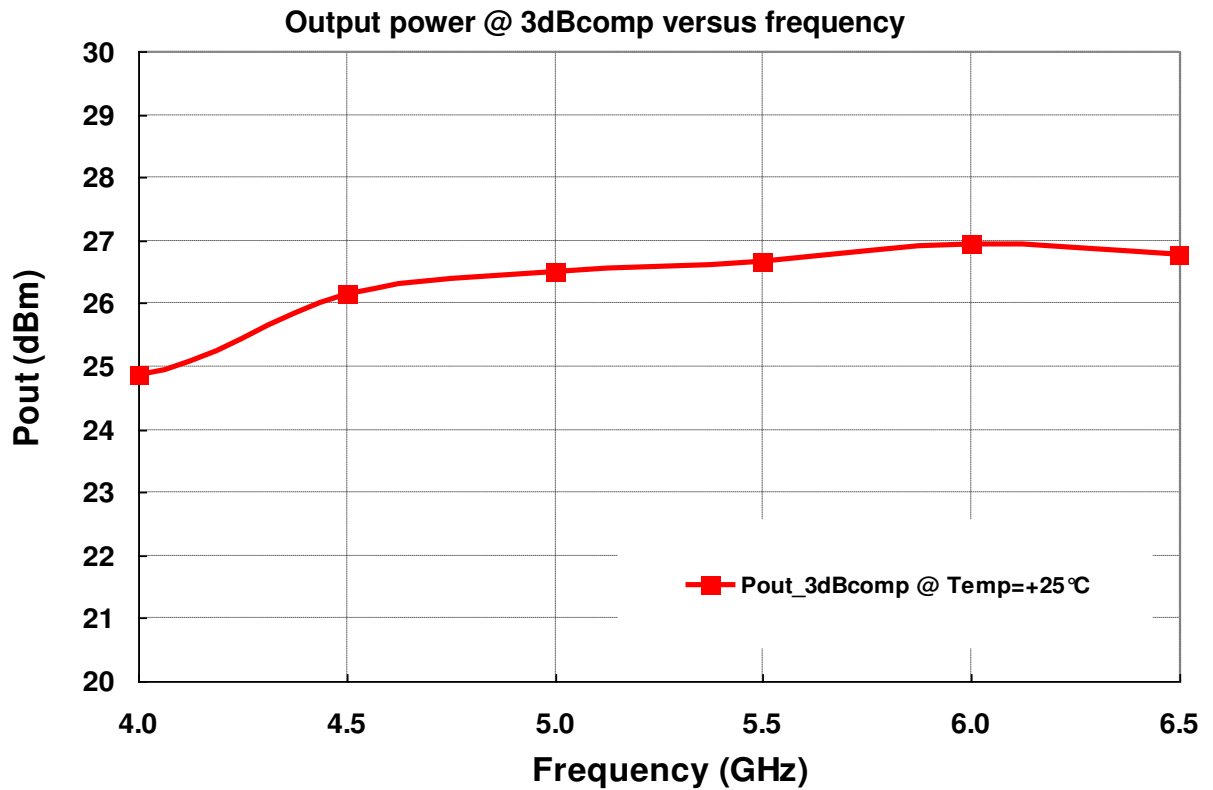


Drain Current @ 1dBcomp versus frequency



Typical on board Measurements

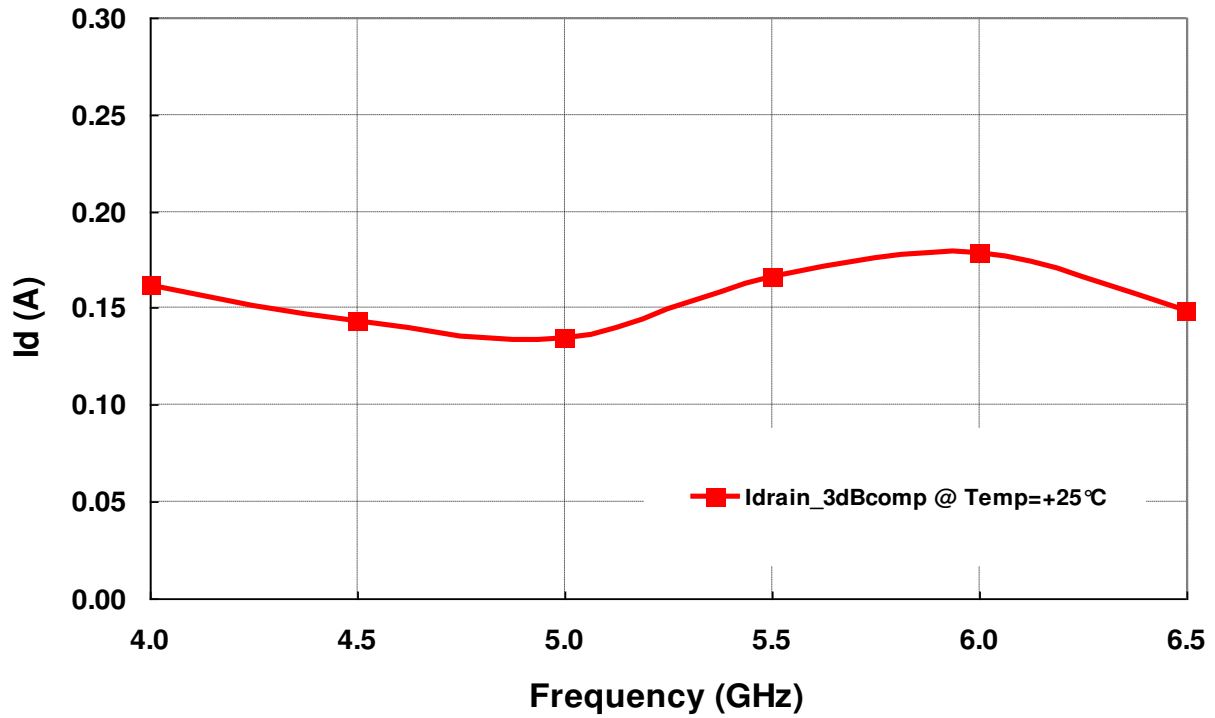
Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50µs, Duty cycle = 10%



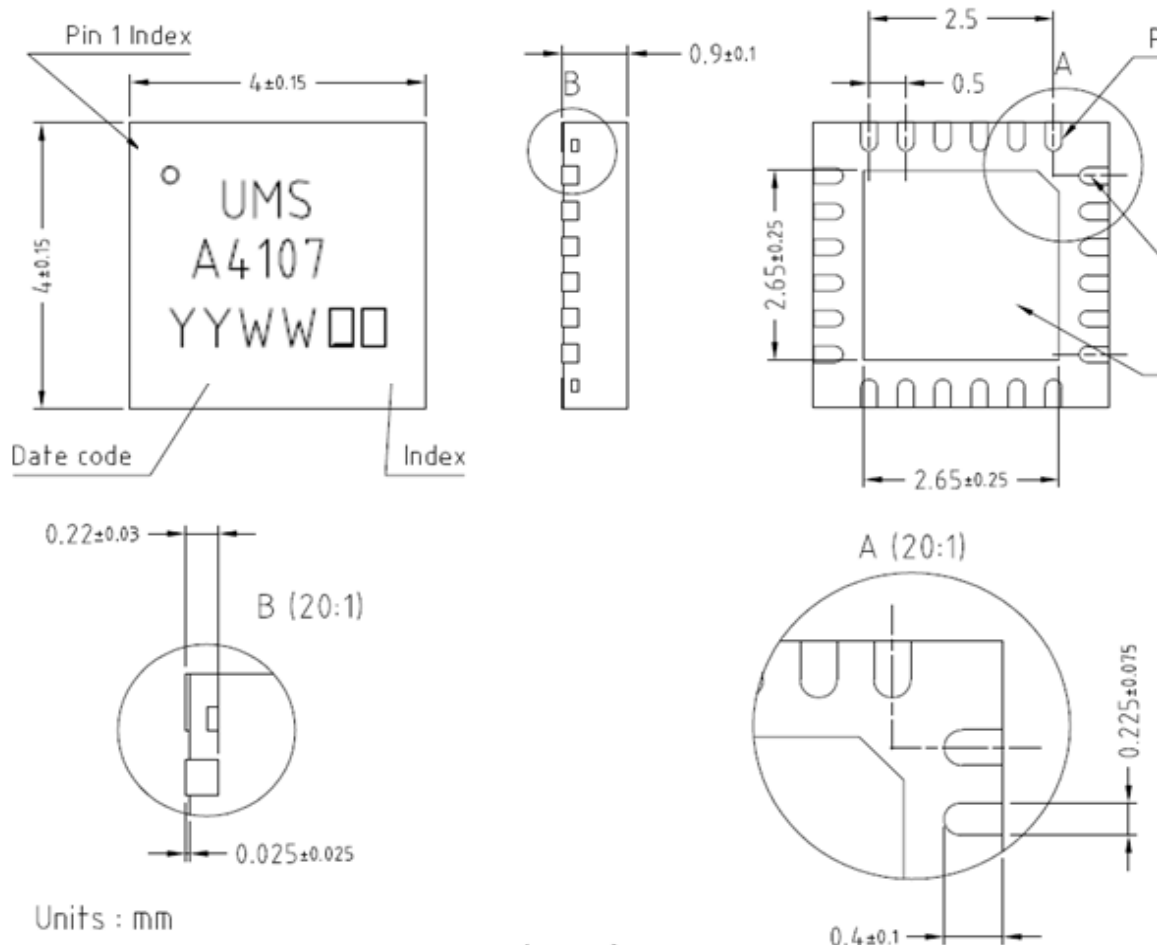
Typical on board Measurements

Vd = 8V, Id (Quiescent) = 120mA, Drain Pulse width = 50µs, Duty cycle = 10%

Drain Current @ 3dBcomp versus frequency



Package outline ⁽¹⁾



Units : mm
 From the standard : JEDEC MO-220 [VGGD]
 Matt tin, Lead free (Green)

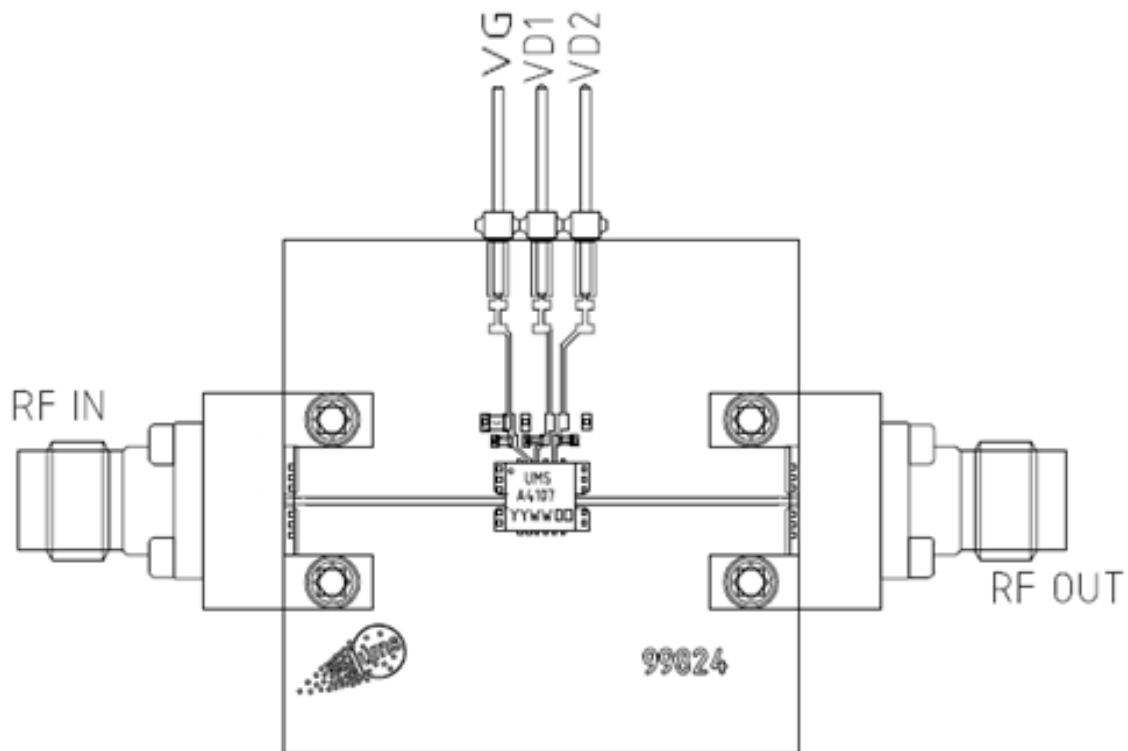
| | | | |
|---------------------------------------------|----------|------------|---------|
| Matt tin. Lead Free (Green) | 1- Nc | 9- Nc | 17- Gnd |
| Units : mm | 2- Gnd | 10- Nc | 18- Nc |
| From the standard : the JEDEC MO-220 (VGGD) | 3- Gnd | 11- Nc | 19- Nc |
| 25- GND | 4- RF In | 12- Nc | 20- Vd2 |
| | 5- Gnd | 13- Gnd | 21- Gnd |
| | 6- Gnd | 14- Gnd | 22- Vd1 |
| | 7- Nc | 15- RF out | 23- Vg |
| | 8- Nc | 16- Gnd | 24- Gnd |

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

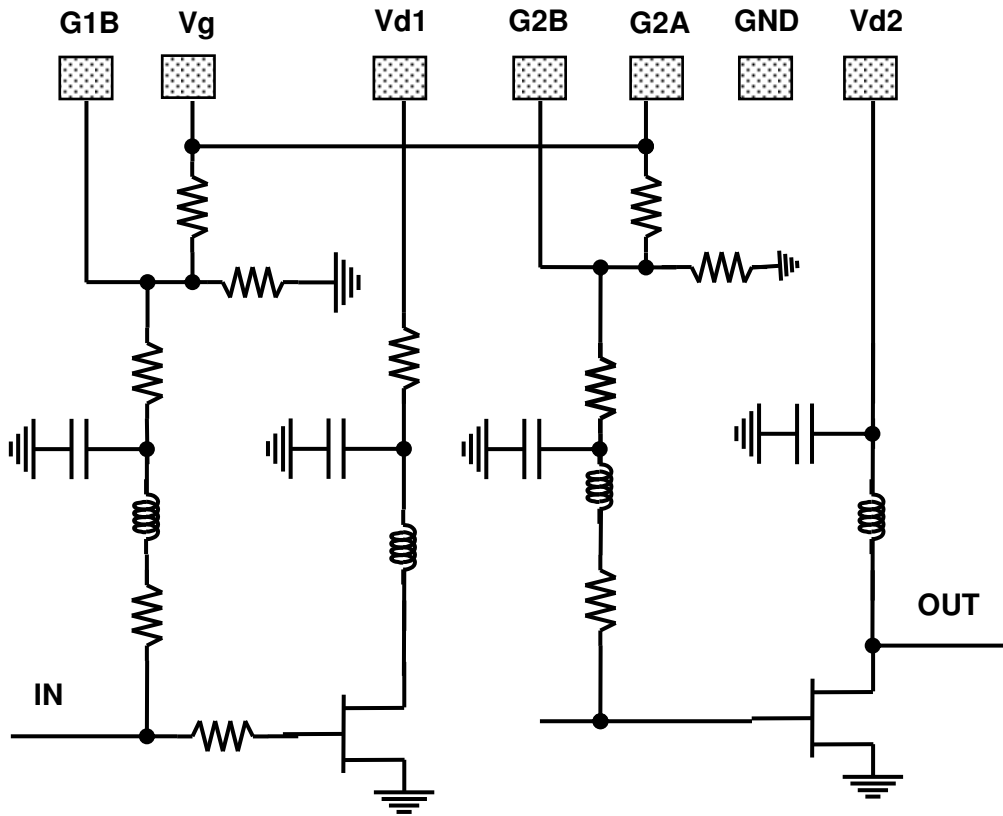
Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- In CW mode, decoupling capacitors of 10nF \pm 10% are recommended for Drain & Gate accesses.
- In pulsed mode, decoupling capacitors of 100pF in parallel with decoupling capacitors of 1nF are recommended for Drain access. On Gate access, decoupling capacitors of 100pF and 1 μ F in parallel are recommended.
- See application note AN0017 for details.



DC Schematic

Medium Power Amplifier: 8V, 120mA



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package: CHA4107-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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