S-Band 6-bit Phase Shifter

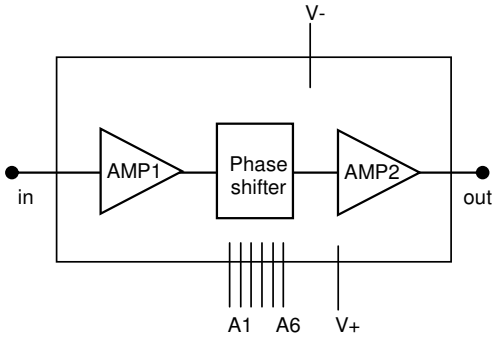
GaAs Monolithic Microwave IC

Description

The CHP1102-98F is 6-bit phase shifter with an amplifier at its input and output. The circuit is driven by a TTL compatible parallel interface. It is designed for radar systems.

The circuit is manufactured with a power pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

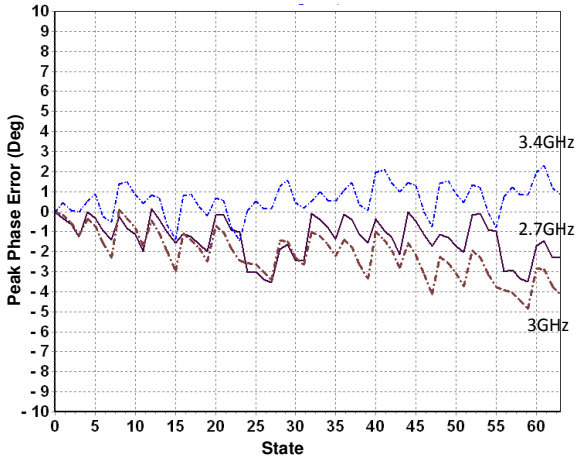
It is available in chip form.



Main Features

- Operating frequency range: 2.7-3.4GHz
- 6-bit phase shifter
- 5.625° phase step
- 10dB gain
- 0/+3.3V phase shifter control voltage
- 13dBm output @ 1dB comp.

- Chip size: 3.14x3.29x0.1mm



Peak Phase Error vs State @ 2.7, 3, 3.4GHz
(on wafer measurements)

Main Characteristics

Tamb= +25°C, V+= +5V, V-= -5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2.7		3.4	GHz
Gain	Small signal gain (state 0)	9	10		dB
RMS_PPE	RMS Peak Phase Error		1		deg

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	2.7		3.4	GHz
G	Small signal gain (state 0)	9	10		
Gvt	Small signal gain variation versus temperature		0.03		dB/°C
NF	Noise figure (state 0)		5.8		dB
S11	Input reflection coefficient		-15		dB
S22	Output reflection coefficient		-15		dB
PPEa	Peak phase error for states 1 to 2		+/- 1.5		°
PPEb	Peak phase error for states 3 to 14		+/- 3		°
PPEd	Peak phase error for states 15 to 63		+/- 5		°
RMS_PPE	RMS Peak phase error		1		°
Ava	Amplitude variation for states 1 to 4		+/- 0.3		dB
Avb	Amplitude variation for states 5 to 63		+/-0.7		dB
RMS_Av	RMS Amplitude variation		0.3		dB
StdDev_Av	Amplitude variation standard deviation		0.12		dB
P_{-1dB}	Output power at 1dB gain compression		13		dBm
V+	DC positive supply		+5		V
V-	DC negative supply		-5		V
Vctrl_L	Phase shifter control voltage (low state)	-	0	0.4	V
Vctrl_H	Phase shifter control voltage (high state)	2.4	3.3	7	V
I_V+	Courant I+ (state 0 and low level)		100		mA
I_V-	Courant I- (state 0 and low level)		23		mA

These values are representative of on wafer measurements.

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Peak Phase Error (PPE) definition

PPE(i) = measured_Phase(S21)@state(i) - measured_Phase(S21)@state(0) - theoreticalPhaseValue@State(i)

Amplitude Variation (Av) definition

Av(i) = Measured_dB(S21)@state(i) - Measured_dB(S21)@state(0)

RMS Peak Phase Error (RMS_PPE) definition

$$\text{RMS\_PPE} = \sqrt{\frac{\sum_{i=0}^{63}(\text{PPE}(i) - \overline{\text{PPE}})^2}{64}}$$

$$\text{Where } \overline{\text{PPE}} = \frac{\sum_{i=0}^{63}\text{PPE}(i)}{64}$$

RMS Amplitude variation (RMS_Av) definition

$$\text{RMS\_AV} = \overline{\text{Av}} = \frac{\sum_{i=0}^{63}\text{Av}(i)}{64}$$

Amplitude variation standart deviation (StdDev_Av) definition

$$\text{StdDev\_Av} = 20\log\left(1 + \sqrt{\frac{1}{64}.\sum_{i=0}^{63}(1 - \text{Av}(i)\_\text{lin})^2}\right) \text{ (dB)}$$

The translation of Av(i) from dB to linear is given by: $\text{Av(i)\_lin} = 10^{\frac{\text{Av}(i)}{20}}$
(i) is in the range [0:63]

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply	+6	V
V-	Maximum DC negative supply	-6	V
Vctrl	Phase shifter control voltage (Vlow Vhigh)	-0.5 +5.5	V
Pin	Maximum peak input power overdrive	+11	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Phase Shifter Control Interface

The phase shifter is controlled by 6 bits (A1 to A6). Reference state is “0”.
State is “0” when 0V is applied, state is “1” when +3.3V is applied.

State	A1	A2	A3	A4	A5	A6	Phase (deg)
0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	5,625
2	0	1	0	0	0	0	11,25
3	1	1	0	0	0	0	16,875
4	0	0	1	0	0	0	22,5
5	1	0	1	0	0	0	28,125
6	0	1	1	0	0	0	33,75
7	1	1	1	0	0	0	39,375
8	0	0	0	1	0	0	45
9	1	0	0	1	0	0	50,625
10	0	1	0	1	0	0	56,25
11	1	1	0	1	0	0	61,875
12	0	0	1	1	0	0	67,5
13	1	0	1	1	0	0	73,125
14	0	1	1	1	0	0	78,75
15	1	1	1	1	0	0	84,375
16	0	0	0	0	1	0	90
17	1	0	0	0	1	0	95,625
18	0	1	0	0	1	0	101,25
19	1	1	0	0	1	0	106,875
20	0	0	1	0	1	0	112,5
21	1	0	1	0	1	0	118,125
22	0	1	1	0	1	0	123,75
23	1	1	1	0	1	0	129,375
24	0	0	0	1	1	0	135
25	1	0	0	1	1	0	140,625
26	0	1	0	1	1	0	146,25
27	1	1	0	1	1	0	151,875
28	0	0	1	1	1	0	157,5
29	1	0	1	1	1	0	163,125
30	0	1	1	1	1	0	168,75
31	1	1	1	1	1	0	174,375
32	0	0	0	0	0	1	180
33	1	0	0	0	0	1	185,625
34	0	1	0	0	0	1	191,25
35	1	1	0	0	0	1	196,875
36	0	0	1	0	0	1	202,5
37	1	0	1	0	0	1	208,125
38	0	1	1	0	0	1	213,75
39	1	1	1	0	0	1	219,375
40	0	0	0	1	0	1	225
41	1	0	0	1	0	1	230,625
42	0	1	0	1	0	1	236,25
43	1	1	0	1	0	1	241,875
44	0	0	1	1	0	1	247,5
45	1	0	1	1	0	1	253,125
46	0	1	1	1	0	1	258,75
47	1	1	1	1	0	1	264,375
48	0	0	0	0	1	1	270
49	1	0	0	0	1	1	275,625
50	0	1	0	0	1	1	281,25
51	1	1	0	0	1	1	286,875
52	0	0	1	0	1	1	292,5
53	1	0	1	0	1	1	298,125
54	0	1	1	0	1	1	303,75
55	1	1	1	0	1	1	309,375
56	0	0	0	1	1	1	315
57	1	0	0	1	1	1	320,625
58	0	1	0	1	1	1	326,25
59	1	1	0	1	1	1	331,875
60	0	0	1	1	1	1	337,5
61	1	0	1	1	1	1	343,125
62	0	1	1	1	1	1	348,75
63	1	1	1	1	1	1	354,375

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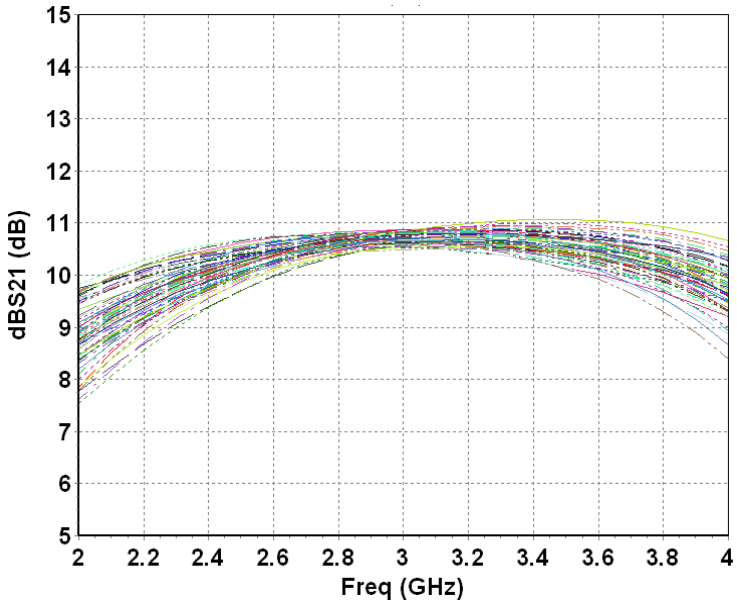
Typical S-parameter results (on wafer measurements)

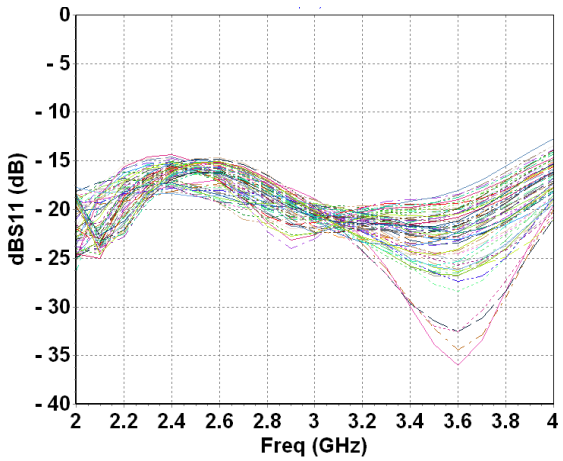
Tamb.= +25°C, V+ = +5V, V- = -5V.

[S] parameters

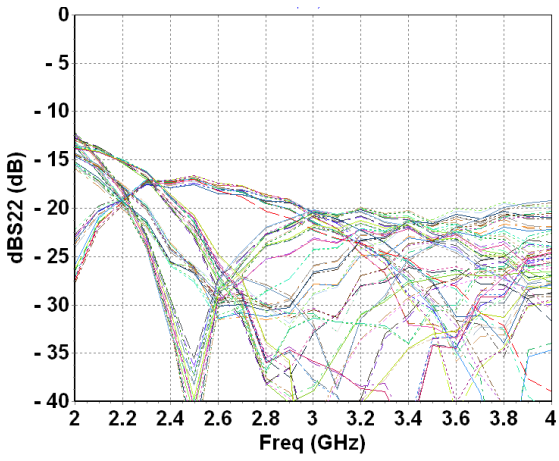
Gain versus Frequency
All phase states



Input return loss versus. Frequency
All phase states



Output return loss versus. Frequency
All phase states



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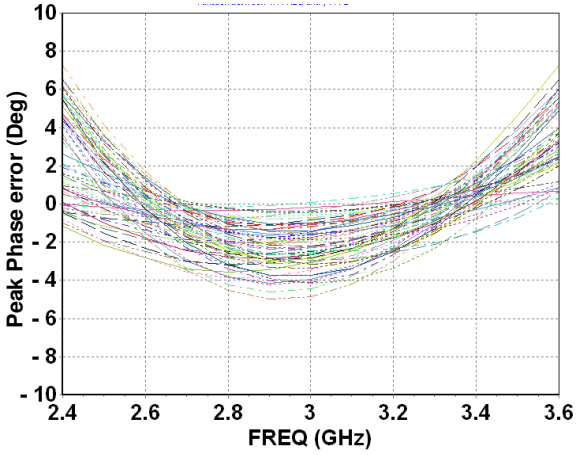
Typical S-parameter results (on wafer measurements)

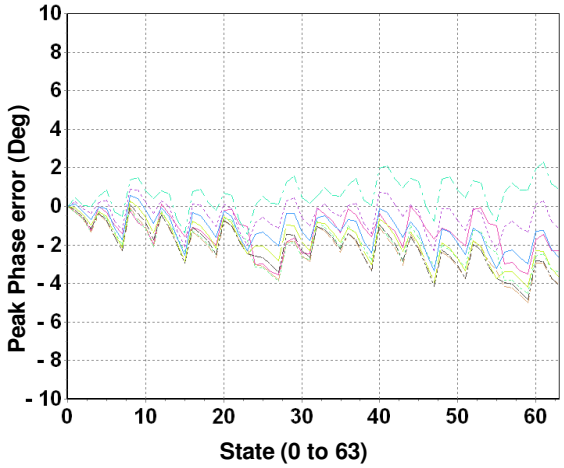
Tamb.= +25°C, V+ = +5V, V- = -5V

Phase shifter performances: Phase error

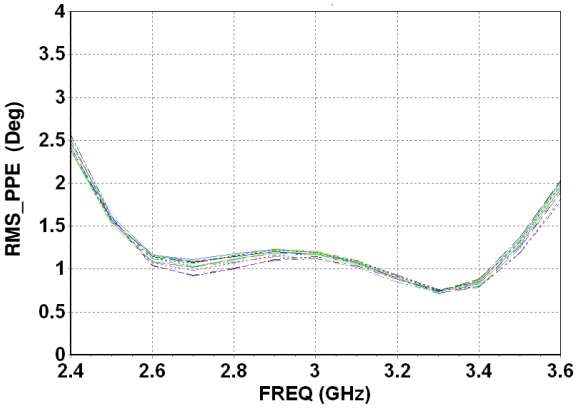
Peak phase error versus frequency (all phase states)



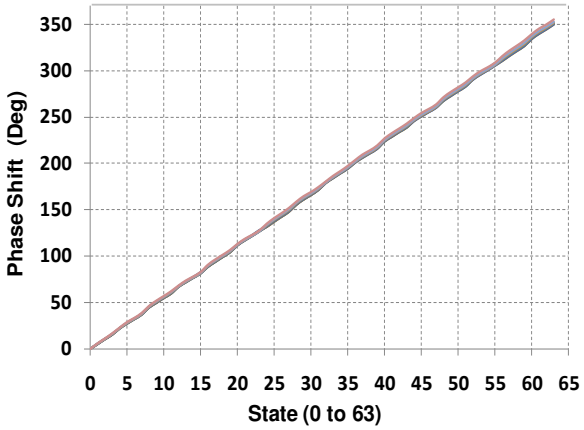
Peak phase error versus state 2.7GHz < frequency < 3.4GHz



RMS phase error versus frequency for 15 chips



Phase shift versus state 2.7GHz < frequency < 3.4GHz



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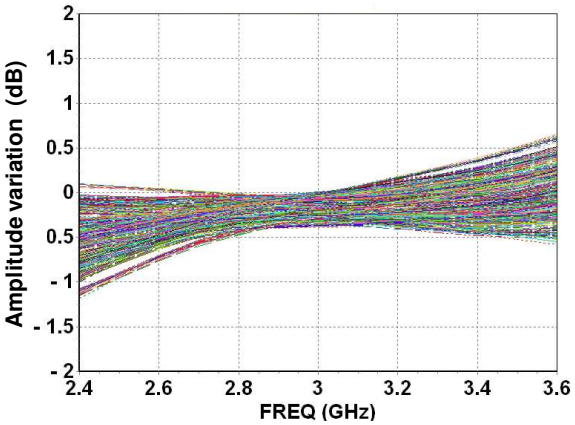
Typical S-parameter results (on wafer measurements)

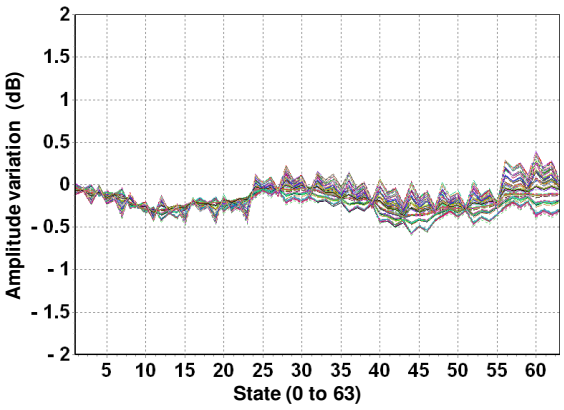
Tamb.= +25°C, V+ = +5V, V- = -5V

Phase shifter performances: Amplitude variation

Amplitude variation versus frequency
(all states)



Amplitude variation versus state
2.7GHz < frequency < 3.4GHz



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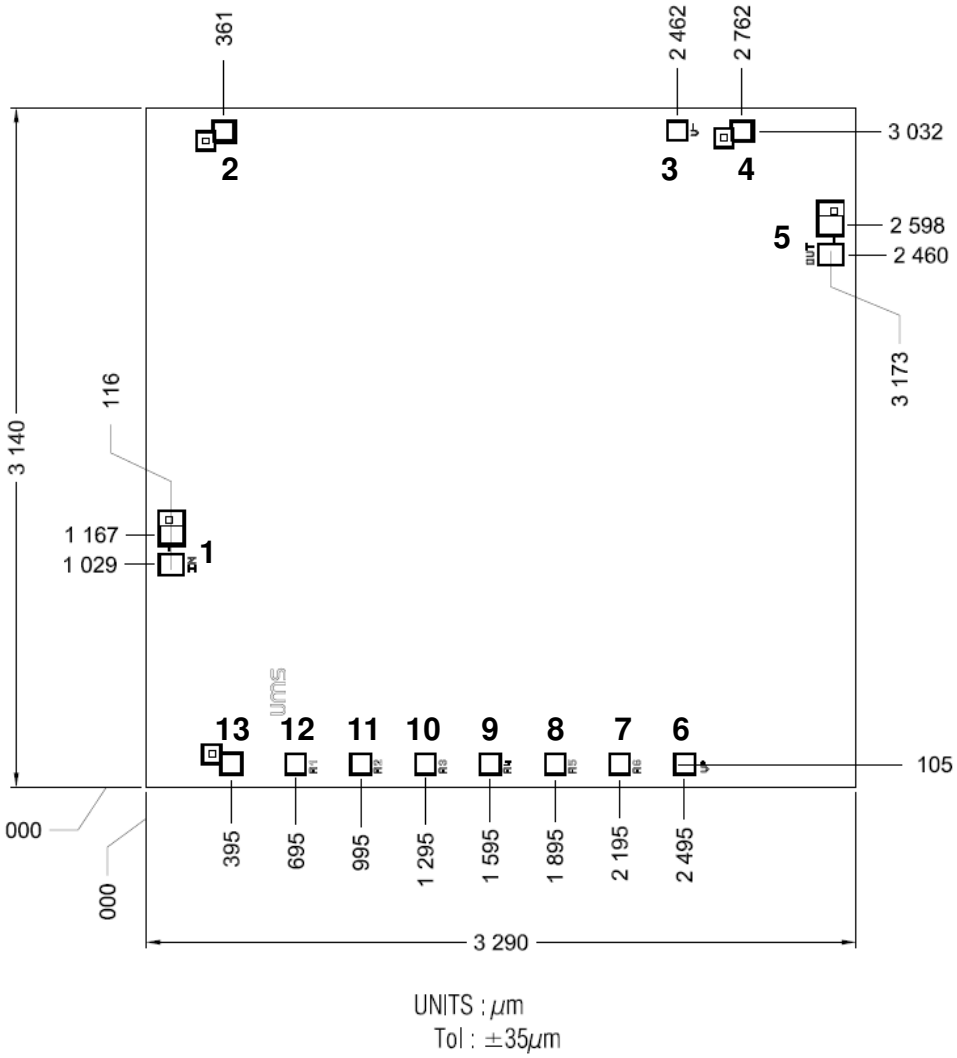
Mechanical dimensions and pad allocation



Chip thickness: 100µm +/- 10µm
RF pads (1, 5): 122 x 100µm²
DC and control pads (2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13): 100 x 100µm²

Pin number	Pad name	Description	Voltage Value
1	IN	Input RF	
2, 4, 13		NC	
3	V-	DC negative supply	-5V
5	OUT	Output RF	
6	V+	DC positive supply	+5V
7	A6	Phase shifter bit 6	0V / 3.3V or 0V / 5V
8	A5	Phase shifter bit 5	0V / 3.3V or 0V / 5V
9	A4	Phase shifter bit 4	0V / 3.3V or 0V / 5V
10	A3	Phase shifter bit 3	0V / 3.3V or 0V / 5V
11	A2	Phase shifter bit 2	0V / 3.3V or 0V / 5V
12	A1	Phase shifter bit 1	0V / 3.3V or 0V / 5V

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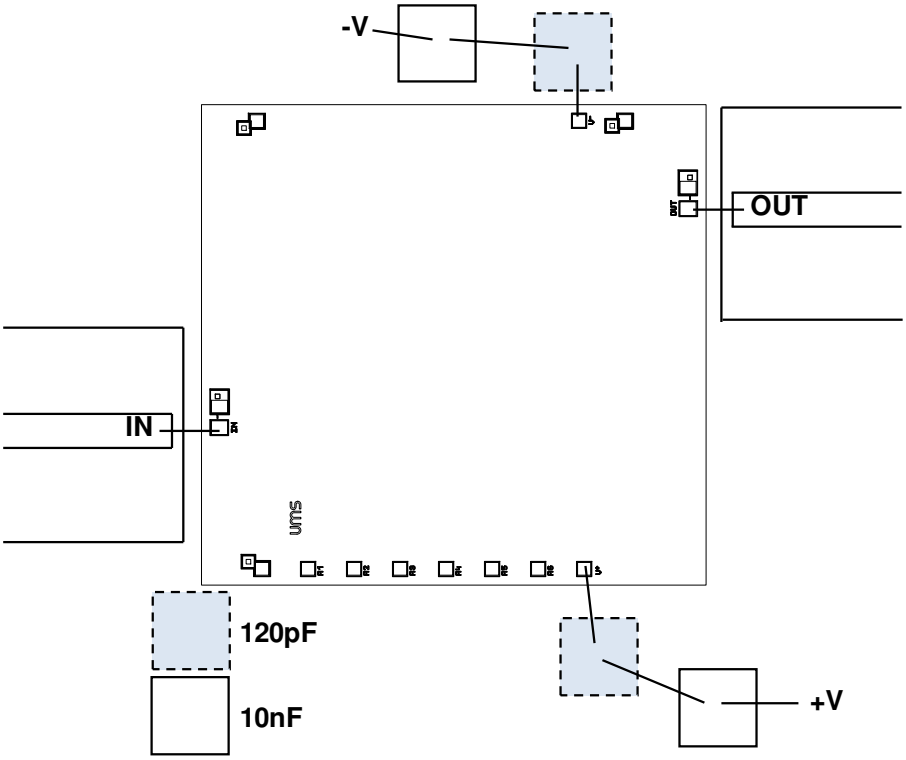
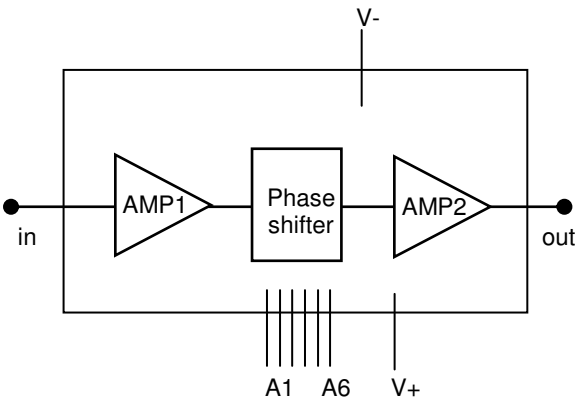
Bonding recommendations

Port	Connection
IN (1) OUT (5)	Inductance (Lbonding) = 0.3nH one wire: diameter 25µm, length 0.4mm
DC and Interface pads	Inductance (Lbonding) = 0.8nH one wire: diameter 25µm, length 1.0mm

Recommended assembly diagram



Circuit schematic



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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form:	CHP1102-98F

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