20-40GHz Frequency Multiplier

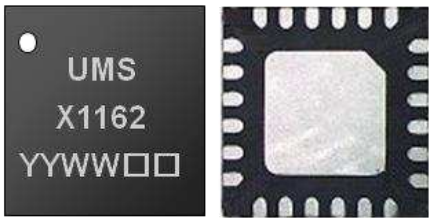
GaAs Monolithic Microwave IC

Description

The CHX1162-QDG is a packaged monolithic time two multiplier which integrates input and output buffer.

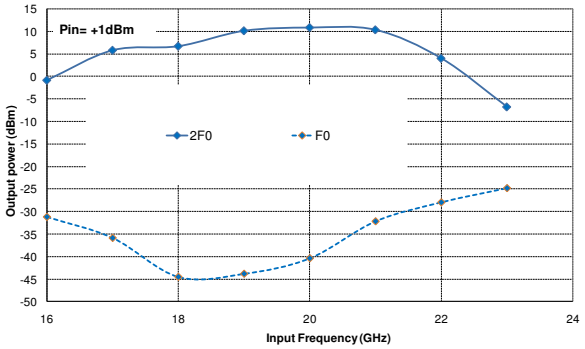
This circuit is a very versatile multiplier for telecommunication and specifically for E-band LO chain. Moreover it is proposed in standard surface mount package and integrates ESD protection. The overall power supply is of +5V/ 50mA.

It is developed on a robust 0.15µm gate length pHEMT process, and will be available in a standard SMD package.



Main Features

- Broadband performances: 17.5-21.5GHz
- 8dBm Pout for +1dBm input power
- DC bias: V+=5Volt, V- = -5V@Id=50mA
- 24L-QFN4x4



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	17.5		21.5	GHz
Fout	Output frequency range	35		43	GHz
Pin	Input power		+1		dBm
Pout_H2	Output Power		8		dBm

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Electrical Characteristics

Tamb.= +25°C, V+ = +5V

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	17.5		21.5	GHz
Fout	Output frequency range	35		43	GHz
Pin	Input power		+1		dBm
Pout_H2	2nd harmonic output power		8		dBm
Rej_H1	Fundamental rejection		40		dBc
RL _in	Input return loss		-12		dB
RL_out	Output return loss		-6		dB
V+	DC positive voltage		+5		V
V-	DC negative voltage		-5		V
Id	DC current		50		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Positive bias voltage	5.5	V
V-	Negative bias voltage	-6	V
Id	DC current	80	mA
Pin	Maximum input power	+6	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.

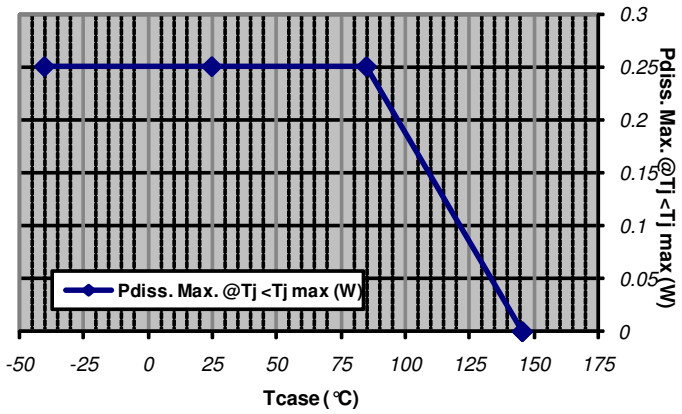
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

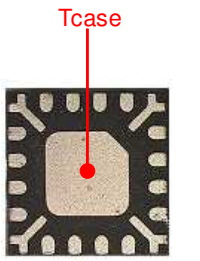
DEVICE THERMAL SPECIFICATION : CHX1162-QDG			
Recommended max. junction temperature (Tj max)	:	146	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	0.3	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	4	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<242	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

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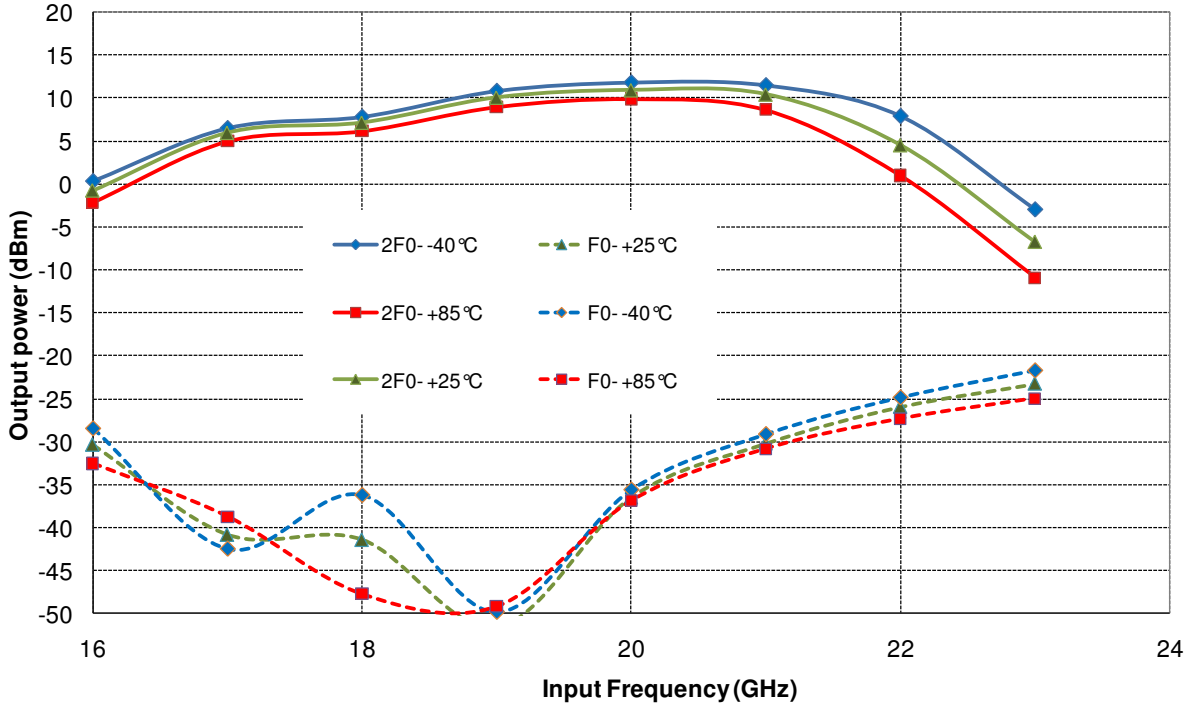
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, Id = 50mA
Results are given in the package access planes

2nd Harmonic & fundamental output power versus frequency
Pin= +1dBm



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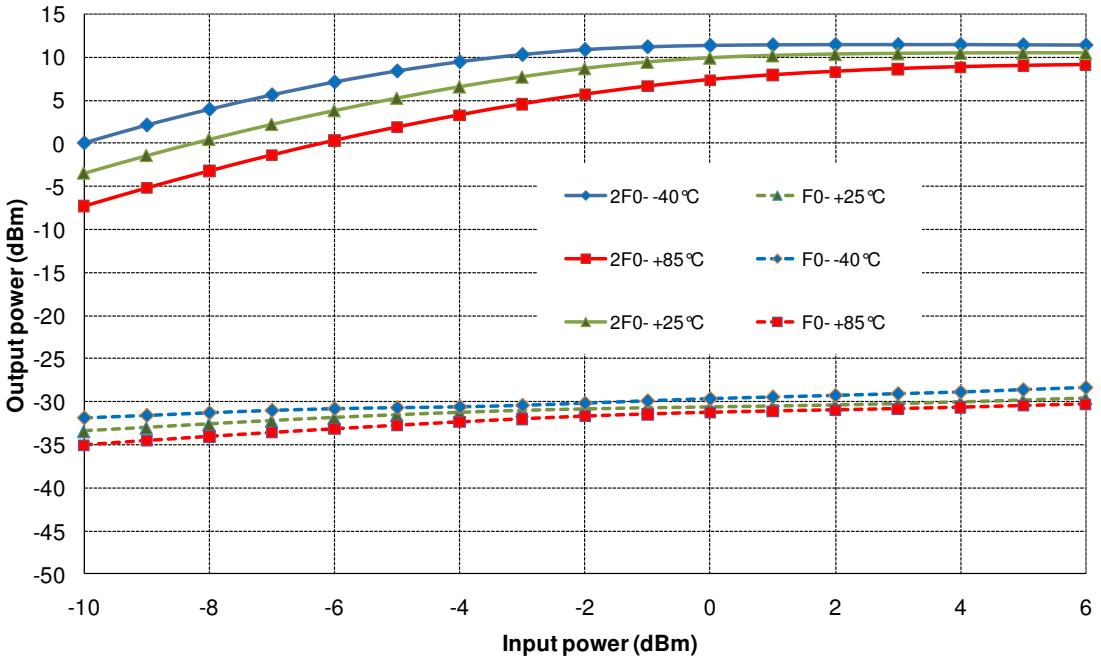
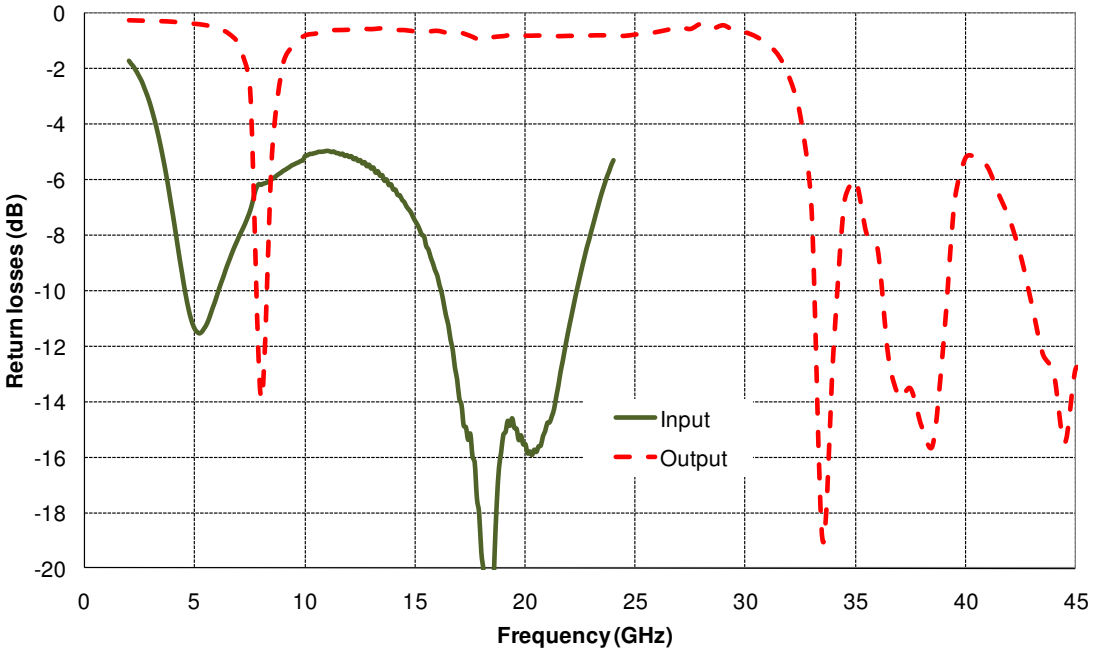
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, Id = 50mA

2nd Harmonic & fundamental output power versus input power
F0=21GHz



Input & Output return loss



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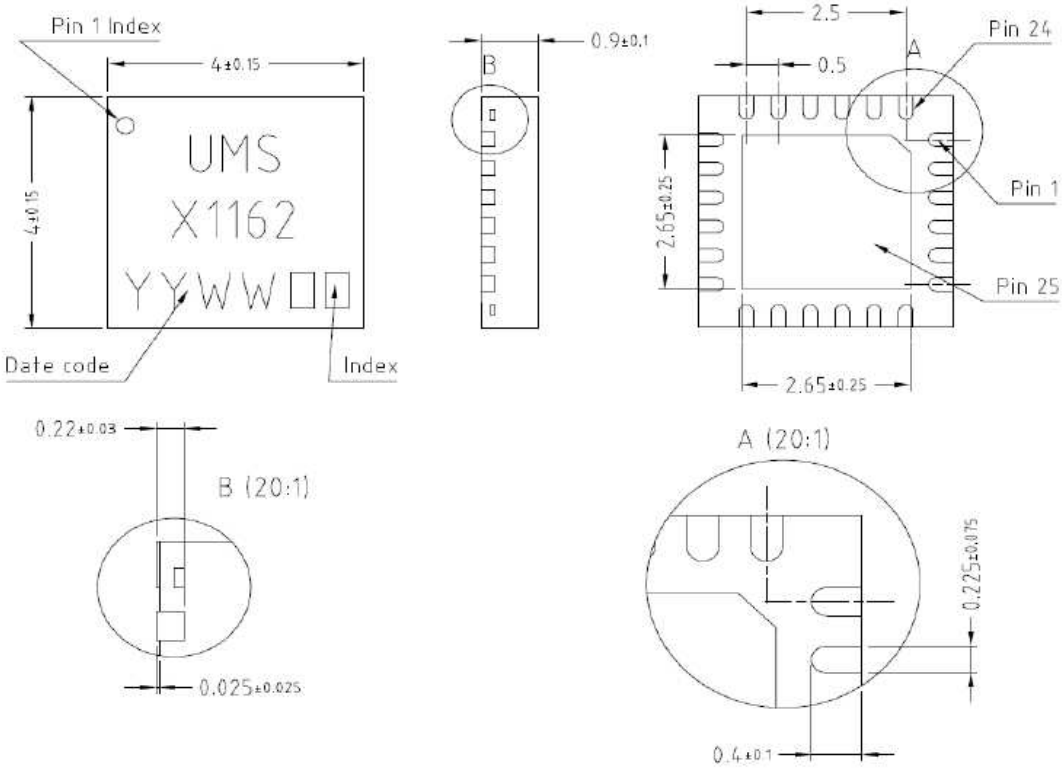
Package outline (1)



Matt tin, Lead Free (Green)	1- Nc	9- Nc	17- Gnd(2)
Units : mm	2- Gnd(2)	10- Nc	18- Nc
From the standard : JEDEC MO-220 (VGGD)	3- Gnd(2)	11- Nc	19- Nc
	4- RF in	12- Nc	20- V+
25- GND	5- Gnd(2)	13- Gnd(2)	21- Gnd(2)
	6- Gnd(2)	14- Gnd(2)	22- Nc
	7- Nc	15- RF out	23- V-
	8- Nc	16- Gnd(2)	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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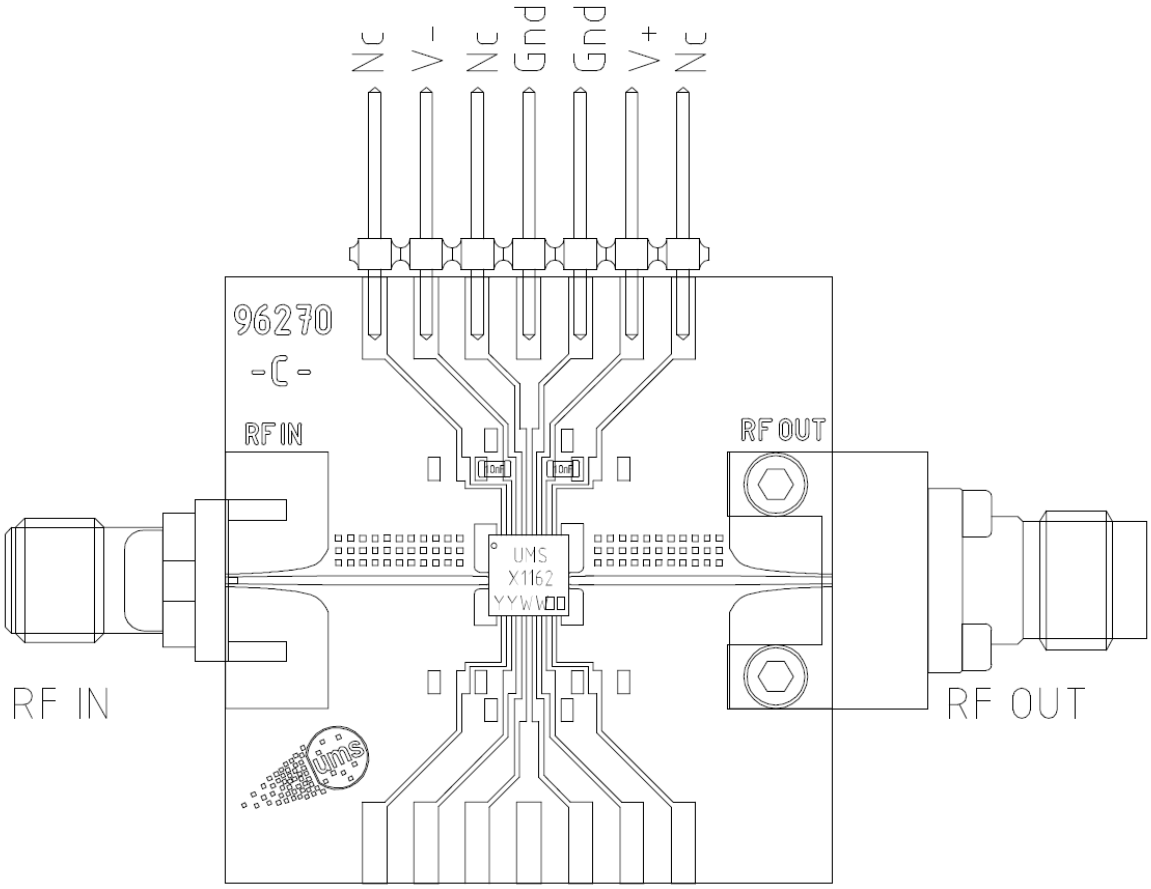
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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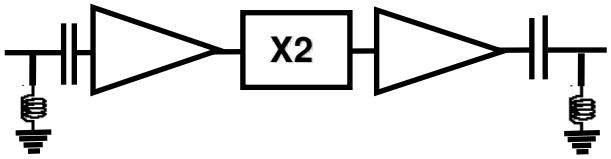
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

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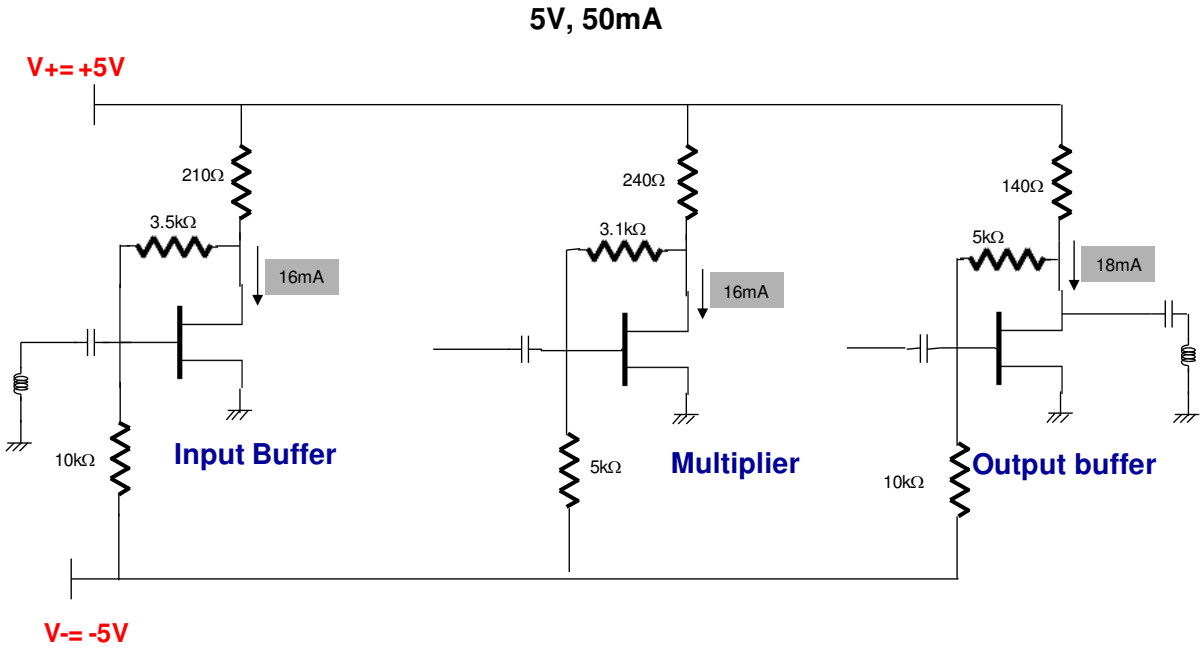
DC Schematic



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHX1162-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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