

W-band Dual Channel Mixer

GaAs Monolithic Microwave IC

Description

The CHM2378a is a dual channel mixer. Each mixer cell is a balanced structure based on a six quarter wave ring. The non-linear devices are high quality Schottky diodes providing low conversion loss and very low 1/f noise.

This circuit is manufactured with the BES-MMIC process: 1 μ m Schottky diode device, air bridges, via holes through the substrate, stepper lithography.

It is available in chip form.

Main Features

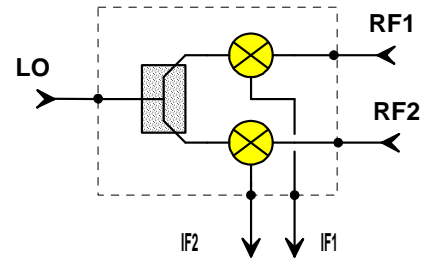
- W-band LO and RF frequency range
- Low conversion loss
- IF from DC to 100MHz
- High LO/RF isolation
- High LO/AM noise rejection
- Very low 1/f noise
- Low LO input power
- Automatic assembly oriented
- Chip size: 1.98 x 2.07 x 0.10 mm

Main Characteristics

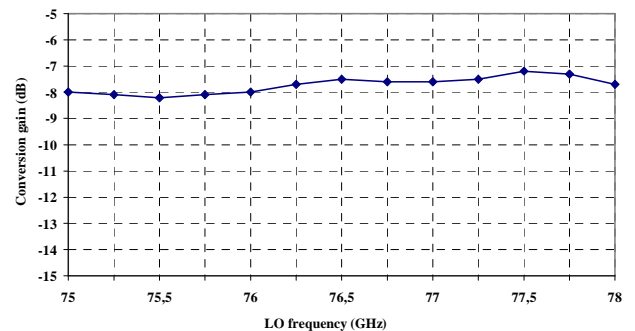
T_{amb.} = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_lo, F_rf	LO,RF frequency	76	76.5	77	GHz
F_if	IF frequency range	DC-100			MHz
Lc	Conversion loss		7.5	9.5	dB
I_lo/rf	LO/RF isolation		25		dB
N_if	IF noise @ 100kHz		-162		dBm/Hz

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!



Dual channel mixer block diagram



*Typical conversion characteristic
LO power = 8dBm ; IF=10MHz
(measurement in test fixture)*

Electrical Characteristics

Full operating temperature range, used according to section "Typical assembly and bias configuration"

Symbol	Parameter	Min	Typ	Max	Unit
F_lo, F_rf	LO,RF frequency	76		77	GHz
F_if	IF frequency range	DC-100			MHz
Lc	Conversion loss	4.5	7.5	9.5	dB
$ (d(\Delta Lc)/dT) * \Delta T $	Conversion loss difference from chip to chip versus temperature			0.3 (to be confirmed)	dB
P_lo	LO input power	4	7	11	dBm
P_RF_1dB	RF input power at 1 dB	-3	0		dBm
VSWR_lo	LO port VSWR (50Ω)		2:1	2.5:1	
VSWR_rf	RF port VSWR (50Ω)		2:1	2.5:1	
IMP_if	IF load impedance (1)		200		Ω
I_lo/rf	LO/RF isolation	20	25		dB
I_rf1/rf2	Isolation between RF channels	25	30		dB
I_rfi/rfj	Isolation between RF and IF channels	25	30		dB
R_lo_am	LO AM noise rejection (SSB)	25	30		dB
NF	Noise figure for IF=1kHz (2)		34	39	dB
	Noise figure for IF=10kHz (2)		28	33	dB
	Noise figure for IF=100kHz (2)		20.5	25.5	dB
	Noise figure for IF=200kHz (2)		17	22	dB
+V	Positive supply voltage (3)		4.5		V
+I	Positive supply current (3)		1.5	2.5	mA
Top	Operating temperature range	-40		+100	°C

(1) The IF optimum load for conversion loss is 200Ω. For minimum noise figure this load can be lower, the best results have been obtained on 50Ω.

(2) Measured on 200Ω IF impedance.

(3) An external resistor controls the bias current (see section "Typical Assembly and Bias Configuration")

Absolute Maximum Ratings (1)

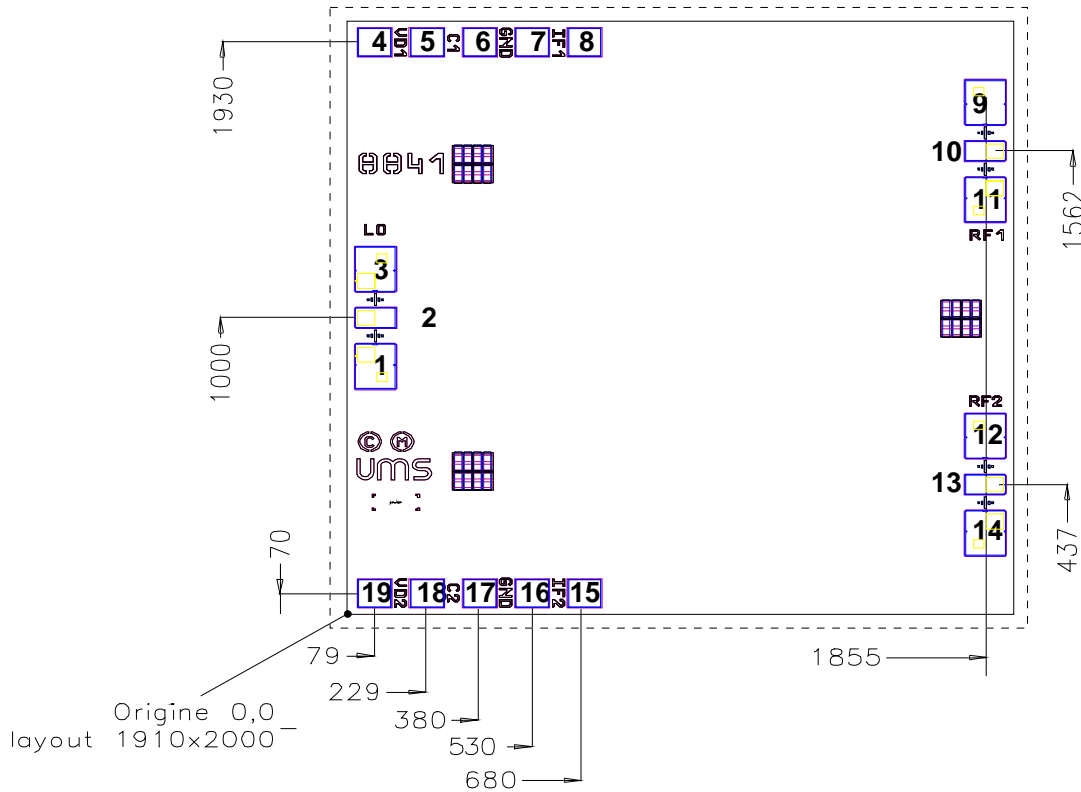
Symbol	Parameter	Values	Unit
+V	Supply voltage	6	V
+I	Supply current (for one input)	2.5	mA
P_lo	Maximum peak input power overdrive at LO port (2)	12	dBm
P_rf_cw	Maximum input power at RF port (3)	3	dBm
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s

(3) Continuous wave mode.

Chip Mechanical Data and Pin References



Unit = μm

External chip size (including dicing streets) = $1980 \times 2070 \pm 35$

Chip thickness = 100 ± 10

HF Pads (2,10,13) = 68×118

DC/IF Pads = 100×100

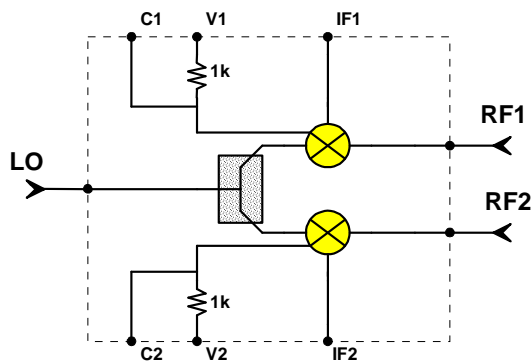
Pin number	Pin name	Description
1,3,9,11,12,14		Ground: should not be bonded. If required, please ask for more information.
6,17		Ground (optional)
7,16		Not Connected
2	LO	LO input
4	+V1	Positive supply voltage 1
5	C1	Bias 1 decoupling
8	IF1	First IF output
10	RF1	First RF input
13	RF2	Second RF input
15	IF2	Second IF output
18	C2	Bias 2 decoupling
19	+V2	Positive supply voltage 2

External components for bias and IF

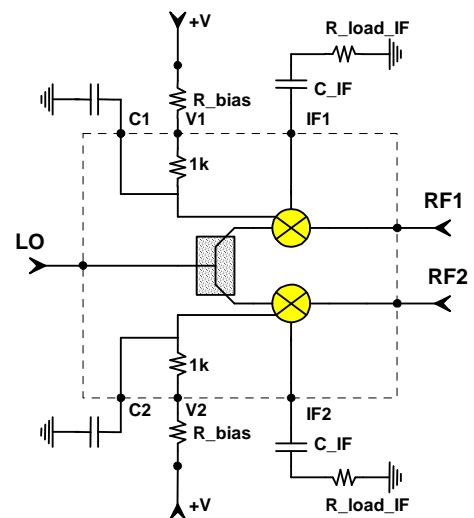
Several external configurations are possible for bias and IF. The objective is to give flexibility for the integration.

As this component is mainly dedicated to low IF use, there are several possibilities for interfacing with low noise IF amplifier. The optimum IF load for conversion loss is 200Ω , however the best results on noise figure have been obtained on 50Ω . Depending on the IF amplifier noise characteristic this load can be modified in order to optimise the noise figure.. A series capacitor, between IF output and the load is recommended.

Due to high sensitivity to electrical discharges an integrated resistance is used and two ports are available for biasing each mixer. One is for the connection of a decoupling capacitor (C1, C2) and the other one is for the supply voltage connection through an external series resistance (+V1, +V2). However, if necessary only the "C1, C2" ports can be used.



Block diagram of the MMIC



Recommended IF/DC external configuration

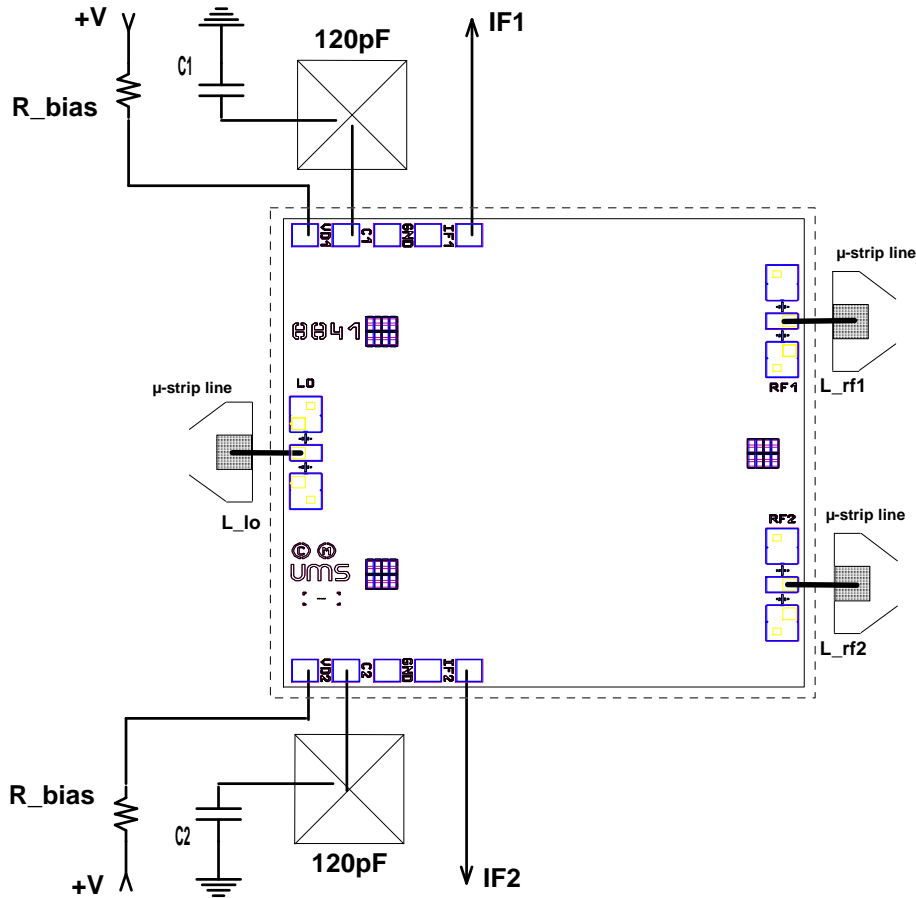
The recommended values for external components are:

C1,C2	$R_{bias_t} * C \gg 1/F_{if}$
R_bias_t	2.5k Ω for 1.5mA current consumption (V = 4.5V, typical LO power)
R_load_if	From 50 to 200 Ω

Notes::

1. $R_{bias_t} = R_{bias} + 1k\Omega$ when V1 and V2 ports are used.
2. R_{bias_t} can be adjusted if necessary; this allows optimising the performances when some parameters are different from recommended (Supply voltage, LO power). However maximum ratings for the current have to be taken into account.
3. A series capacitor at IF outputs is recommended for DC decoupling.

Typical Assembly Configuration



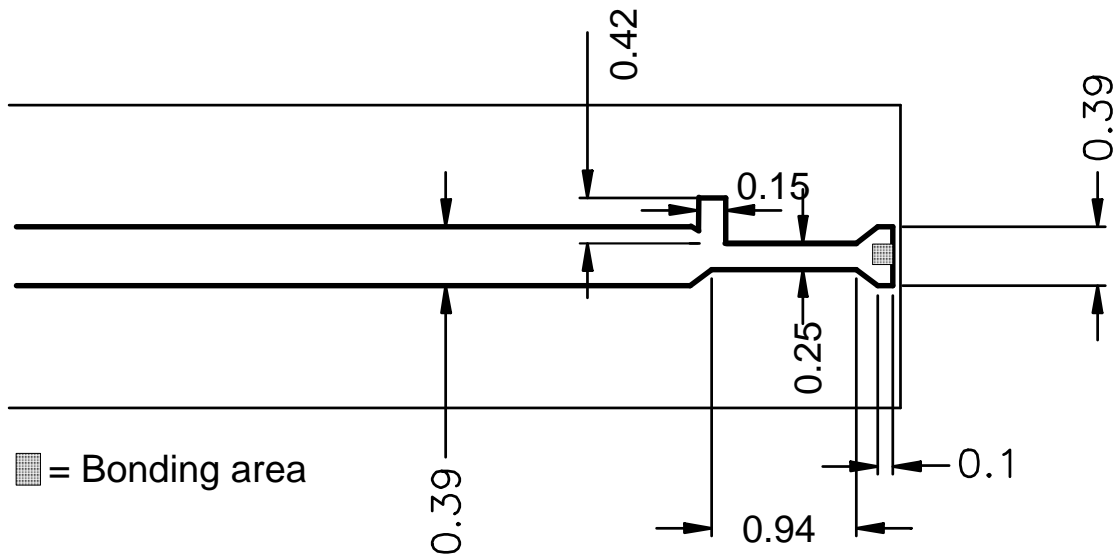
This drawing shows an example of assembly configuration. The bias and IF inter-connections are according to the example given in the previous chapter. For the RF pads the equivalent wire bonding inductance (diameter=25 μ m) have to be according to the following recommendation.

Port	Equivalent inductance (nH)	Approximative wire length (mm)
LO (2)	$L_{lo} = 0.26$	0.33
RF1 (10)	$L_{rf1} = 0.26$	0.33
RF2 (13)	$L_{rf2} = 0.26$	0.33

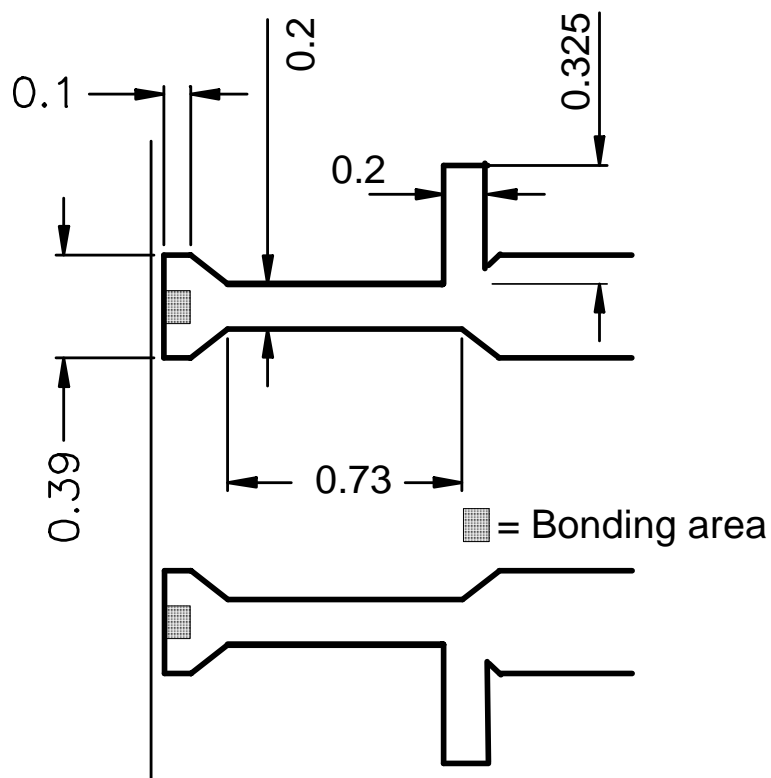
For a micro-strip configuration a hole in the substrate is recommended for chip assembly.

As the connections at 77GHz (between MMIC and MMIC or between MMIC and external substrate) are critical, the transition matching network is split into two parts: one on MMIC and one on the external substrate. This choice allows doing both kinds of connections.

In the case of connection from MMIC to an external substrate a network is proposed on soft substrate for LO, RF1 and RF2 ports. The following drawings give the dimensions (in mm) for a DUROID substrate (thickness=0.127mm, $\epsilon_r=2.2$).



Proposed matching network for a 50Ω transition between LO and a μ-strip line on DUROID substrate



Proposed matching network for a 50Ω transition between RF1/RF2 and μ-strip lines on DUROID substrate.

Ordering Information

Chip form: CHM2378a99F/00

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