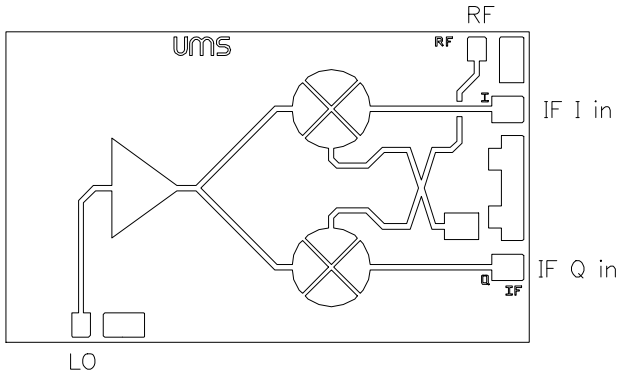
25-32GHz Single Side Band Mixer

GaAs Monolithic Microwave IC

Description

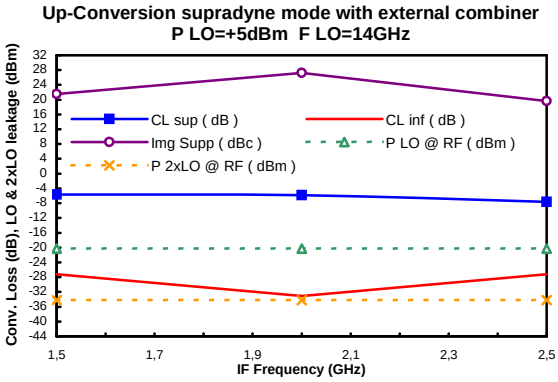
The CHM1291 is a multifunction chip (MFC) which integrates a LO buffer amplifier and a sub-harmonically balanced diodes mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion. It is designed for a wide range of applications, typically commercial communication systems for broadband local access (LMDS). The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performance : 25-32GHz
- 11dB conversion Loss
- 15dBc image rejection
- +5dBm LO input power
- +1dBm input power (1dB gain comp.)
- Low DC power consumption, 55mA@3.5V
- Chip size : 2.06 x 1.25 x 0.10mm



Main Characteristics

Tamb=+25℃

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	25		32	GHz
F_{LO}	LO frequency range	12		15.5	GHz
F_{IF}	IF frequency range	0.1		3	GHz
L_c	Conversion Loss		11	15	dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - B.P.46 - 91401 Orsay Cedex France
Tel. : +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Electrical Characteristics for Broadband Operation

Tamb=+25℃, Vd=3.5V, Id=55mA

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	25		32	GHz
F_{LO}	LO frequency range	12		15.5	GHz
F_{IF}	IF frequency range	0.1		3	GHz
L_c	Conversion Loss		11	15	dB
P_{LO}	LO Input power		+5		dBm
2xLO Leak	2xLO Leakage (for P_{LO}=+5dBm)		-35	-30	dBm
Img Rej	Image Rejection (1)	13	15		dBc
P1dB	Input power at 1dB gain compression	-2	0		dBm
P03	Input power at 3dB gain compression	0	+2		dBm
IP3	Input 3rd order intercept point		+8		dBm
LO Match	LO VSWR (2)		2.0:1		
RF Match	RF VSWR (2)		2.0:1		
IF Match	IF VSWR (2)		2.0:1		
Id	Bias current		55		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

(2) A bonding wire of typically 0.1 to 0.15nH will improve the accesses matching.

Current source biasing network is recommended.

Absolute Maximum Ratings

Tamb=+25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	100	mA
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +155	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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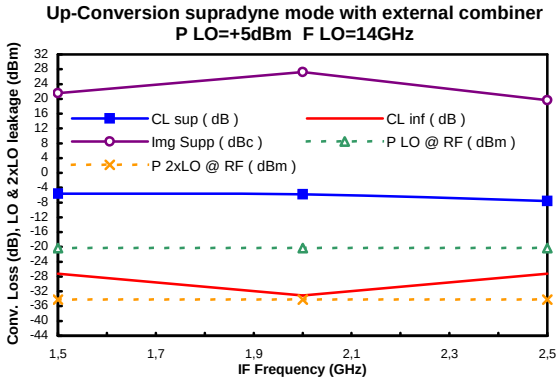
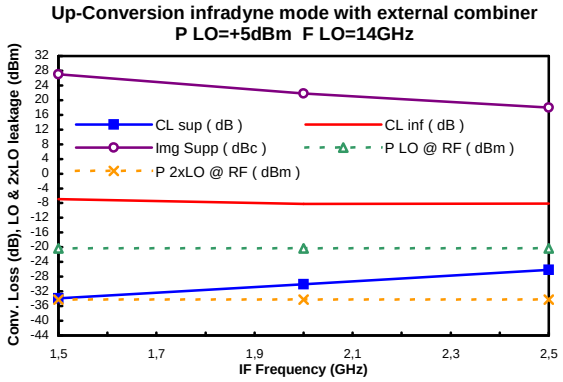
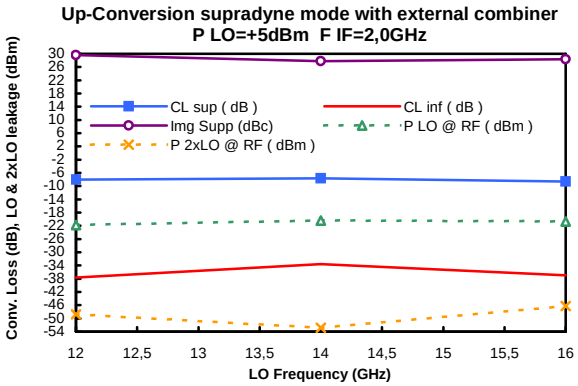
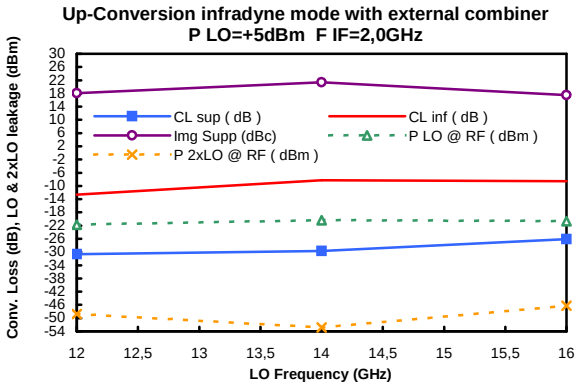
Typical On-wafer Measurements in Up-Conversion mode with external IF quadrature combiner

Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA



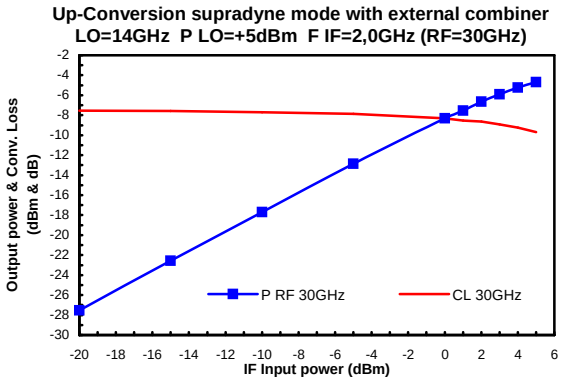


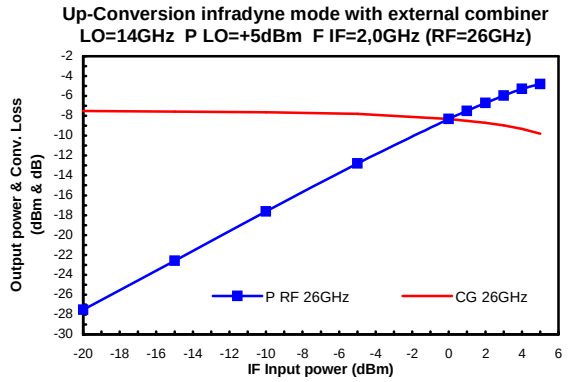




Typical On-wafer Compression Measurements in Up-Conversion mode with external IF quadrature combiner

Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA





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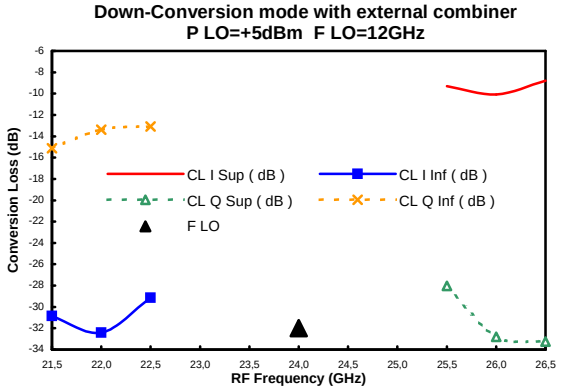
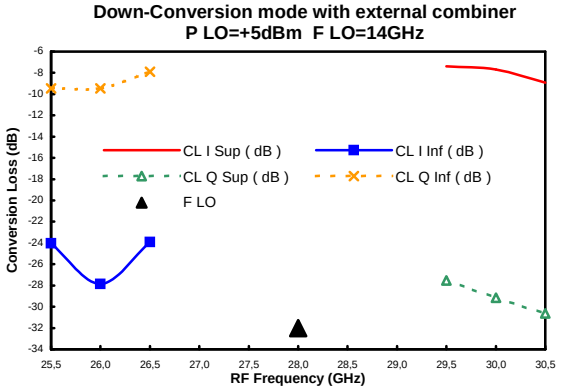
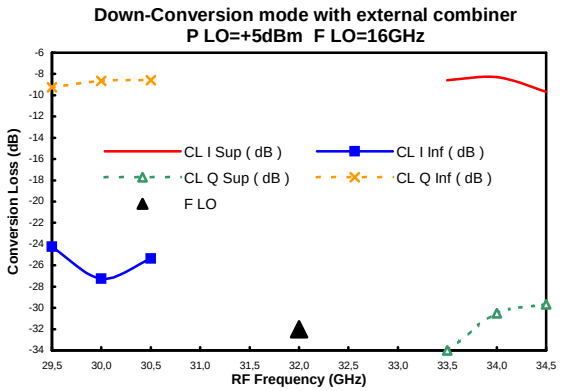
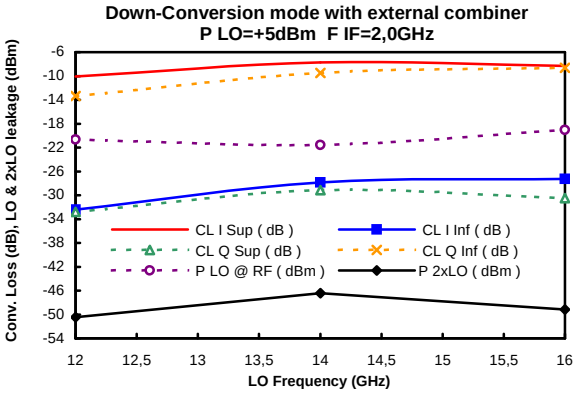
Typical On-wafer Measurements in Down-Conversion mode with external IF quadrature combiner

Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA



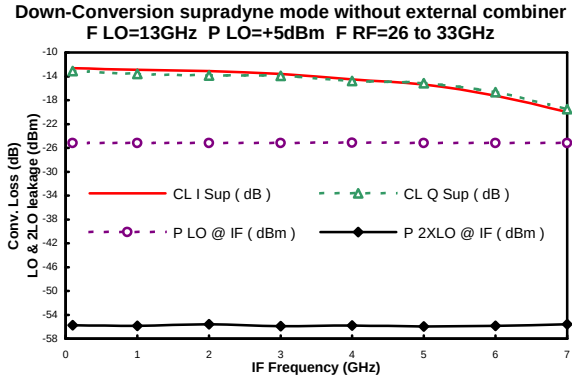


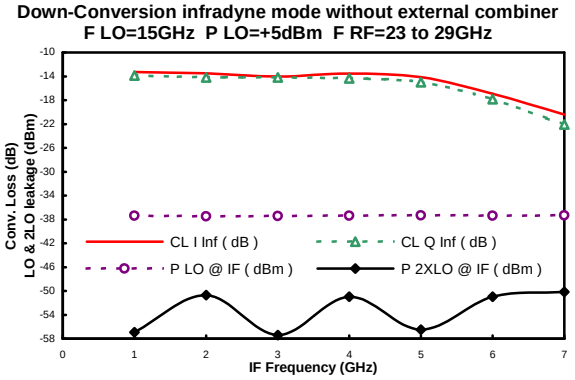




Typical On-wafer Measurements in Down-Conversion mode without external IF quadrature combiner

Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA





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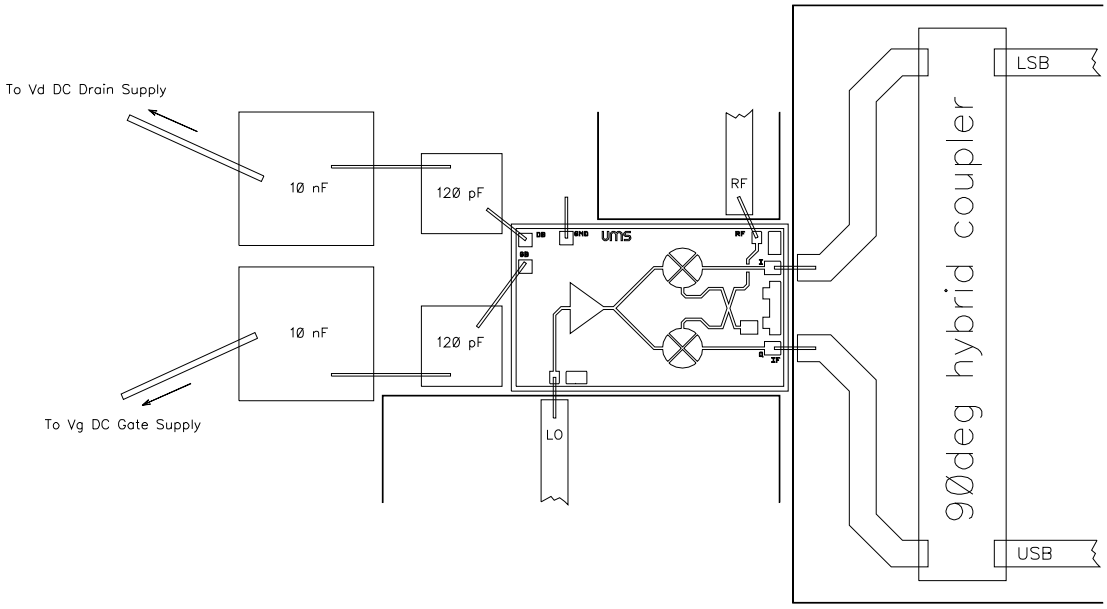
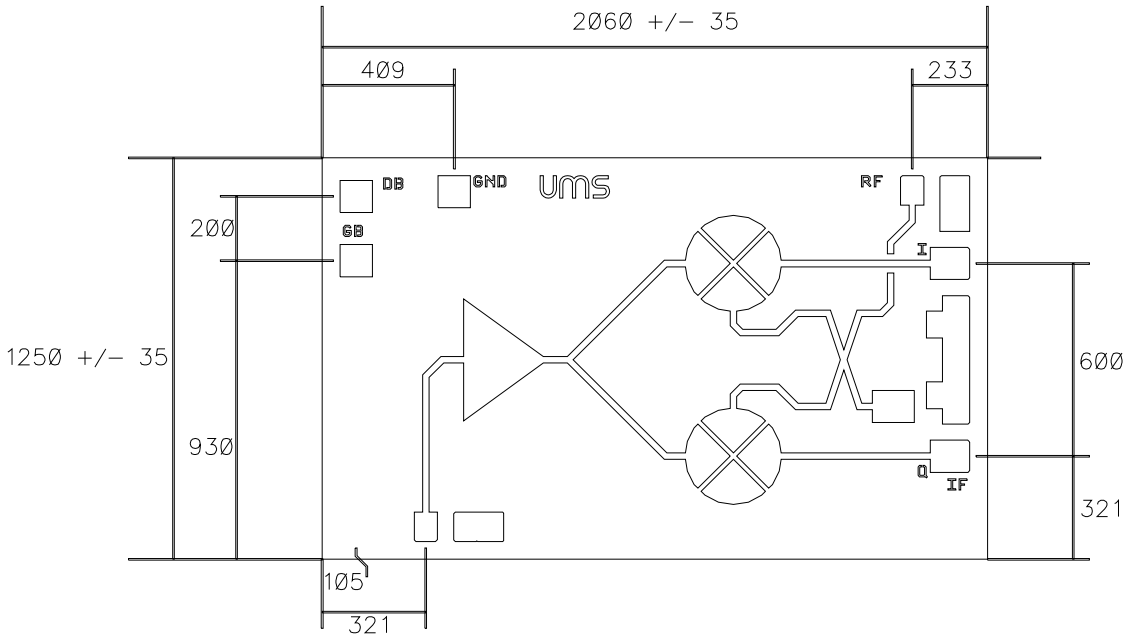
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions

(Chip thickness : 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form : CHM1291-99F/00

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