

80-105GHz Balanced Low Noise Amplifier

GaAs Monolithic Microwave IC

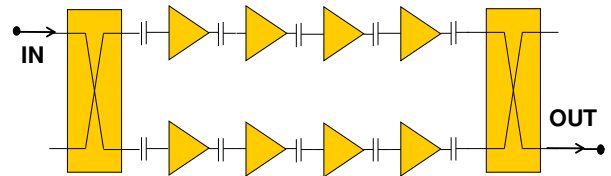
Description

The CHA1008-99F is a broadband, balanced, four-stage monolithic low noise amplifier.

It is designed for Millimeter-Wave Imaging applications and can be used in commercial digital radios and wireless LANs.

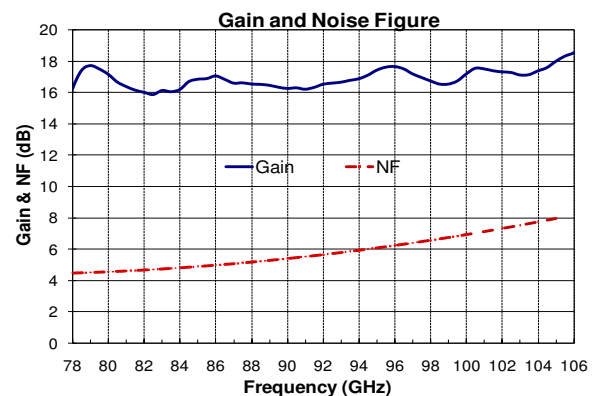
The circuit is manufactured on a pHEMT process, 0.10µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performances: 80-105GHz
- Balanced configuration
- 16dB linear gain from 80 to 90GHz
- 5dB noise figure from 80 to 90GHz
- DC bias: VD=2.5V@ ID=115mA
- Chip size 3.40x1.60x0.07mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	80		105	GHz
Gain	Linear Gain (from 80 to 90GHz)		16		dB
NF	Noise Figure (from 80 to 90GHz)		5		dB
Pout	Output Power @1dB comp.		5		dBm

CHA1008-99F 80-105GHz Balanced Low Noise Amplifier

Electrical Characteristics

Tamb.= +25°C, VD = 2.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	80		105	GHz
Gain	Linear Gain		17		dB
NF	Noise Figure		[80-90]GHz [90-100]GHz [100-105]GHz	5.0 6.5 7.5	dB
RLin	Input Return Loss		-14		dB
RLout	Output Return Loss		-12		dB
IN/OUT impedance	Input & Output impedance in the chip plan		50		Ohms
OP1dB	Output Power @1dB compression		5		dBm
VG1, VG2	Gate voltages (either on VG1 or VG2 or both on VG1 & VG2)		+0.15		V
VD	Drain voltage		2.5		V
ID	Drain current		115		mA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD	Drain bias voltage	3	V
ID	Drain bias current	150	mA
VG1, VG2	Gate bias voltage	-2 to +0.8	V
Pin	Maximum peak input power overdrive ⁽²⁾	0	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD	DC drain voltage	2.5	V
ID	Drain current controlled with VG1 or VG2	115	mA
VG1, VG2	DC gate voltages linked together into the circuit (only one can be used)	+0.15	V

Typical on-wafer Sij parameters

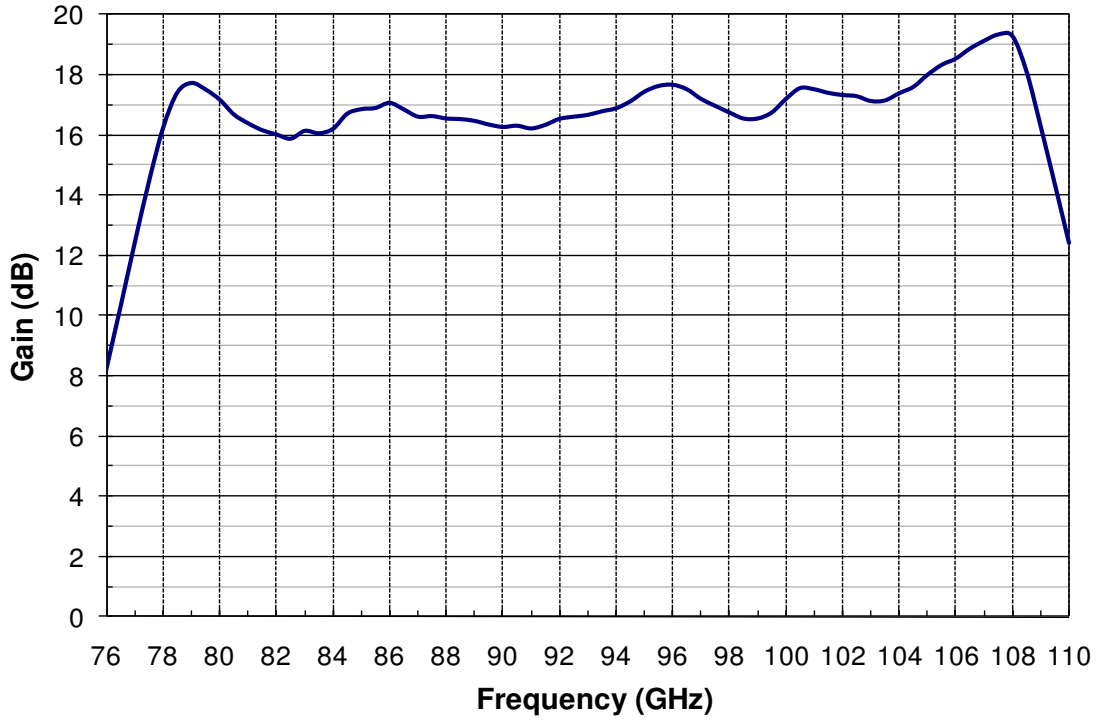
Tamb.= +25°C, VD = 2.5V, ID = 115mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
70	-9.62	-27.4	-46.61	-1.7	-14.84	-77.4	-19.06	-147.5
71	-7.90	-59.9	-45.20	-29.0	-12.29	-97.7	-23.78	-147.3
72	-6.07	-92.8	-40.60	-79.9	-9.91	-112.3	-15.39	-132.2
73	-4.55	-129.0	-39.39	-141.1	-6.20	-126.5	-15.31	-151.5
74	-2.99	-177.8	-38.67	-178.6	-1.39	-145.8	-16.08	174.2
75	-3.70	112.1	-37.80	122.6	3.76	-175.9	-21.34	156.5
76	-7.04	27.1	-39.02	57.8	8.27	147.2	-32.33	-88.8
77	-9.89	-54.8	-49.41	11.4	12.45	106.5	-25.50	-87.4
78	-11.11	-119.6	-50.15	8.0	16.25	55.7	-15.98	-91.1
79	-15.87	-165.0	-47.11	-33.3	17.72	-1.7	-14.77	-113.8
80	-24.20	173.2	-60.94	-113.5	17.16	-50.1	-12.28	-136.7
81	-28.72	-99.1	-51.00	-67.4	16.38	-88.2	-12.32	-152.4
82	-21.77	-98.6	-48.05	-109.3	16.01	-121.7	-13.09	-159.2
83	-18.19	-113.9	-53.75	-119.6	16.13	-154.9	-11.89	-171.9
84	-16.98	-118.1	-52.54	-161.8	16.20	174.3	-12.21	171.4
85	-15.21	-135.4	-51.74	146.8	16.85	141.8	-13.98	156.7
86	-15.61	-154.4	-52.07	103.4	17.06	107.0	-15.12	152.8
87	-16.28	-162.2	-55.59	-10.9	16.60	73.6	-15.11	154.1
88	-16.82	-172.6	-63.41	-173.6	16.54	44.6	-15.99	144.6
89	-17.77	174.3	-59.12	100.7	16.46	14.0	-16.01	138.5
90	-20.16	162.6	-56.99	37.3	16.26	-16.5	-15.98	127.1
91	-23.37	160.8	-58.98	-48.2	16.21	-45.1	-17.49	117.1
92	-25.07	174.8	-63.88	42.0	16.53	-73.5	-18.31	108.2
93	-27.83	-176.8	-49.55	15.8	16.66	-103.9	-18.51	99.7
94	-24.20	-142.3	-45.20	-14.8	16.88	-132.6	-23.35	82.7
95	-19.58	-159.9	-44.79	-51.8	17.43	-163.4	-27.83	119.0
96	-19.07	169.2	-47.08	-78.6	17.66	160.9	-20.18	121.6
97	-20.34	148.5	-47.05	-86.8	17.19	127.5	-20.52	105.7
98	-21.08	132.2	-46.64	-96.8	16.74	97.5	-20.30	83.3
99	-20.56	115.6	-46.80	-89.2	16.54	69.0	-21.28	67.8
100	-19.37	85.3	-43.63	-90.3	17.19	41.0	-28.63	-10.1
101	-18.31	52.3	-41.25	-106.8	17.51	4.7	-28.04	164.1
102	-16.68	28.0	-40.83	-125.1	17.32	-29.6	-21.86	121.9
103	-14.47	1.7	-43.05	-142.1	17.12	-62.6	-22.99	113.3
104	-13.45	-28.5	-41.39	-138.6	17.38	-94.2	-22.85	74.3
105	-13.48	-46.5	-40.08	-150.1	17.99	-129.8	-30.09	105.1
106	-12.52	-54.9	-40.47	-165.1	18.53	-169.5	-28.68	173.0
107	-11.21	-72.6	-41.80	-163.4	19.12	146.3	-20.32	169.1
108	-11.12	-84.1	-39.92	175.3	19.28	91.4	-12.90	138.1
109	-9.82	-90.7	-36.78	173.2	16.28	29.9	-10.74	106.6
110	-8.67	-109.5	-36.82	159.6	12.41	-8.0	-10.66	76.0

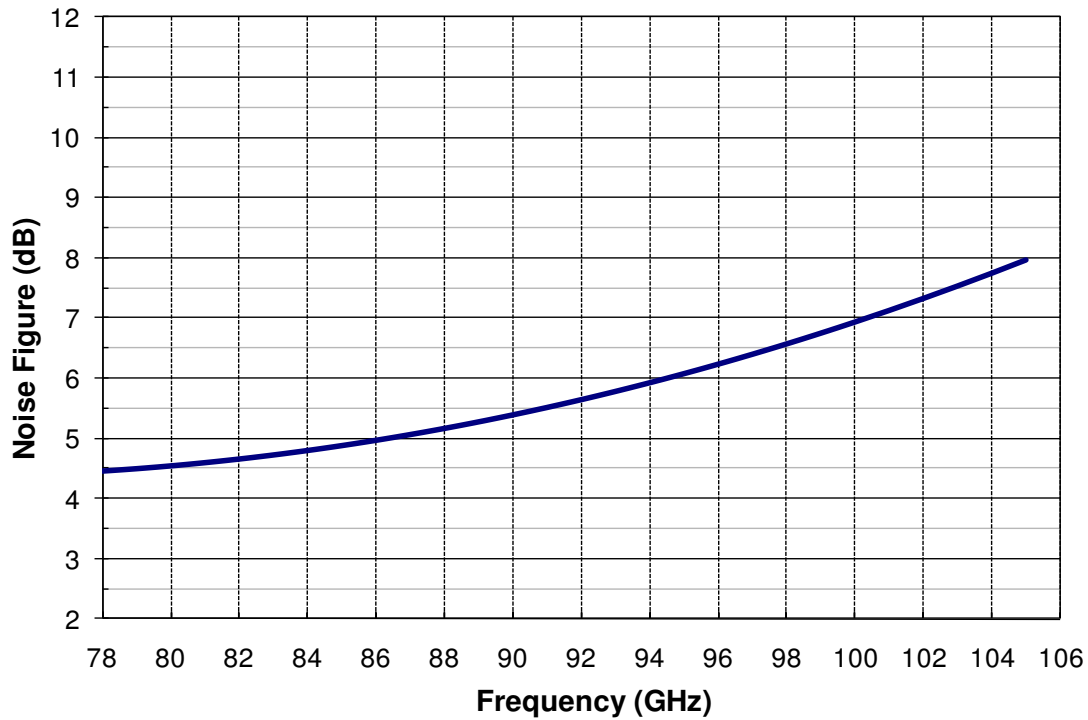
Typical On wafer Measurements

Tamb.= +25°C, VD = 2.5V, ID = 115mA

Linear Gain versus Frequency

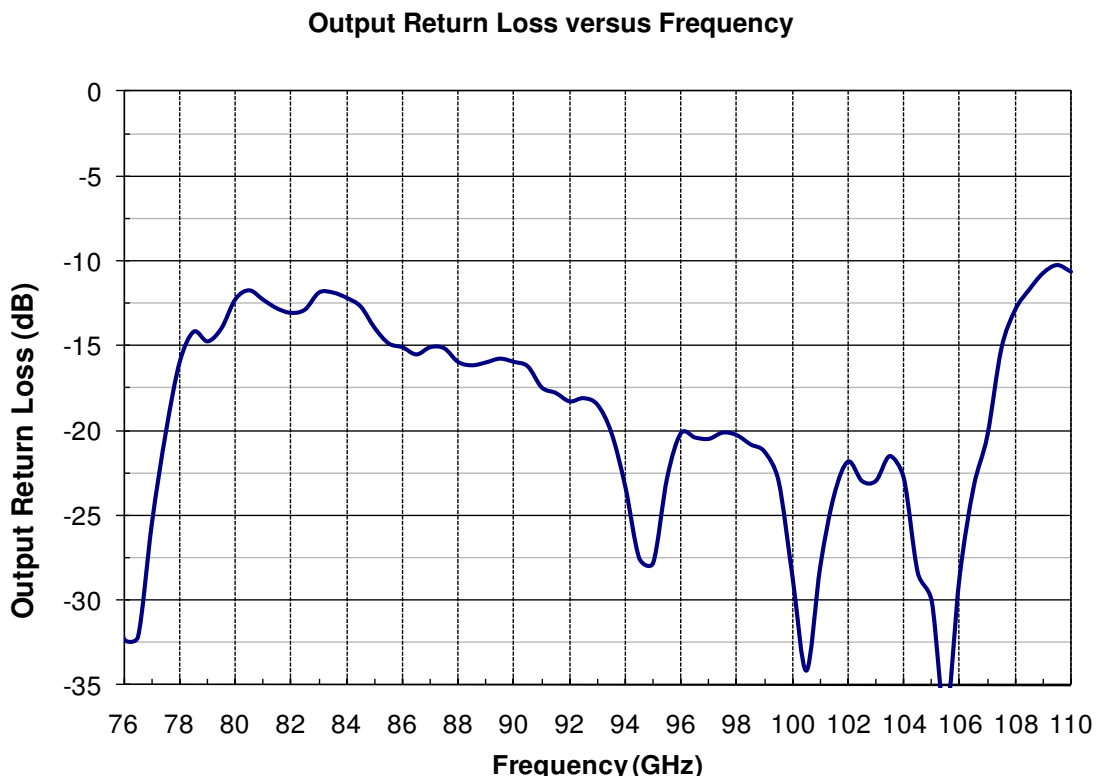
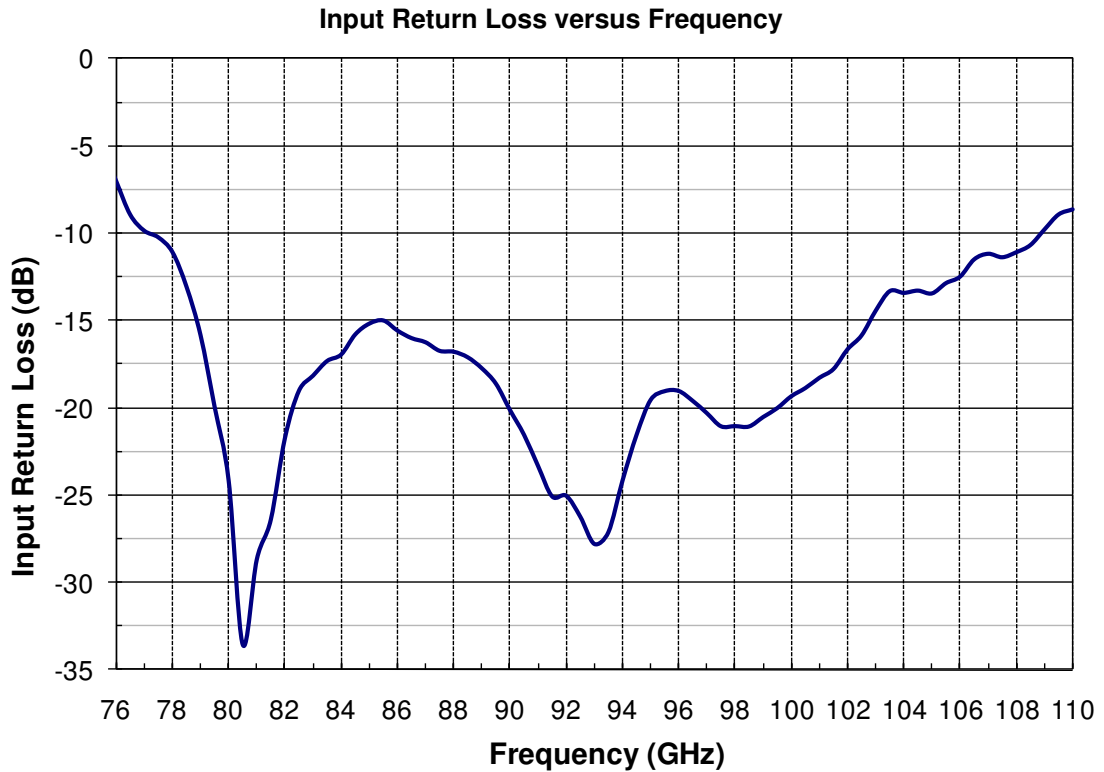


Noise Figure versus Frequency

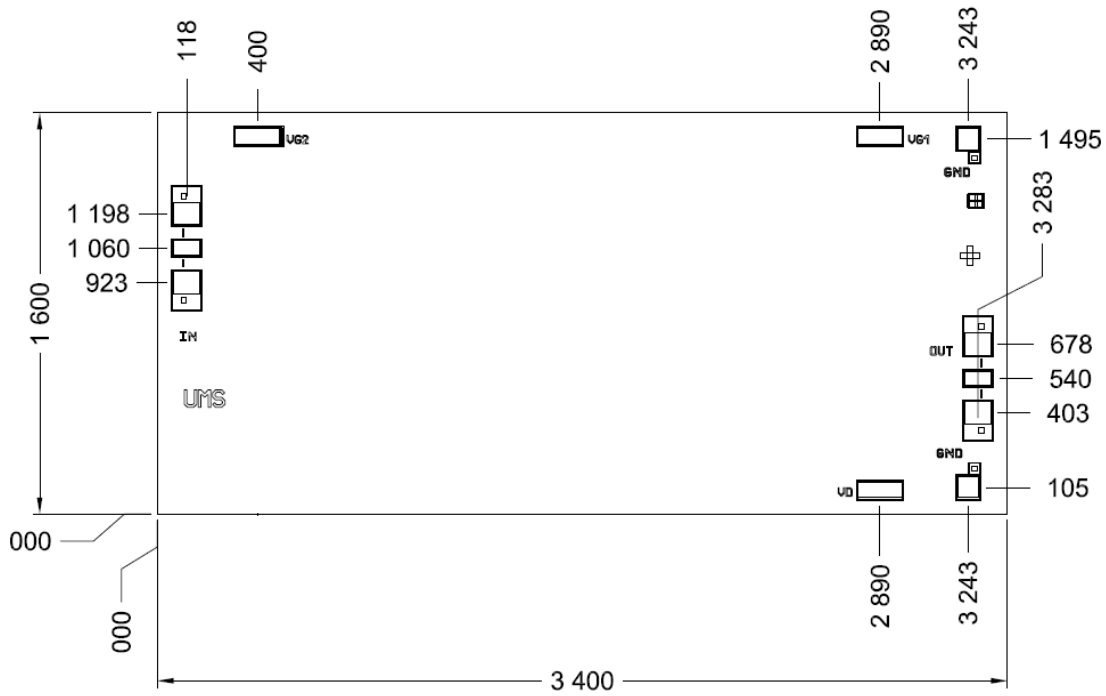


Typical On wafer Measurements

Tamb. = +25°C, VD = 2.5V, ID = 115mA

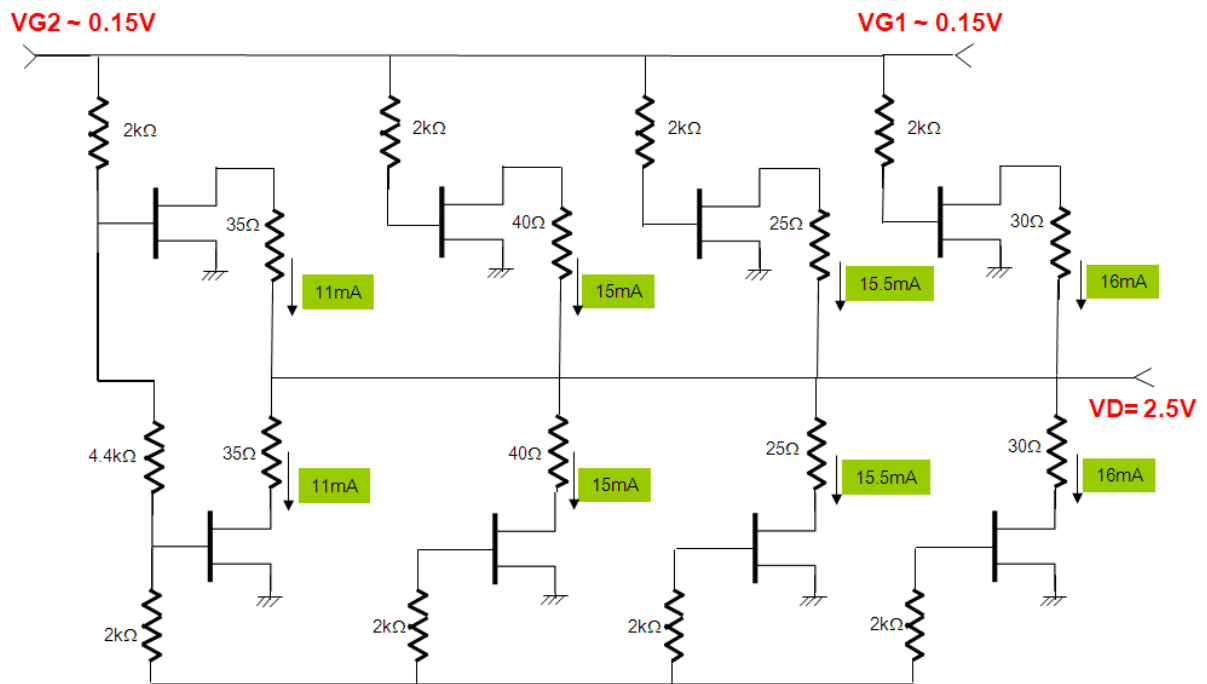


Mechanical data



Chip thickness: 70μm
 DC pad size: 190x80μm
 RF pad size: 122x72μm
 Chip size: 3400x1600 ±35μm
 All dimensions are in micrometers

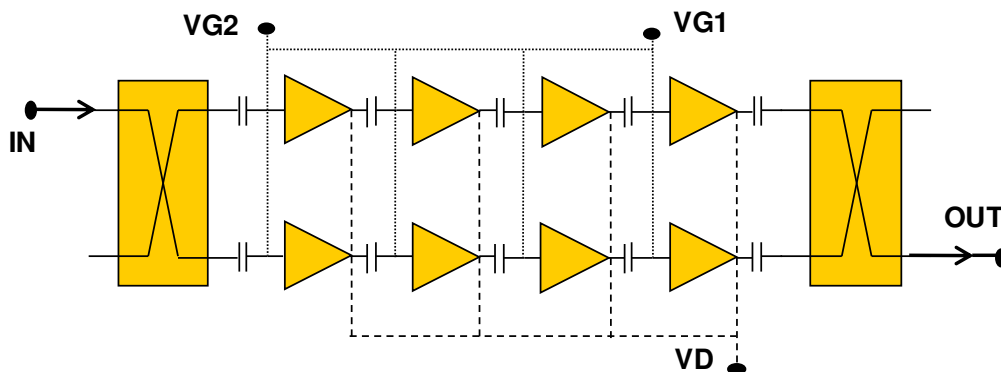
DC Schematic



Notes

VD supply voltage is common for the 4 stages of the amplifier.

VG1 and VG2 pads are linked in the circuit so the gate supply voltage can be apply either on VG1 or VG2.



Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Ordering Information

Chip form: CHA1008-99F/00

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