

55-65GHz Low Noise / Medium Power Amplifier

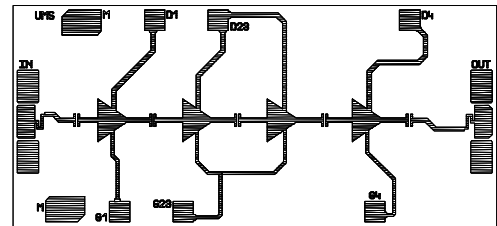
GaAs Monolithic Microwave IC

Description

The CHA2159 is a four - stage low noise and medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This simplifies the assembly process.

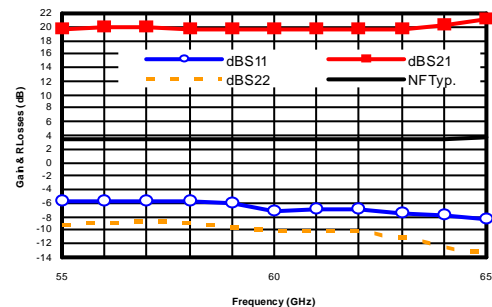
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in chip form.



Main Features

- 4.0 dB noise figure
- 20 dB gain
- 14 dBm output power (-1dB gain comp.)
- DC power consumption, 115mA @ 3.5V
- Chip size: 2.35 x 1.11 x 0.10 mm



Typical on Wafer Measurements

Main Characteristics

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	55		65	GHz
G	Small signal gain	18	20		dB
NF	Noise figure		4.0	4.8	dB
P1dB	Output power at 1dB gain compression	13	14		dBm
Id	Bias current		115	150	mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	55		65	GHz
G	Small signal gain (1)	18	20		dB
ΔG	Small signal gain flatness (1)		±1.0		dB
Is	Reverse isolation (1)	40	50		dB
NF	Noise figure		4.0	4.8	dB
P1dB	CW output power at 1dB compression (1)	13	14		dBm
VSWRin	Input VSWR (1)		2.5:1	4.0:1	
VSWRout	Output VSWR (1)		2.0:1	2.5:1	
Id	Bias current		115	130	mA
Vd	DC Voltage		3.5		V

(1) These values are representative for CW on-wafer measurements that are made without bonding wires at the RF ports.

A wire bond of typically 0.1 to 0.15 nH will improve the input and output matching.

Absolute Maximum Ratings

Tamb = +25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current in linear condition	150	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	0	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

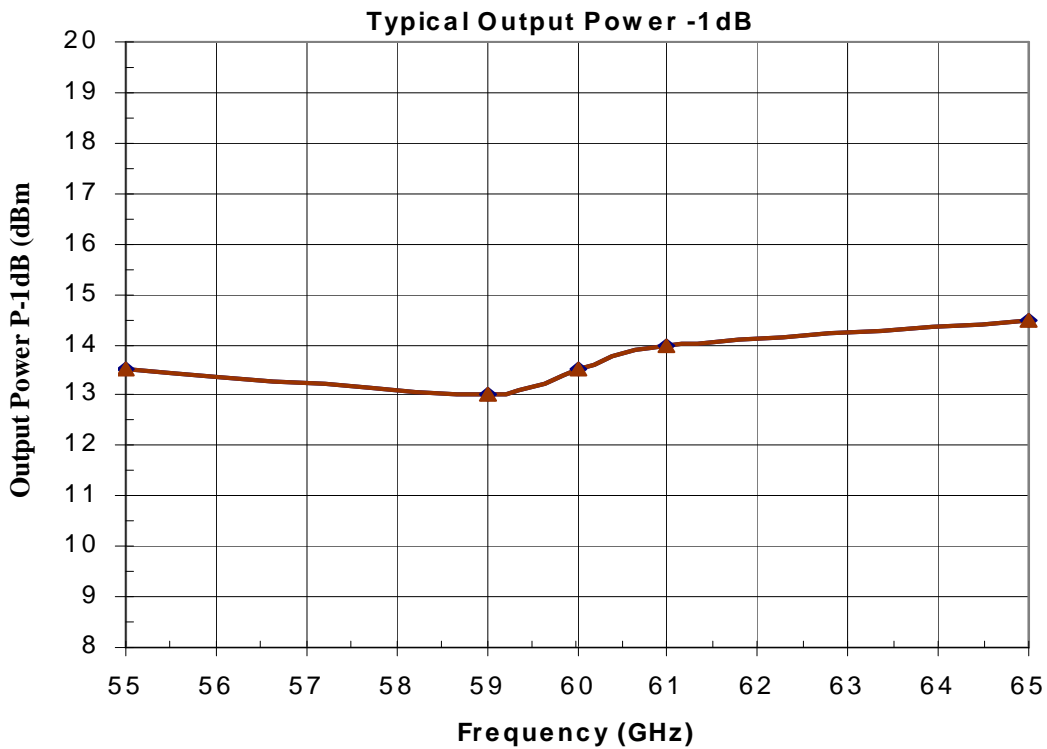
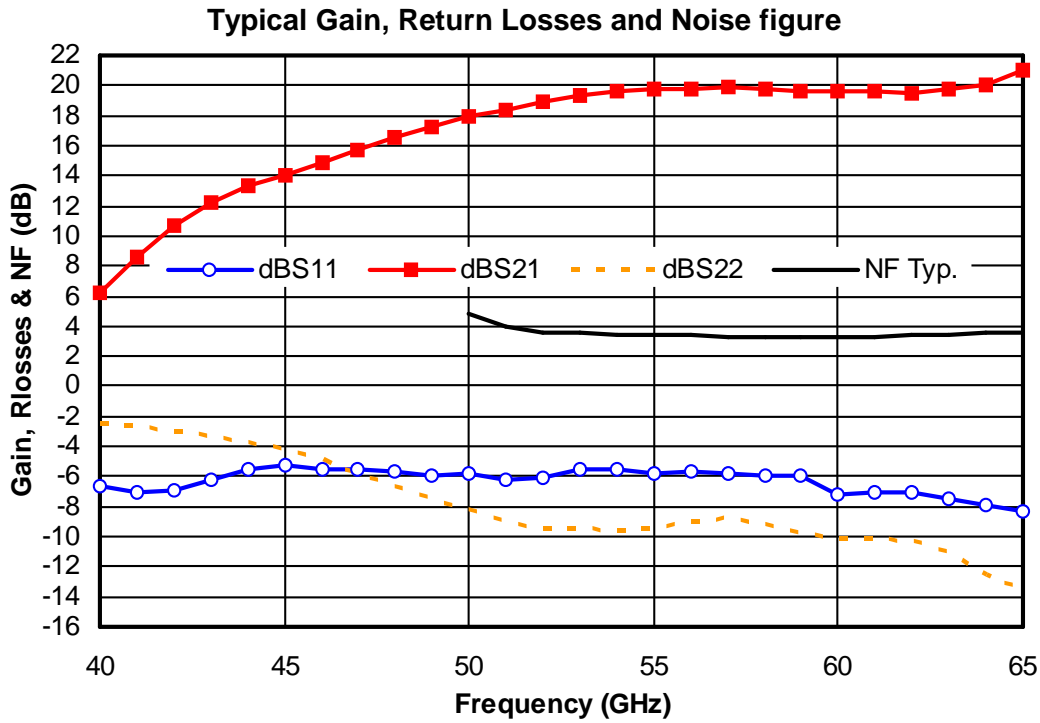
Typical chip on wafer Sij parameters

Bias Conditions: $V_d = +3.5V$, $V_{g1} = V_{g23} = V_{g4}$ adjusted for $I_d = 115mA$

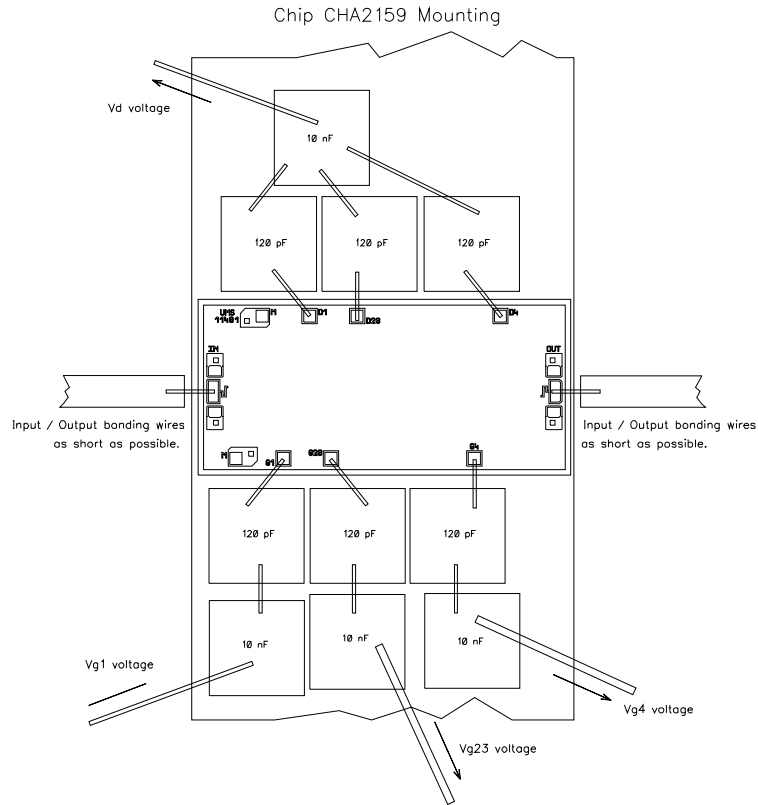
Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P(S21) (°)	dB(S22)	P(S22) (°)
20	-3.6	-168.5	-64.4	166	-8.4	-116	-4.7	-177
21	-3.7	-172.8	-67.3	173	-7.7	-142	-4.5	-180
22	-3.6	-177.5	-62.1	150	-7.4	-168	-4.3	177
23	-3.5	177.6	-58.6	162	-7.1	167	-4.1	174
24	-3.5	172.6	-58.3	146	-6.9	144	-3.8	170
25	-3.5	167.9	-54.5	113	-6.6	122	-3.5	166
26	-3.5	163.2	-57.5	129	-6.5	101	-3.3	161
27	-3.5	158.5	-54.9	106	-6.3	82	-3.1	156
28	-3.5	153.2	-54.9	100	-6.0	62	-2.9	151
29	-3.4	147.9	-53.0	96	-5.7	44	-2.7	146
30	-3.4	142.3	-52.6	88	-5.4	25	-2.7	140
31	-3.4	136.2	-54.4	84	-5.2	7	-2.6	135
32	-3.5	130.0	-51.5	76	-4.8	-10	-2.5	129
33	-3.6	123.7	-50.5	70	-4.4	-25	-2.4	124
34	-3.7	117.5	-49.7	60	-3.9	-40	-2.3	117
35	-3.9	110.8	-50.1	50	-3.2	-54	-2.2	111
36	-4.1	103.7	-48.8	42	-2.2	-66	-2.2	104
37	-4.5	95.9	-49.7	31	-0.7	-78	-2.3	98
38	-4.9	88.5	-49.6	28	1.3	-93	-2.2	90
39	-5.7	81.3	-48.9	10	3.6	-109	-2.3	83
40	-6.6	78.0	-50.3	3	6.2	-131	-2.5	74
41	-7.1	76.7	-49.3	4	8.6	-155	-2.6	66
42	-6.9	76.6	-48.3	-1	10.7	176	-3.0	58
43	-6.2	73.3	-48.5	-18	12.2	146	-3.3	49
44	-5.5	64.0	-48.1	-21	13.3	116	-3.7	41
45	-5.3	53.7	-48.1	-39	14.1	88	-4.1	32
46	-5.5	42.8	-49.8	-49	14.9	61	-4.8	24
47	-5.5	34.2	-50.8	-59	15.8	33	-5.8	17
48	-5.7	24.3	-51.8	-40	16.6	4	-6.6	11
49	-5.9	16.0	-49.8	-52	17.3	-23	-7.5	6
50	-5.9	6.7	-51.2	-42	18.0	-53	-8.2	1
51	-6.2	-0.5	-49.9	-72	18.4	-82	-9.0	-1
52	-6.0	-8.6	-47.8	-68	18.9	-111	-9.4	-4
53	-5.6	-18.2	-47.4	-58	19.4	-141	-9.4	-6
54	-5.5	-31.1	-47.2	-63	19.7	-172	-9.6	-9
55	-5.8	-40.4	-57.2	-91	19.8	157	-9.4	-14
56	-5.7	-50.9	-51.5	-99	19.8	127	-9.1	-20
57	-5.8	-62.2	-48.4	-79	19.9	96	-8.8	-26
58	-5.9	-72.9	-49.5	-91	19.7	65	-9.1	-38
59	-6.0	-84.0	-49.0	-105	19.7	35	-9.7	-43
60	-7.1	-94.9	-44.6	-115	19.6	5	-10.1	-52
61	-7.1	-102.8	-49.7	-141	19.7	-27	-10.1	-57
62	-7.0	-111.9	-44.5	-141	19.5	-59	-10.3	-64
63	-7.5	-122.1	-46.1	-168	19.7	-91	-10.9	-72
64	-7.9	-127.1	-44.5	175	20.1	-124	-12.5	-75
65	-8.3	-137.0	-48.4	167	21.0	-161	-13.4	-69

Typical on Wafer Measurements

Bias conditions: $T_{amb} = +25^{\circ}C$, $V_d = 3.5V$, $V_{g1} = V_{g2} = V_{g3} = V_{g4}$ adjusted for $I_d = 115mA$

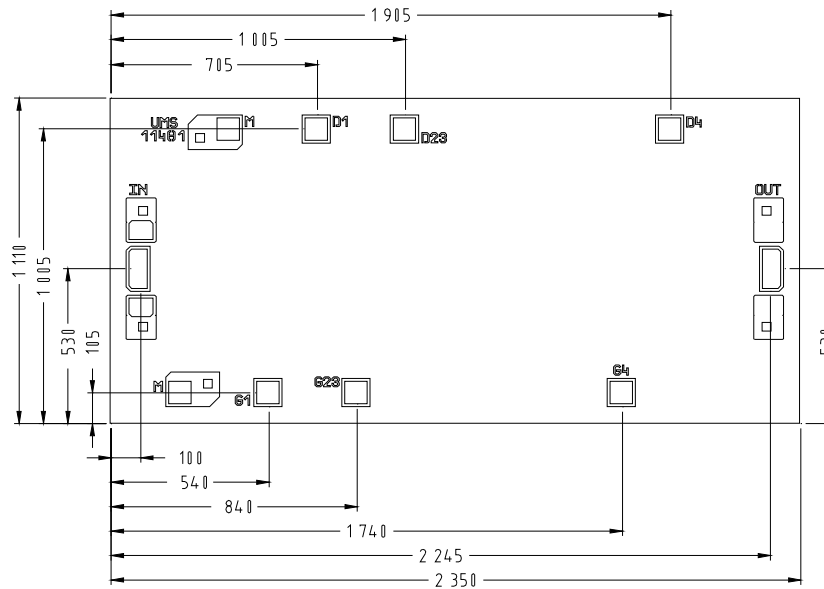


Chip Assembly and Mechanical Data



Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended.

Bonding pad positions



UNITS : µm
Tol : ±35µm

DC Pads size: 100/100 µm, chip thickness: 100µm.

Ordering Information

Chip form : CHA2159-99F/00

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