

34-44GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

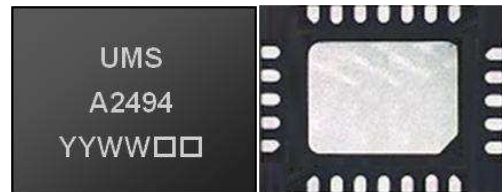
Description

The CHA2494-QEG is a wide band monolithic low noise amplifier.

It is designed for a wide range of applications, from military to commercial communication systems.

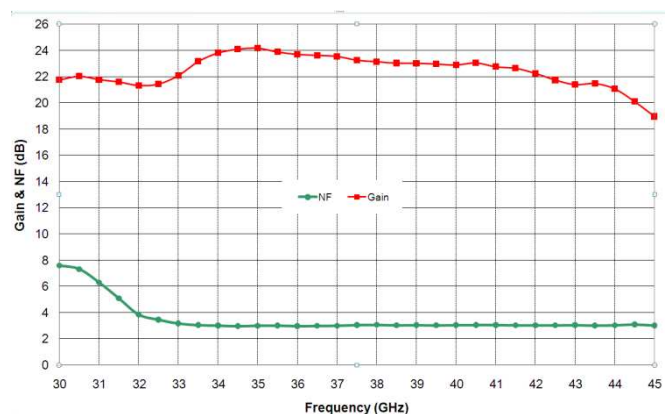
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 34-44GHz
- 3dB noise figure
- 22dB gain
- 20dBm Output IP3
- DC bias: Vd=4V @ Id=80mA
- 24L-QFN4x5
- MSL1



Main Characteristics

Tamb.= +25 °C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	34		44	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		3		dB
OIP3	3 rd order intercept point		20		dBm

Main Characteristics

Tamb.= +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	34		44	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		3		dB
RLlin	Input Return Loss		-8		dB
RLout	Output Return Loss		-10		dB
OIP3	Output 3 rd order intercept point		20		dBm
OP1dB	Output Power @ 1dB comp.		12		dBm
Vg	Gate voltage		-0.45		V
Id	Drain current		80		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Note: Electrostatic discharge sensitive device observe handling precautions!

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Drain bias current	160	mA
Vg	Gate bias voltage	-2 to +0.4	V
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

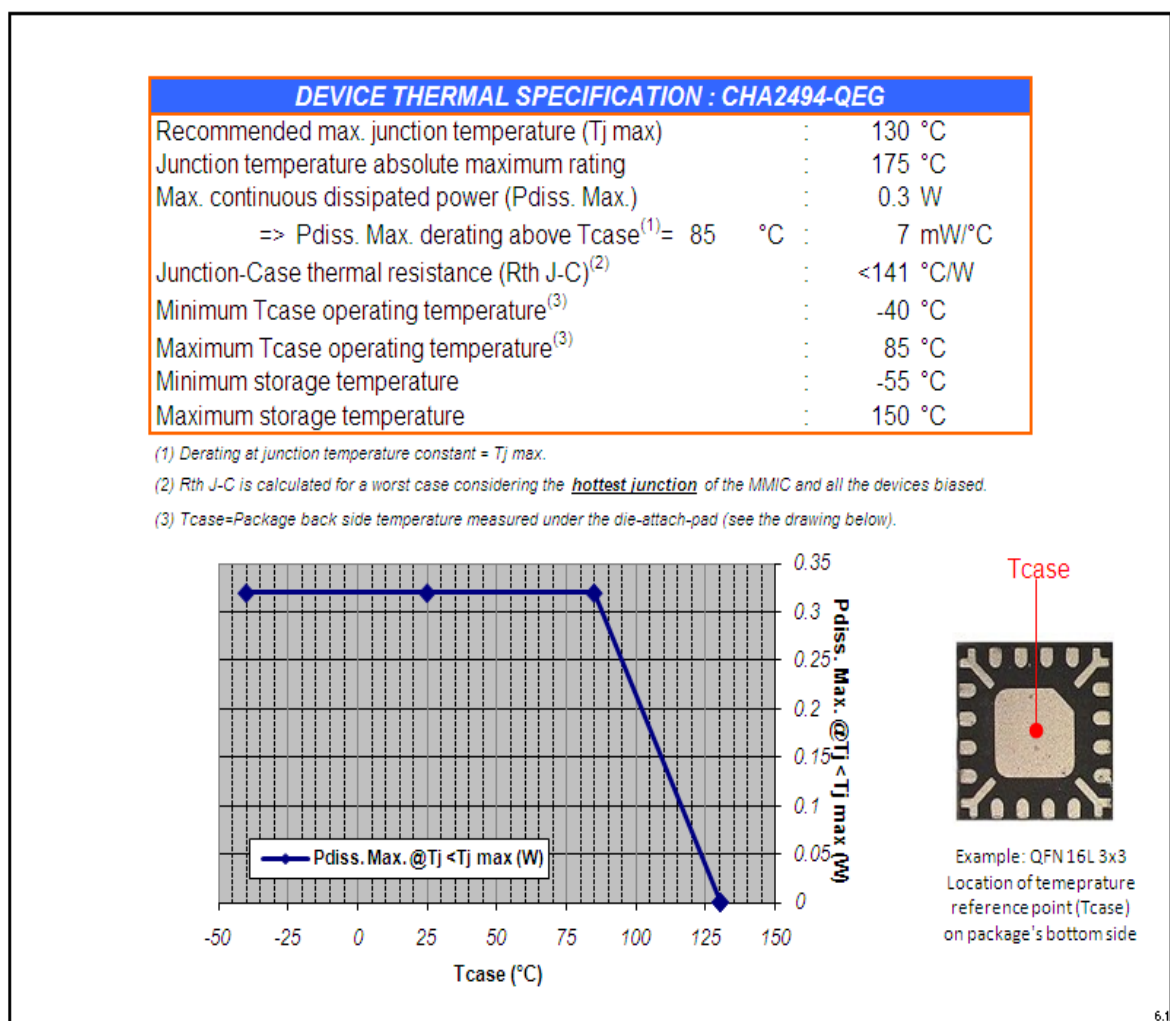
Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd	20	DC drain voltage	4	V
Id	20	DC drain current controlled with Vg	80	mA
Vg	10	DC gate voltage	-0.45	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max}$) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters

Tamb.= +25°C, Vd = +4V, Id = 80mA

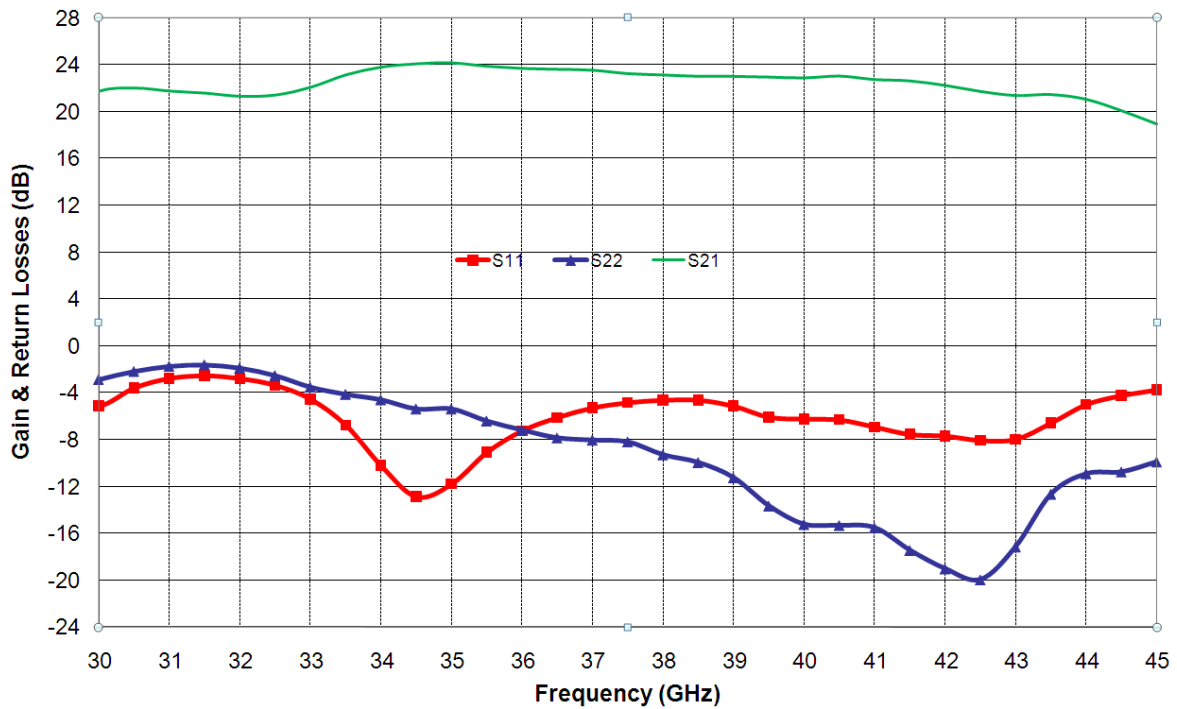
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-0.81	141.00	-76.35	75.37	-68.03	20.33	-0.91	140.50
3.0	-1.18	118.30	-69.72	2.81	-61.16	-103.80	-2.04	116.40
4.0	-2.48	90.35	-65.74	19.77	-52.75	138.10	-5.58	97.95
5.0	-6.07	59.86	-66.78	23.61	-54.50	39.57	-7.58	109.50
6.0	-13.90	54.47	-69.24	-10.67	-69.43	34.28	-5.84	106.20
7.0	-13.68	100.70	-62.22	23.39	-55.04	58.11	-4.83	91.20
8.0	-9.70	94.38	-67.57	-20.04	-50.78	7.38	-4.39	74.01
9.0	-7.86	76.91	-62.64	-16.79	-49.28	-50.35	-4.22	55.97
10.0	-6.84	57.13	-67.32	-29.04	-47.62	-92.94	-4.15	37.22
11.0	-6.32	40.46	-63.73	-47.97	-46.16	-145.20	-4.17	19.82
12.0	-6.04	25.17	-58.87	-100.50	-46.05	165.40	-4.21	2.94
13.0	-5.76	12.01	-57.19	-158.20	-42.69	132.70	-4.34	-13.63
14.0	-5.46	-4.82	-58.46	176.90	-40.82	107.00	-4.52	-29.46
15.0	-5.86	-16.73	-55.08	116.20	-35.82	71.74	-4.72	-44.98
16.0	-5.98	-26.52	-54.55	95.35	-31.67	27.60	-5.03	-60.00
17.0	-5.79	-35.65	-53.52	52.78	-29.34	-18.21	-5.30	-74.67
18.0	-5.40	-46.27	-58.29	149.80	-27.44	-51.99	-5.71	-89.70
19.0	-4.77	-57.68	-50.49	129.40	-24.21	-87.72	-6.18	-104.00
20.0	-4.18	-72.42	-51.14	64.14	-21.51	-122.40	-6.64	-116.90
21.0	-3.67	-88.96	-48.17	53.89	-19.17	-158.60	-6.85	-129.40
22.0	-3.26	-105.90	-46.52	53.16	-16.65	172.40	-7.01	-143.20
23.0	-2.92	-122.50	-48.59	49.40	-13.61	146.50	-7.06	-158.40
24.0	-2.63	-140.20	-47.36	27.54	-10.45	117.80	-7.67	-174.80
25.0	-2.34	-158.20	-45.58	23.69	-6.63	92.33	-9.21	172.90
26.0	-2.15	-174.40	-44.63	8.87	-1.84	64.37	-11.65	172.90
27.0	-2.19	169.30	-40.77	2.51	3.42	30.73	-9.93	-167.80
28.0	-2.32	151.20	-43.87	13.22	9.55	-9.21	-6.13	-176.00
29.0	-3.23	134.80	-39.07	-22.84	16.42	-62.55	-4.37	167.90
30.0	-5.04	135.10	-40.07	-54.83	21.12	-142.40	-3.35	151.80
31.0	-3.33	126.50	-42.76	-77.96	21.18	147.60	-2.72	133.60
32.0	-3.24	108.90	-41.12	-64.78	20.95	93.19	-2.73	114.80
33.0	-4.98	85.88	-39.54	-90.93	21.56	46.46	-4.06	98.21
34.0	-10.59	71.51	-42.96	-127.40	23.52	-5.46	-5.55	94.85
35.0	-11.52	123.20	-43.92	-91.98	23.67	-64.94	-5.88	82.61
36.0	-7.01	123.20	-40.06	-110.50	23.05	-115.90	-6.40	77.98
37.0	-5.68	105.00	-41.73	-96.54	22.62	-164.30	-7.55	76.98
38.0	-5.39	85.28	-41.08	-116.00	22.37	150.30	-8.54	67.00
39.0	-5.67	65.19	-43.16	-138.80	22.27	104.40	-10.32	51.85
40.0	-6.91	58.36	-42.74	-137.00	22.37	58.32	-12.74	61.19
41.0	-7.31	31.63	-39.90	-155.20	22.41	7.07	-11.21	70.58
42.0	-7.51	-11.40	-39.95	-125.80	21.52	-45.05	-12.89	72.65
43.0	-8.42	-75.28	-36.11	-153.40	20.31	-90.70	-14.31	71.80
44.0	-6.14	-144.60	-34.80	140.90	20.38	-141.90	-12.14	100.00
45.0	-4.18	170.00	-34.34	163.90	18.81	161.70	-10.15	106.40

Typical Board Measurements

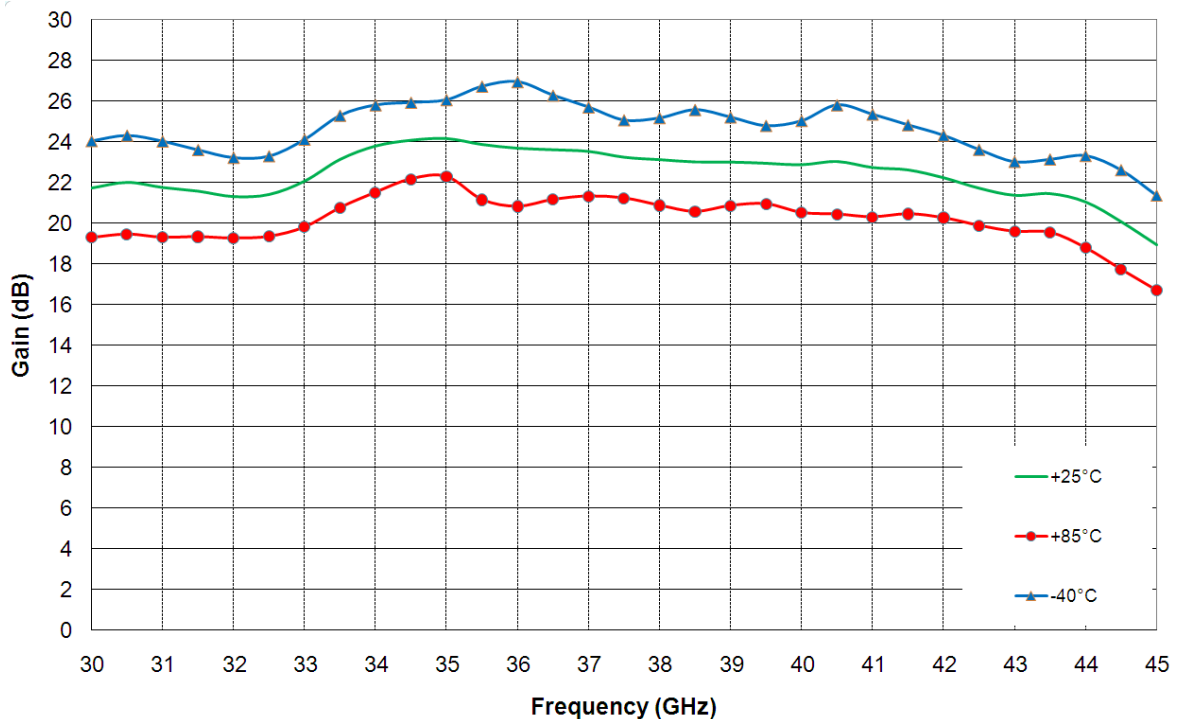
Tamb = +25°C, Tcold = -40°C, That = +85°C, Vd = +4V, Id = 80mA

The following values are representative of onboard measurements, on QFN access planes.

Gain & Return Losses at ambient temperature



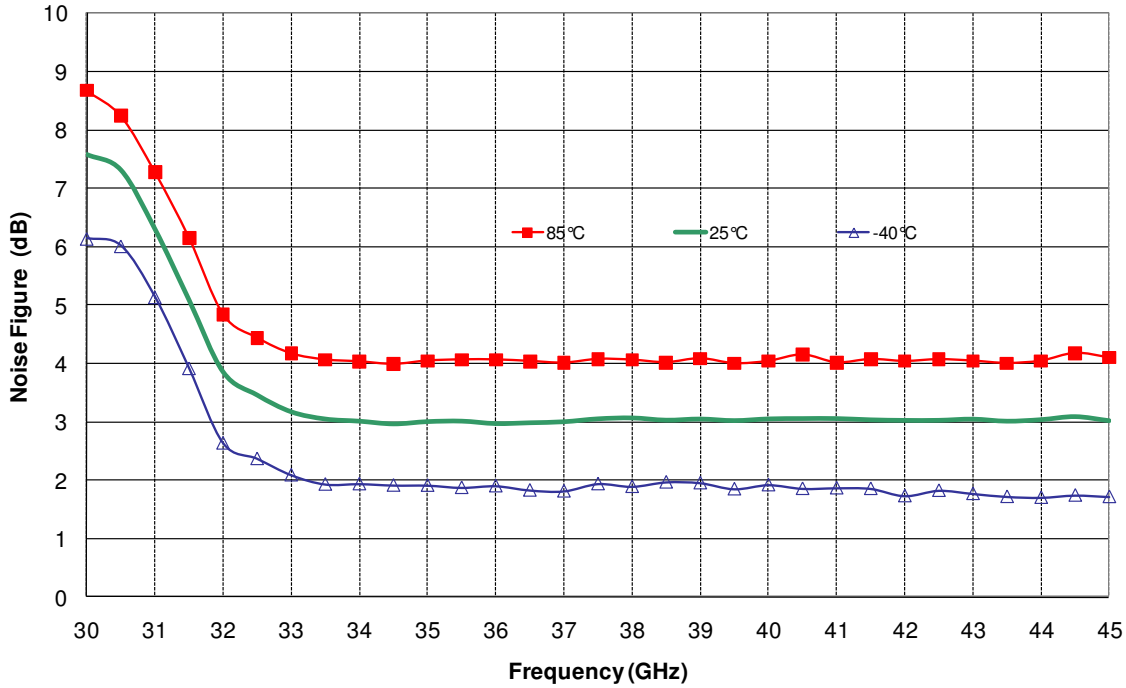
Gain versus temperature



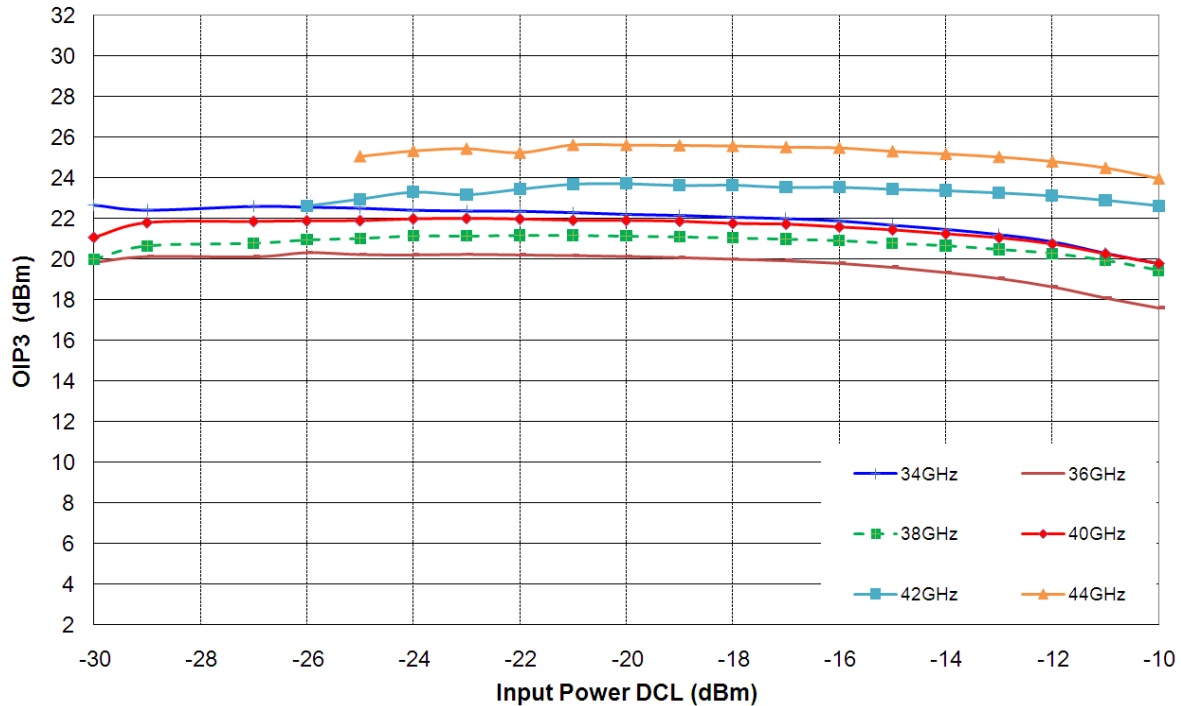
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C, Vd = +4V, Id = 80mA

Noise figure versus temperature



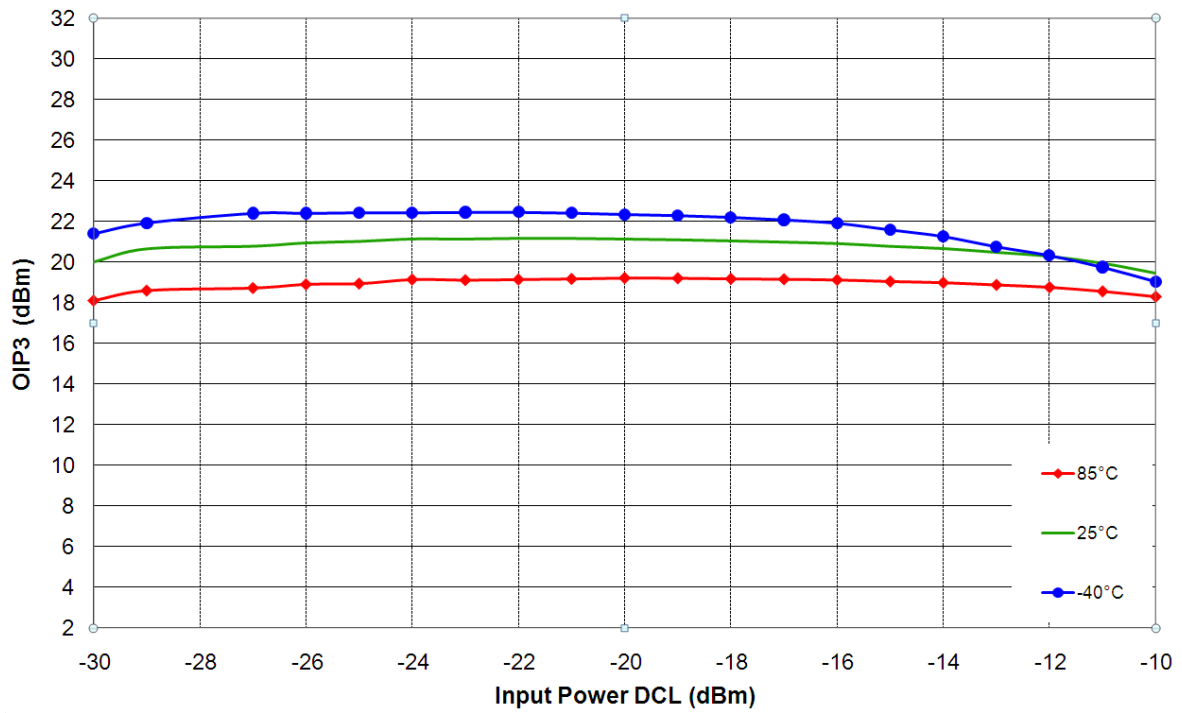
Output IP3 versus frequency and input power at ambient temperature



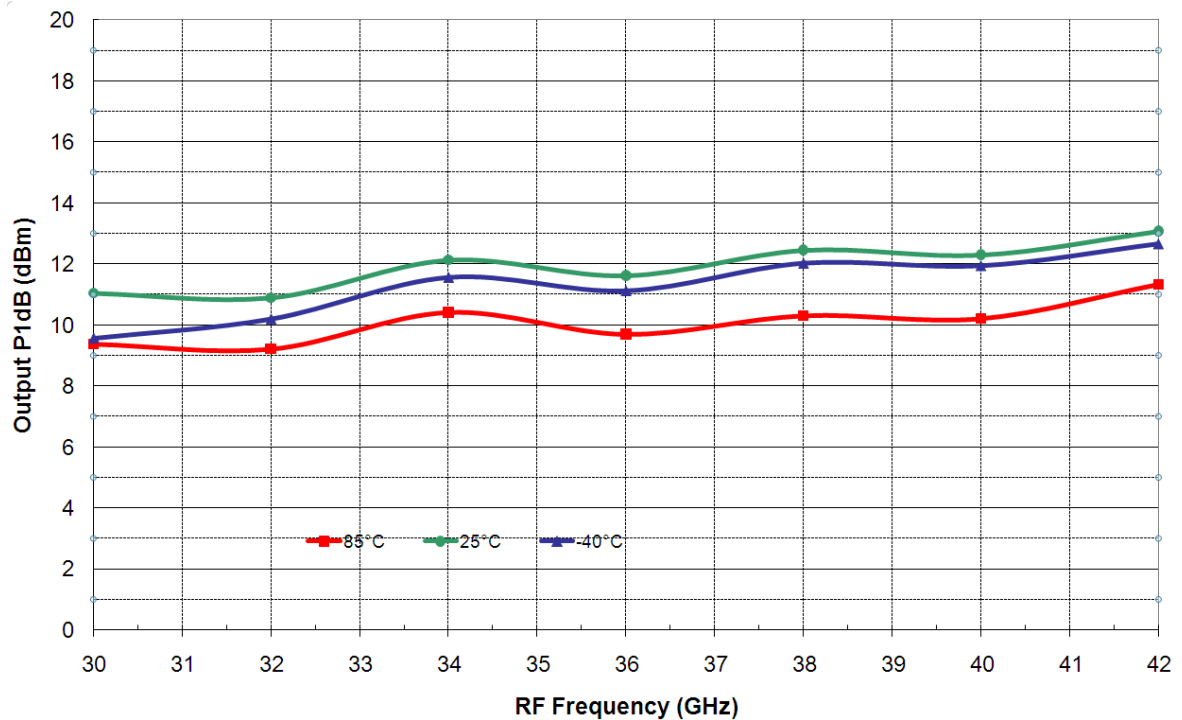
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C, Vd = +4V, Id = 80mA

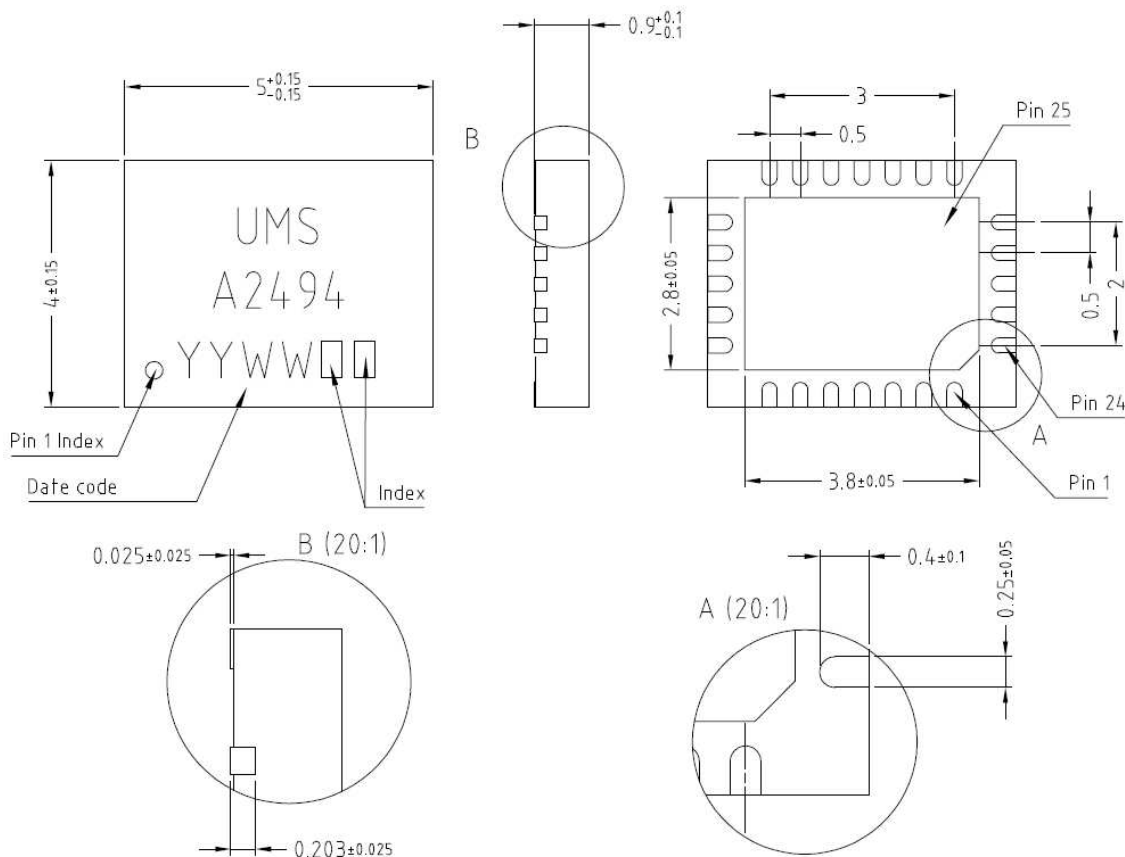
Output IP3 at 38GHz versus temperature and input power



Output Power @ 1dB comp. versus temperature and frequency



Package outline ⁽¹⁾



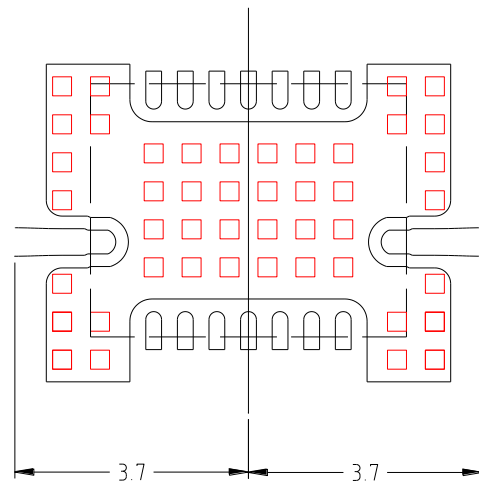
Matt tin, Lead Free (Green)		1- Nc	9- Nc	17- Nc
Units : mm		2- Nc	10- Vg	18- Nc
From the standard : JEDEC MO-220 (VGGD)		3- Nc	11- Gnd ⁽²⁾	19- Nc
		4- Gnd ⁽²⁾	12- Nc	20- Vd
	25- GND	5- RF out	13- Nc	21- Nc
		6- Gnd ⁽²⁾	14- Gnd ⁽²⁾	22- Nc
		7- Nc	15- RF in	23- Nc
		8- Nc	16- Gnd ⁽²⁾	24- Nc

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

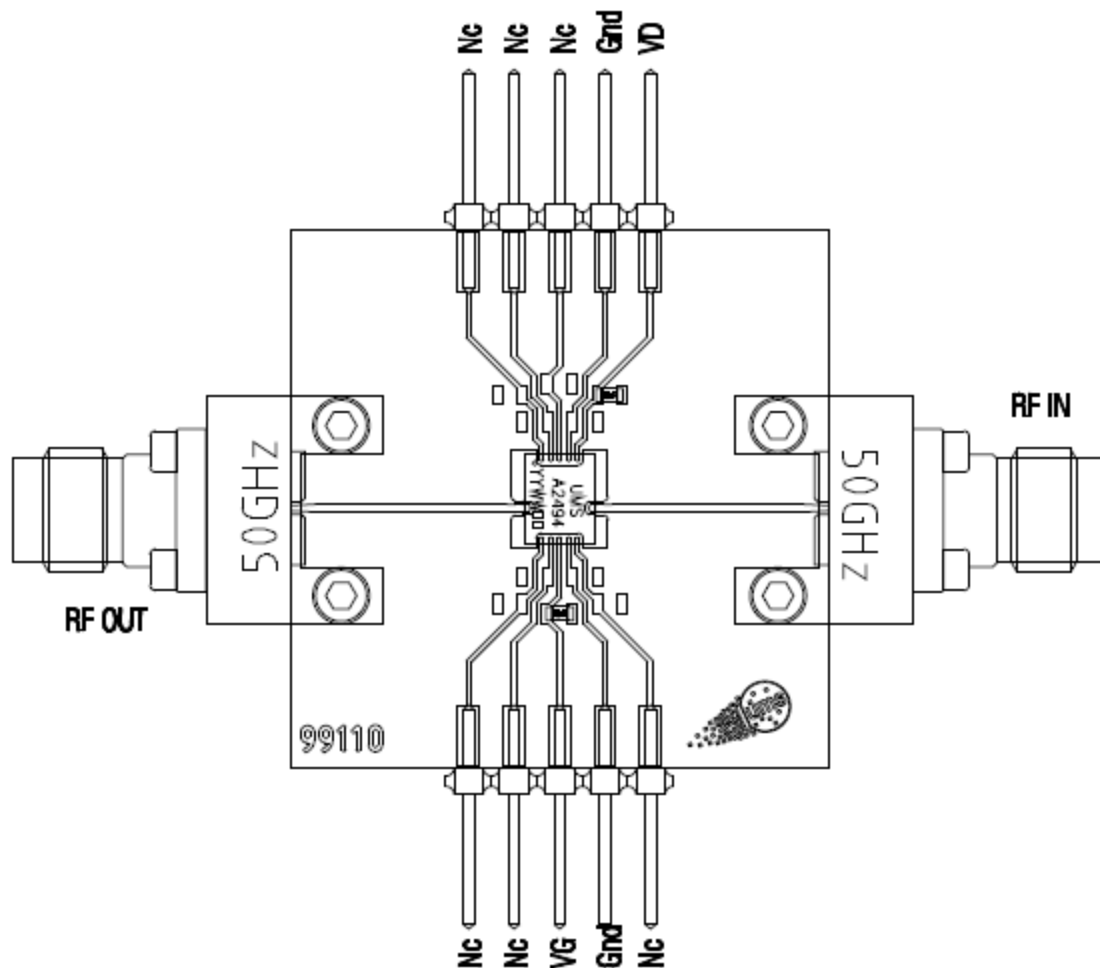
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.7mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



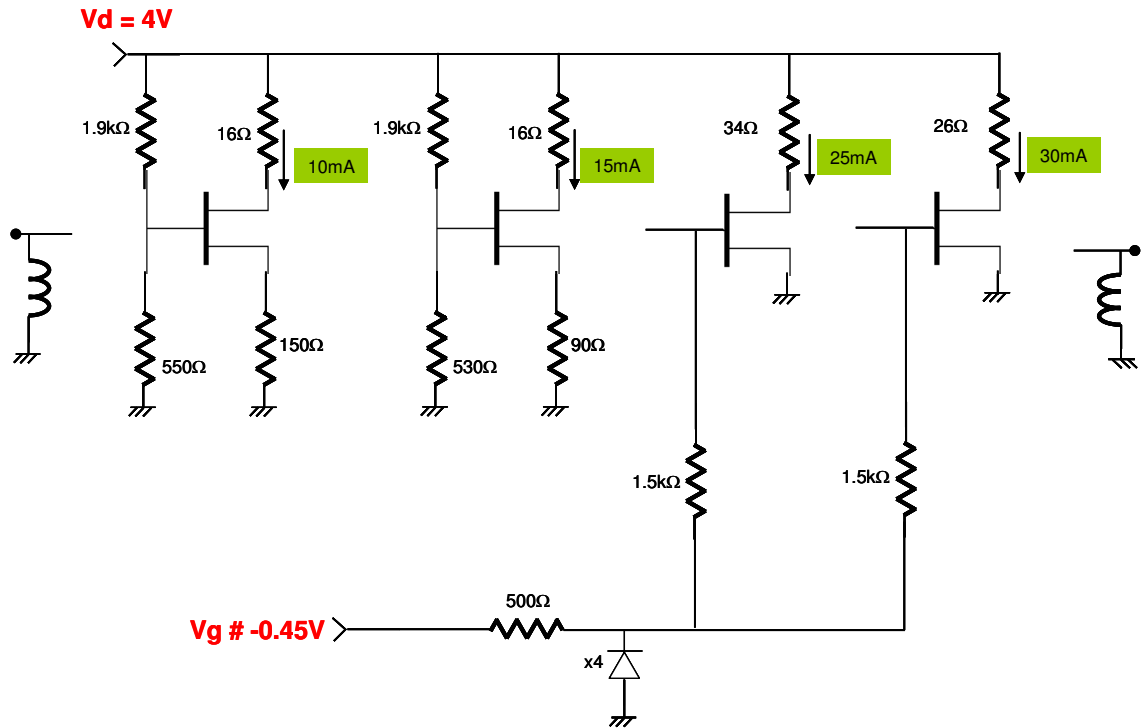
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.



DC Schematic

LNA: 4V, 80mA



Notes

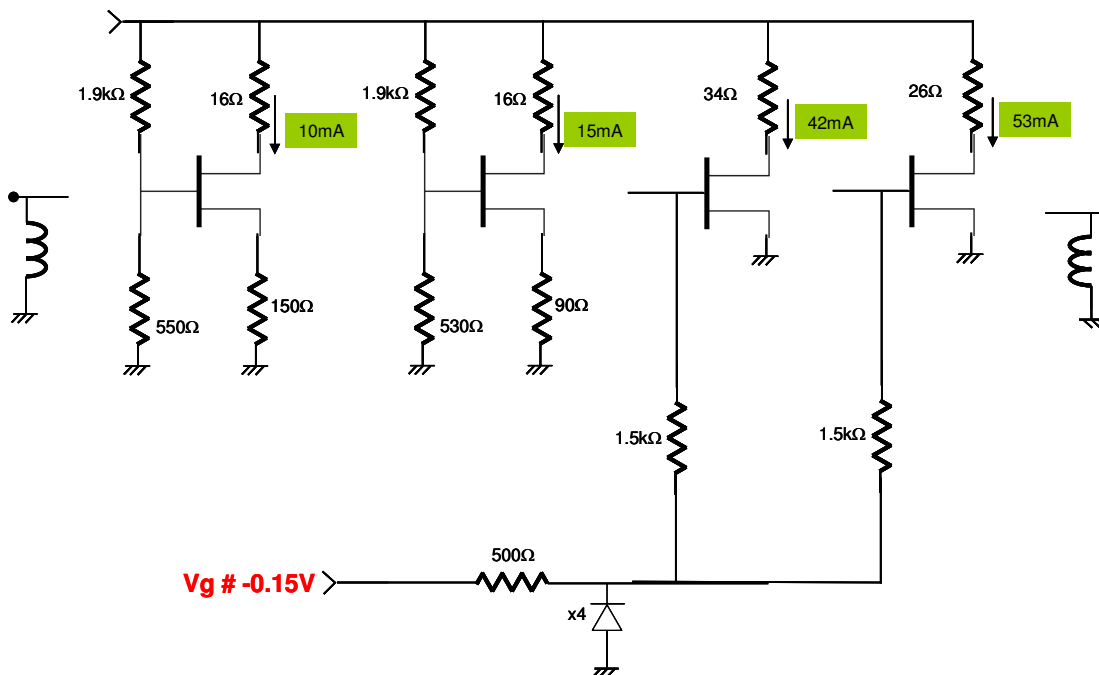
1) Other Bias Conditions:

Symbol	Pad N°	Parameter	Values	Unit
Vd	20	DC drain voltage	4	V
Id	20	DC drain current controlled with Vg	120	mA
Vg	10	DC gate voltage	-0.15	V

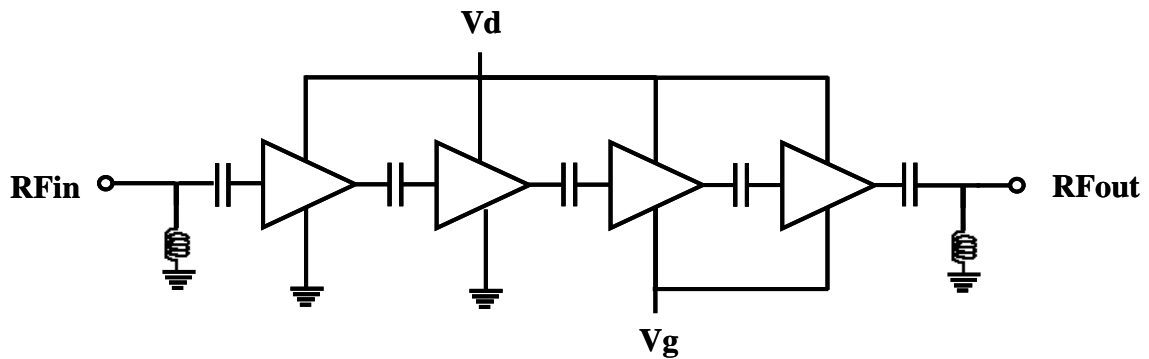
Main characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	34		44	GHz
Gain	Linear Gain		24		dB
NF	Noise Figure		3		dB
OIP3	3 rd order intercept point		22		dBm

DC Schematic



- 2) Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections is also implemented on gate access common to 3rd and 4th stage (1st and 2nd stage are self-biased).

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 package:

CHA2494-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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