

## X-band High Power Amplifier

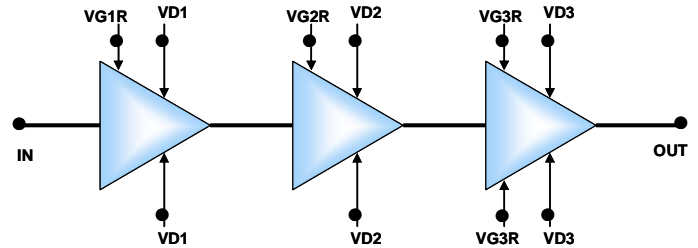
### GaAs Monolithic Microwave IC

#### Description

The CHA7215 is a monolithic three-stage GaAs high power amplifier designed for X band applications.

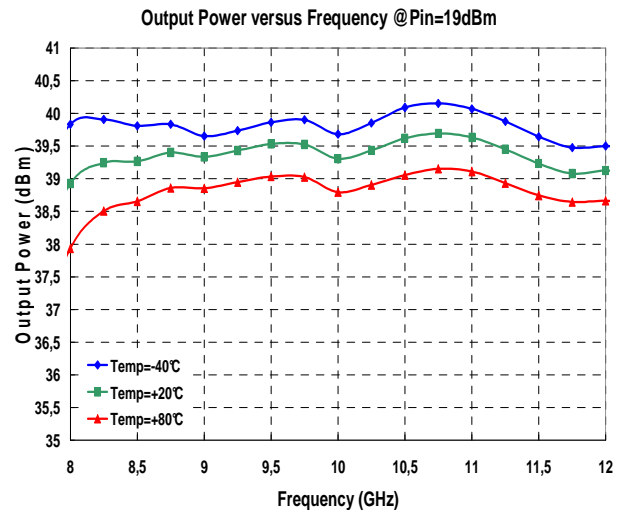
The HPA provides typically 9W output power associated to 35% power added efficiency at 4dBc and a high robustness on mismatch load.

This device is manufactured using 0.25  $\mu\text{m}$  Power pHEMT process, including, via holes through the substrate and air bridges.



#### Main Features

- 0.25  $\mu\text{m}$  Power pHEMT Technology
- Frequency band: 8.5 – 11.5GHz
- Output power: 39.5dBm at saturation
- High linear gain: 28dB
- Power added efficiency: 34% @4dBc
- Quiescent bias point:  $V_d=8\text{V}$ ,  $I_d=2.3\text{A}$
- Chip size: 5 x 3.31 x 0.07mm



#### Main Characteristics

$V_d=8\text{V}$ ,  $I_d$  (Quiescent) = 2.3A, Drain Pulse width = 25 $\mu\text{s}$ , Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Top	Operating temperature range	-40		+80	$^{\circ}\text{C}$
Fop	Operating frequency range	8.5		11.5	GHz
PAE_4dBc	Power added efficiency @4dBc @ 20 $^{\circ}\text{C}$		34		%
Psat	Saturated output power @ 20 $^{\circ}\text{C}$		39.5		dBm
G	Small signal gain @ 20 $^{\circ}\text{C}$	25	28	31	dB

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!

## Electrical Characteristics on test fixture

Tamb = 20°C, Vd=8V, Id (Quiescent) = 2.3A, Drain Pulse width = 25µs, Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency	8.5		11.5	GHz
G	Small signal gain	25	28	31	dB
G_T	Small signal gain variation versus temperature		-0.05		dB/°C
RLin	Input Return Loss		10		dB
RLout	Output Return Loss		12		dB
Psat	Saturated output power		39.5		dBm
Psat_T	Saturated output power variation versus temperature		-0.01		dB/°C
PAE_4dBc	Power added efficiency @4dBc		34		%
Id_4dBc	Supply drain current @ 4dBc		3.3	4.4	A
Vd1, Vd2, Vd3	Drain supply voltage (2)		8		V
Id	Supply quiescent current (1)		2.3		A
Vg1, Vg2, Vg3	Gate supply voltage		-2.2		V

- (1) Parameter can be adjusted by tuning of Vg.
- (2) 0.5V variation on Vd leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings)

## Absolute Maximum Ratings (1)

Tamb = 20°C

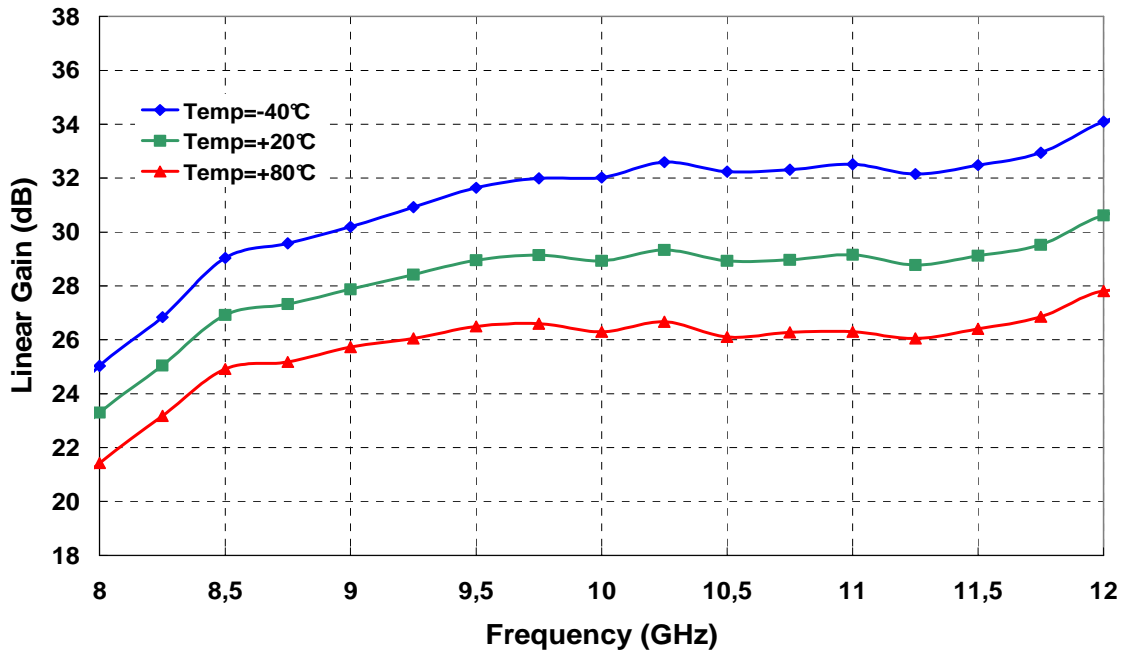
Symbol	Parameter	Values	Unit
Cmp	Compression level (2)	6	dBc
Vd	Supply voltage with RF input power	9	V
Vd	Supply voltage without RF input power	10	V
Id	Supply quiescent current	3	A
Id_sat	Supply current in saturation	4.8	A
Vg	Supply voltage	-1.1	V
Tj	Maximum junction temperature	175	°C
Tstg	Storage temperature range	-55 to +125	°C
Top	Operating temperature range	-40 to +80	°C

- (1) Operation of this device above anyone of these parameters may cause permanent damage.
- (2) For higher compression the level limit can be increased by decreasing the voltage Vd using the rate 0.5 V / dBc

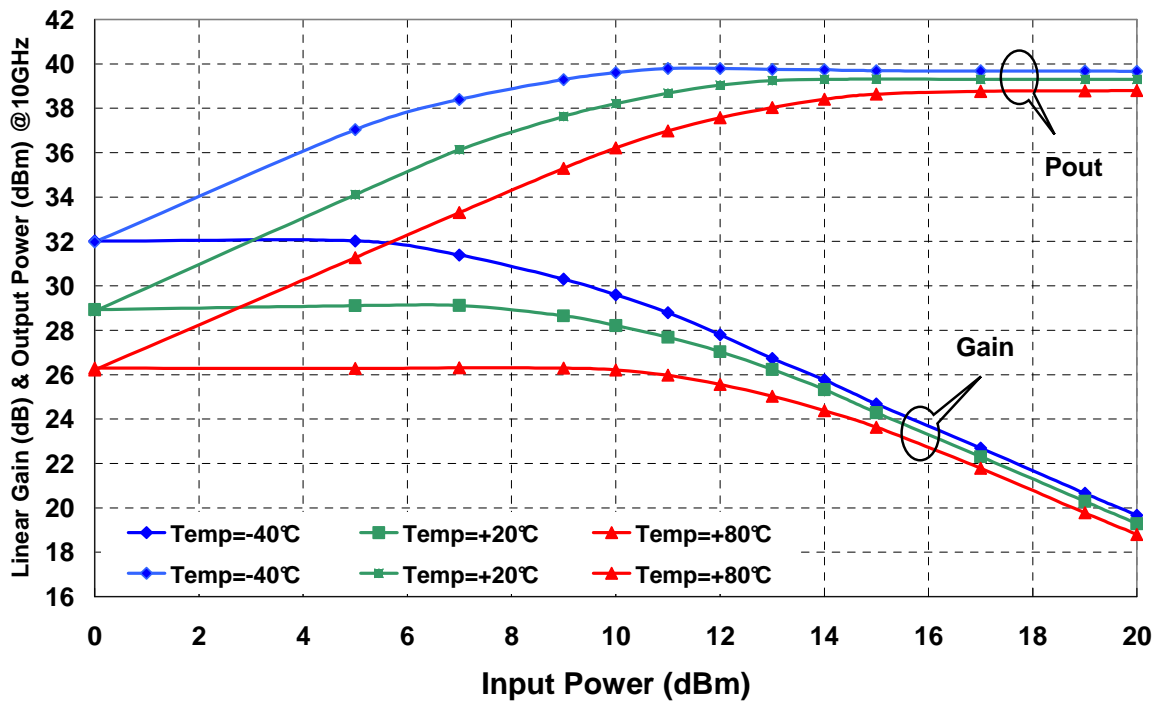
Typical measured characteristics

Measurements on Jig:

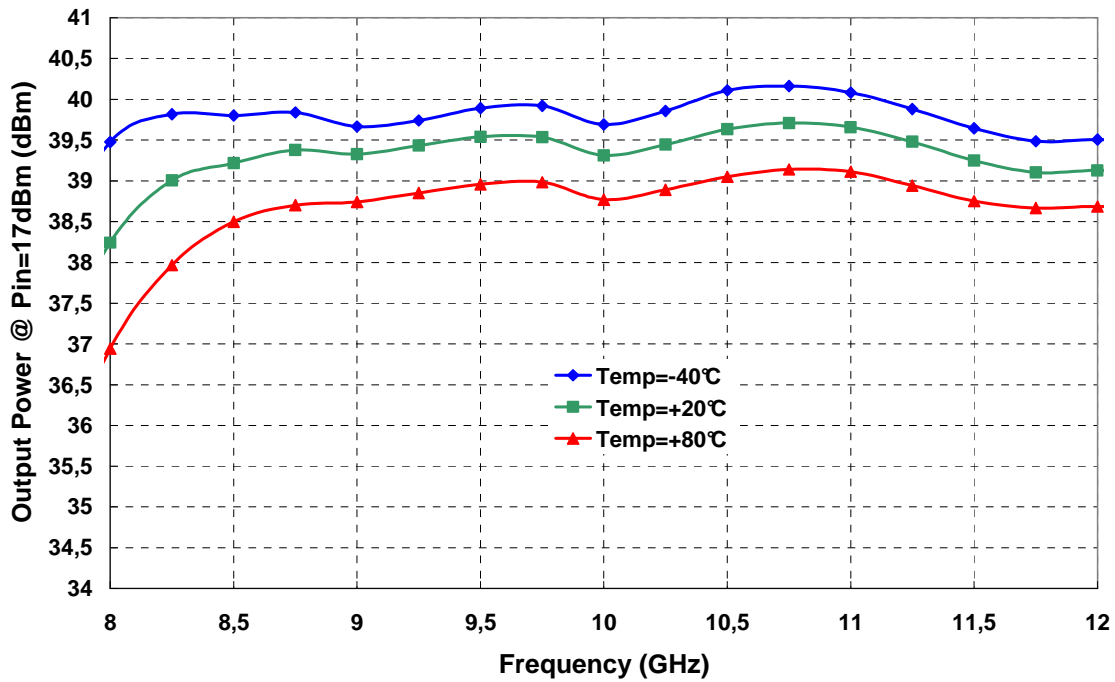
Vd=8V, Id (Quiescent) = 2.3A, Drain Pulse width = 25µs, Duty cycle = 10%



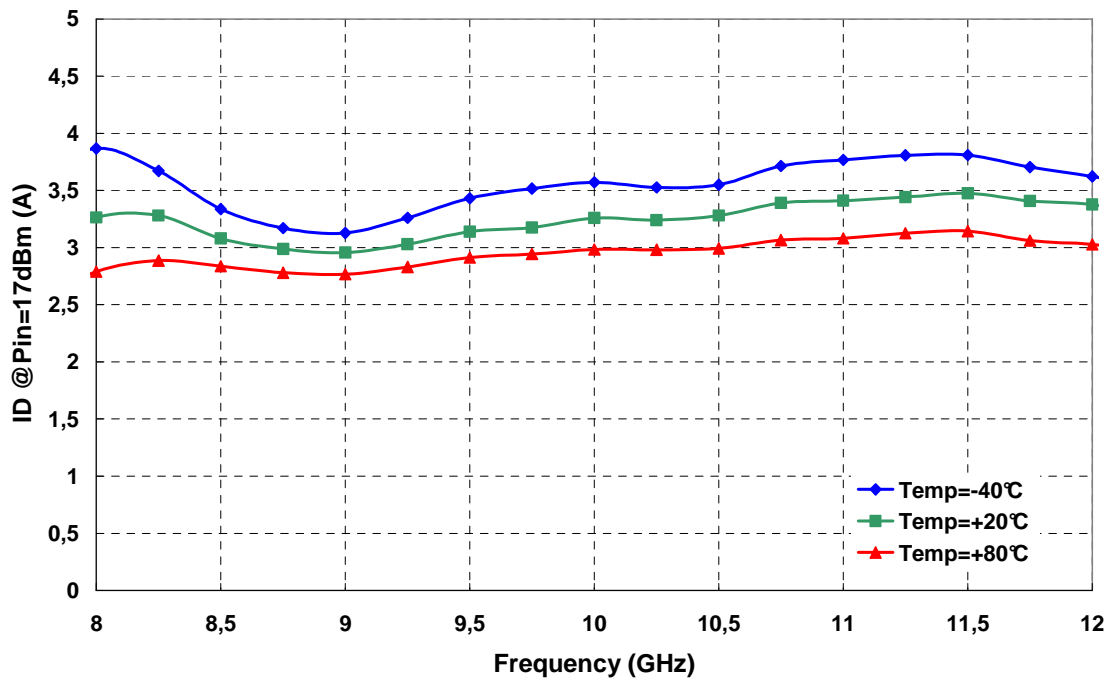
Linear gain versus frequency and temperature



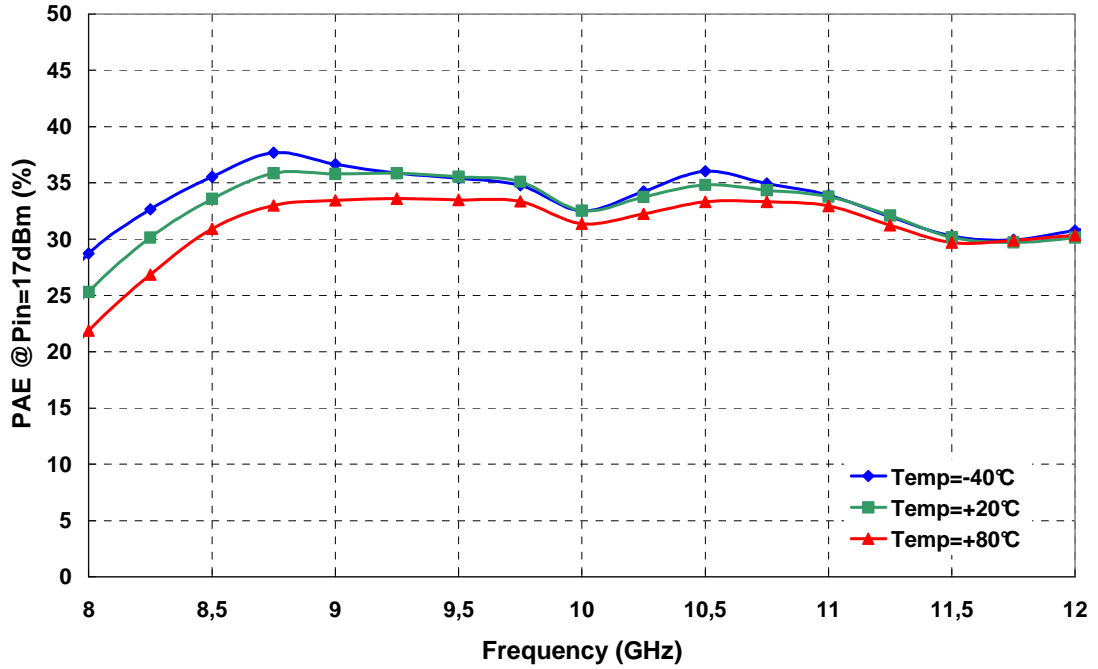
Linear Gain and Output Power @ Freq=10GHz versus input power and temperature



**Output Power @Pin=17dBm versus frequency and temperature**

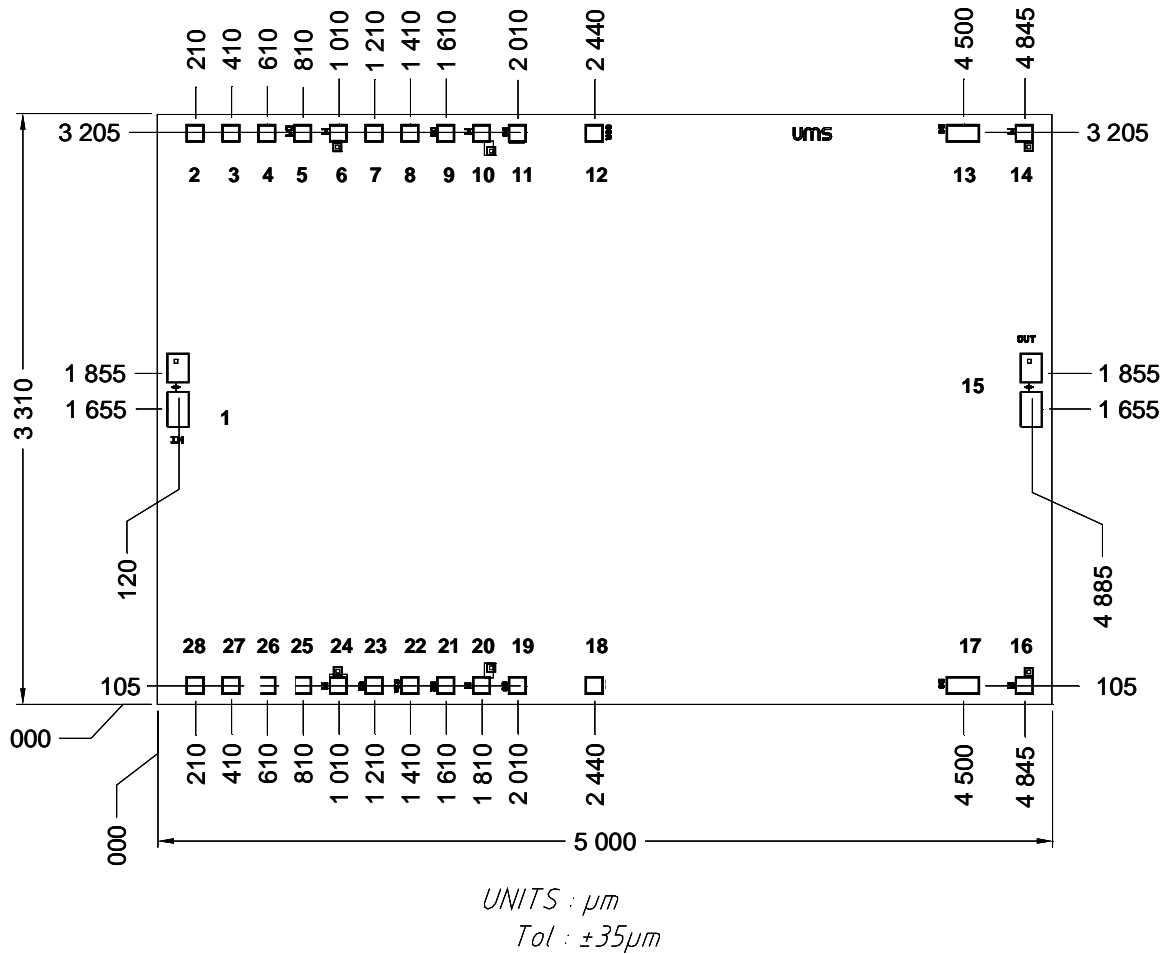


**Id @Pin=17dBm versus frequency and temperature**



*PAE @Pin=17dBm versus frequency and temperature*

## Chip Mechanical Data and Pin references



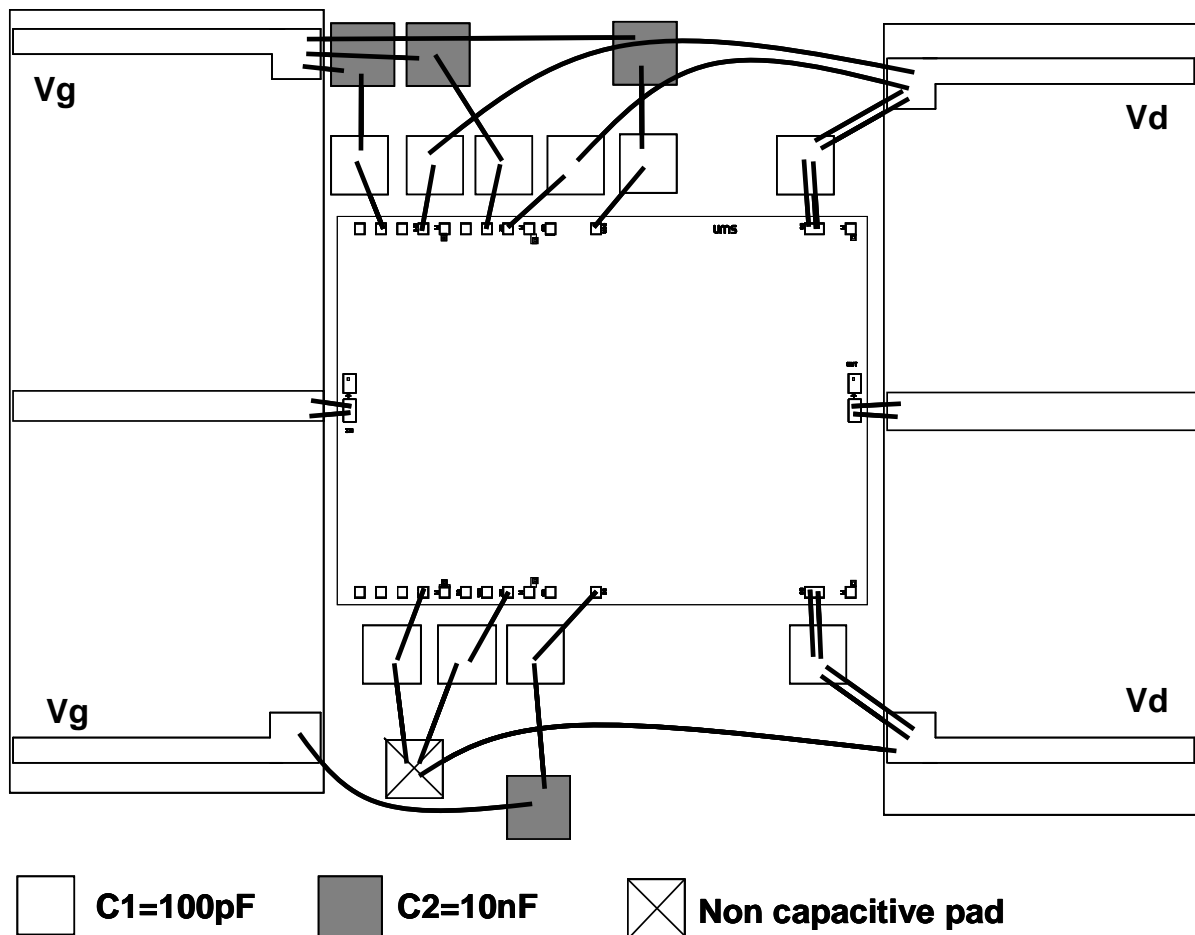
Chip thickness =  $70\mu\text{m} \pm 10\mu\text{m}$   
 RF pads (1, 15) =  $(122 \times 200)\mu\text{m}^2$   
 DC pads (2 to 12, 14, 16, 18 to 28) =  $(100 \times 100)\mu\text{m}^2$   
 DC pads (13, 17) =  $(186 \times 100)\mu\text{m}^2$

Pin number	Pin name	Description
1, 15	IN / OUT	Input / Output RF
3, 8, 12, 18	GiR	Gate supply voltage
4, 6, 10, 14, 16, 20, 24, 26	M	Ground (Not connected)
5, 9, 13, 17, 21, 25	Di	Drain supply voltage
2, 7, 11, 19, 22, 23, 27, 28	Gi / GiR	Not connected

**Bonding recommendations**

Port	Connection	External capacitor
IN	Inductance (L <sub>bonding</sub> ) = 0.35nH 2 gold wires with diameter of 25 μm (600μm max)	
OUT	Inductance (L <sub>bonding</sub> ) = 0.35nH 2 gold wires with diameter of 25 μm (600μm max)	
Vg	Inductance ≤ 1nH	C1 ~ 100pF C2 ~ 10nF
Vd	Inductance ≤ 1nH	C1 ~ 100pF

**Assembly recommendations in test fixture**



**Recommended ESD management**

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

## Ordering Information

Chip form : CHA7215-99F/00

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