

## 6-18GHz High Power Amplifier

### GaAs Monolithic Microwave IC

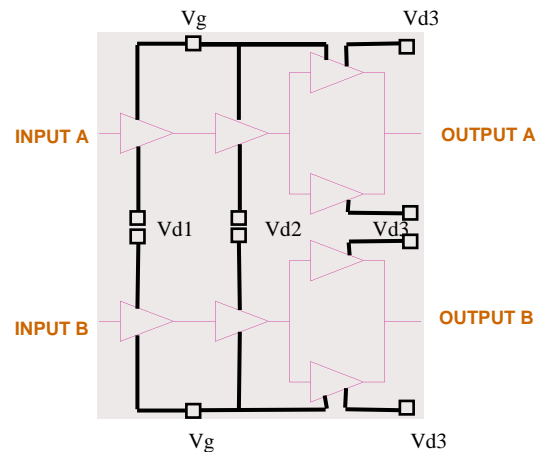
#### Description

The **CHA6517** is a Dual channel monolithic three-stage GaAs high power amplifier designed for wide band applications.

This device is manufactured using a UMS 0.25  $\mu\text{m}$  Power pHEMT process, including, via holes through the substrate and air bridges.

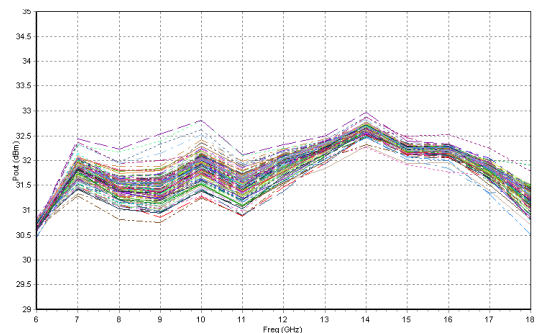
To simplify the assembly process:

- the backside of the chip is both RF and DC grounded
- bond pads and back side are gold plated for compatibility with eutectic die attach method and thermosonic or thermocompression bonding process.



#### Main Features

- 0.25 $\mu\text{m}$  Power pHEMT Technology
- 6 – 18GHz Frequency Range
- 32dBm Output Power per channel
- Compatible for balanced configuration
- 22dB nominal Gain
- Quiescent Bias point : 600mA @ 8V per channel
- Chip size: 4.32 x 3.90 x 0.07mm



*Output Power versus Frequency*

#### Main Characteristics

$T_{\text{amb}}=25^{\circ}\text{C}$  ( $T_{\text{amb}}$  is the back-side of the chip)

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency range	6		18	GHz
Psat	Saturated output power	30	32		dBm
G_lin	Linear gain	19	22		dB

## Electrical Characteristics (one channel)

Tamb=25°C (2), Vd=8V, Id (Quiescent)=0.6A, Pulsed biasing mode

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	6		18	GHz
G_lin	Linear gain (Pin=-5dBm)	19	22		dB
RL_in	Input Return Loss		-14	-8	dB
RL_out	Output Return Loss		-8	-4	dB
Psat	Saturated output power (Pin=11dBm)	30	32		dBm
PAE_sat	Power Added Efficiency in saturation		15		%
Vd	Positive supply voltage		8		V
Id	Power supply quiescent current (1)		0.6		A
Vg	Negative supply voltage		-0.4		V
Top	Operating temperature range (2)	-40		+70	°C

(1) This parameter is fixed by gate voltage Vg

(2) The reference is the back-side of the chip

## Absolute Maximum Ratings (1)

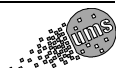
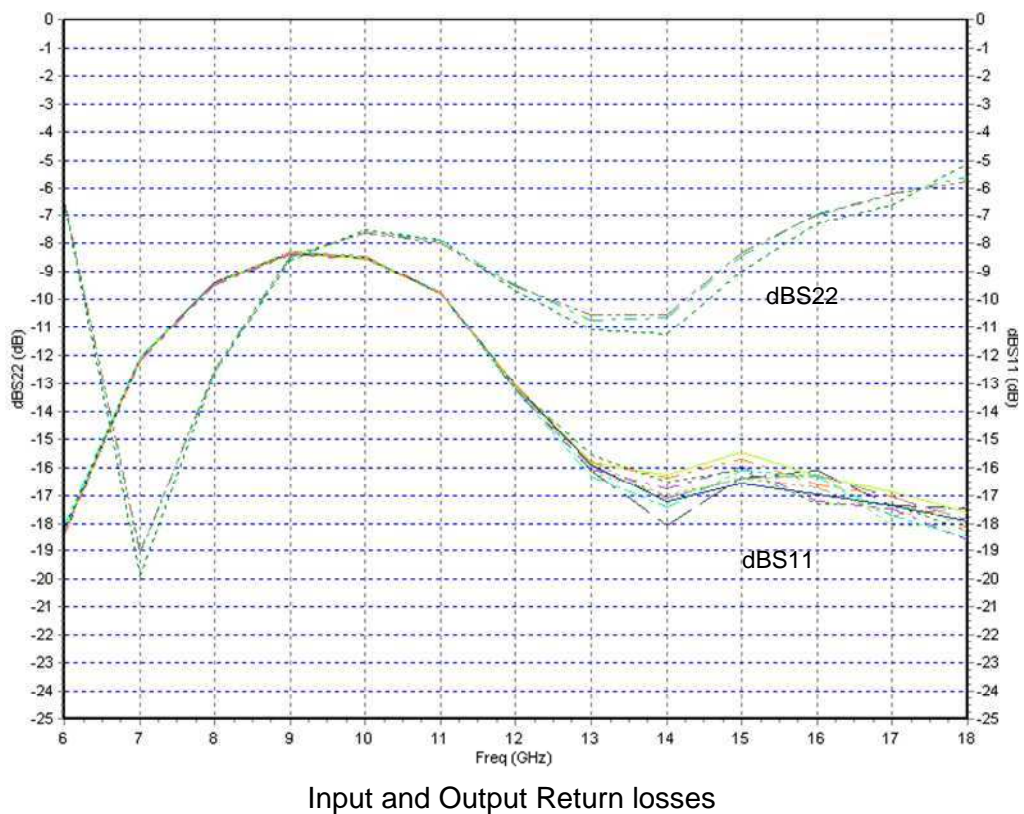
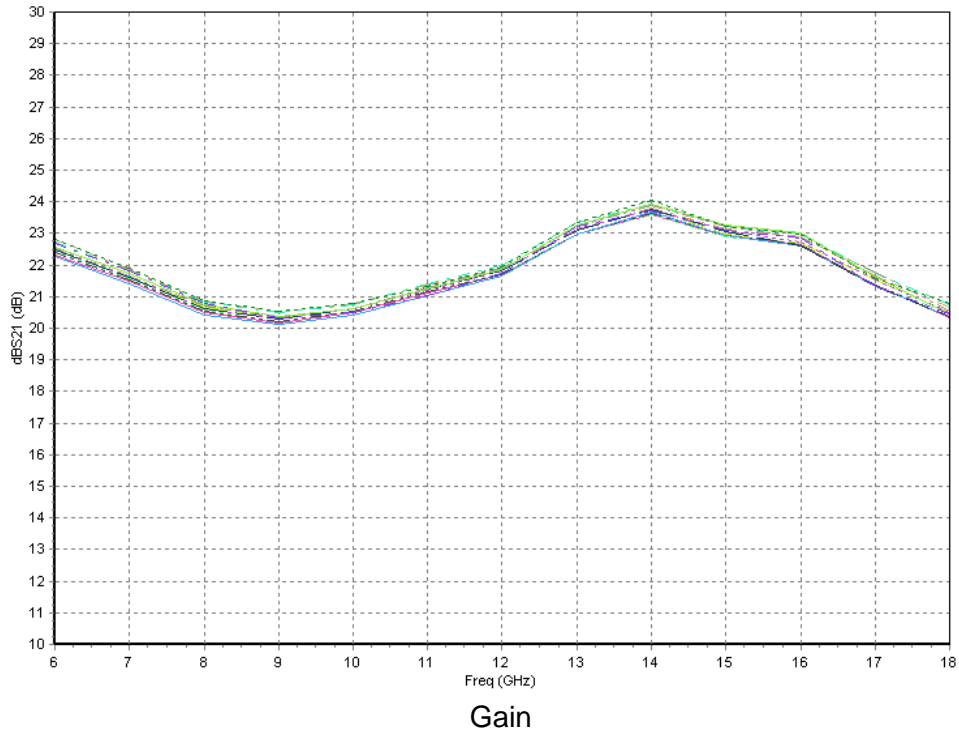
Symbol	Parameter	Values	Unit
Pin (2)	Maximum Input power	19	dBm
Vd (2)	Positive supply voltage without RF power	8.5	V
Id (2)	Positive supply quiescent current	1	A
Pd (2)	Power dissipation	13.5	W
Tj	Junction temperature	175	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) These values are specified for Tamb=25°C

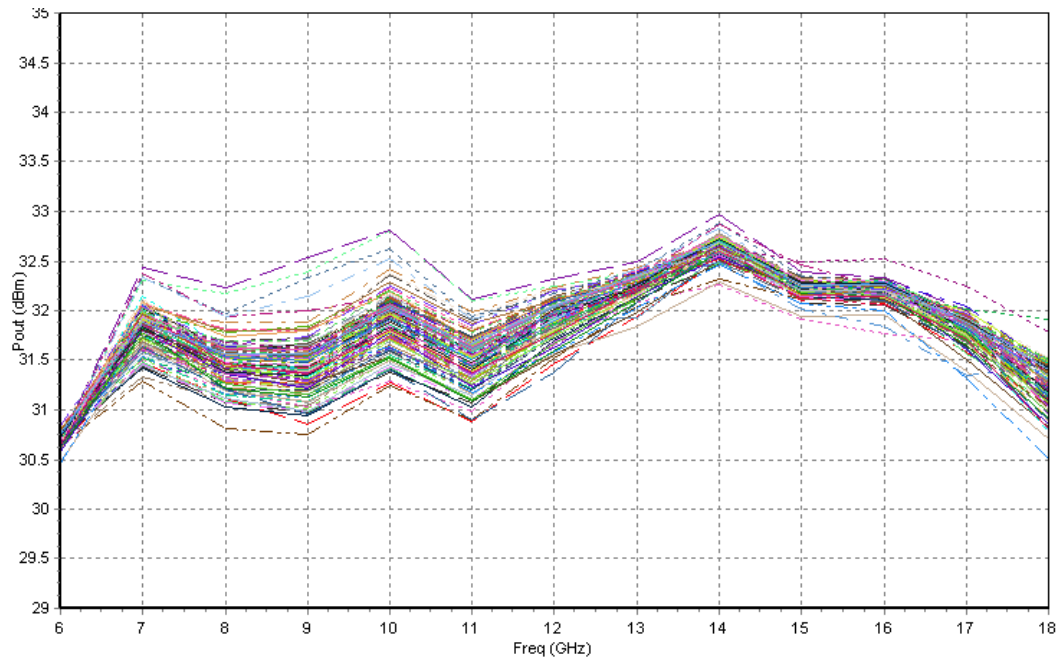
## Typical measured characteristics

On Wafer Measurements, S parameters (one channel):  
Tamb=25°C, Vd=8V, Id (Quiescent)=0.6A, pulsed mode :

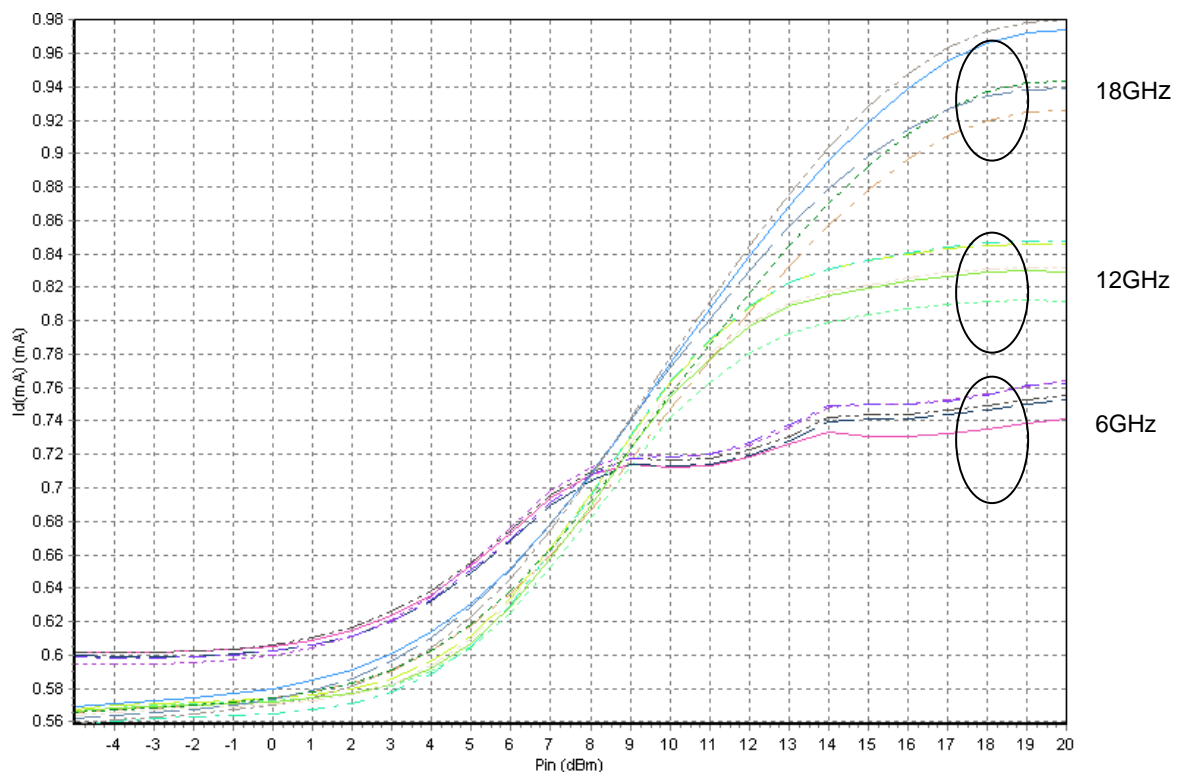


### On Wafer Measurements (one channel):

$T_{amb}=25^{\circ}\text{C}$ ,  $V_d=8\text{V}$ ,  $I_d(\text{Quiescent})=0.6\text{A}$ ,  $P_{in}=11\text{dBm}$ , pulsed mode:



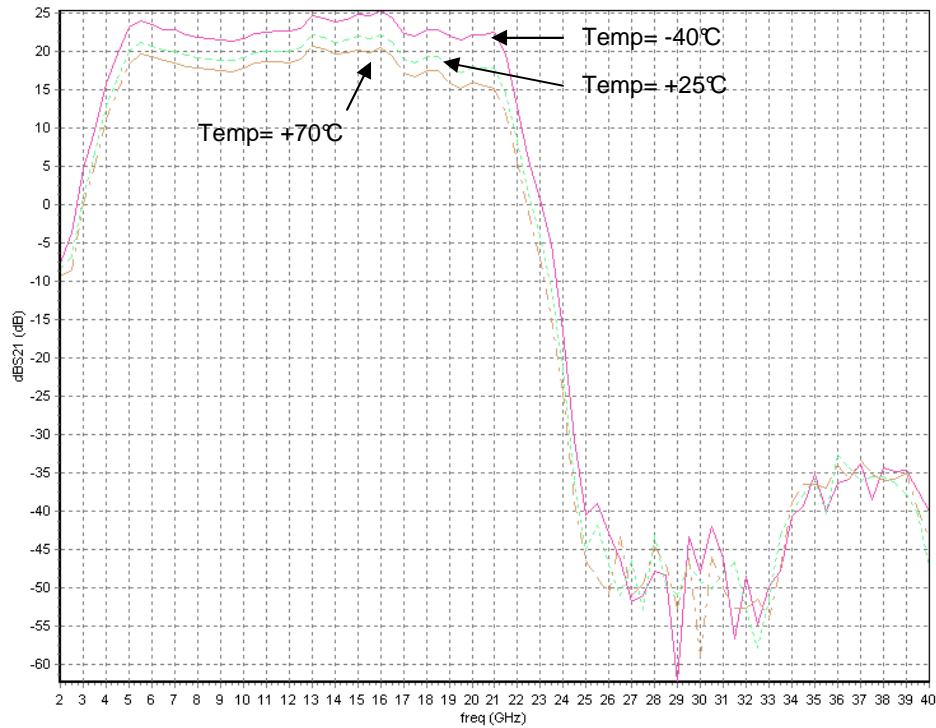
Output Power versus Frequency



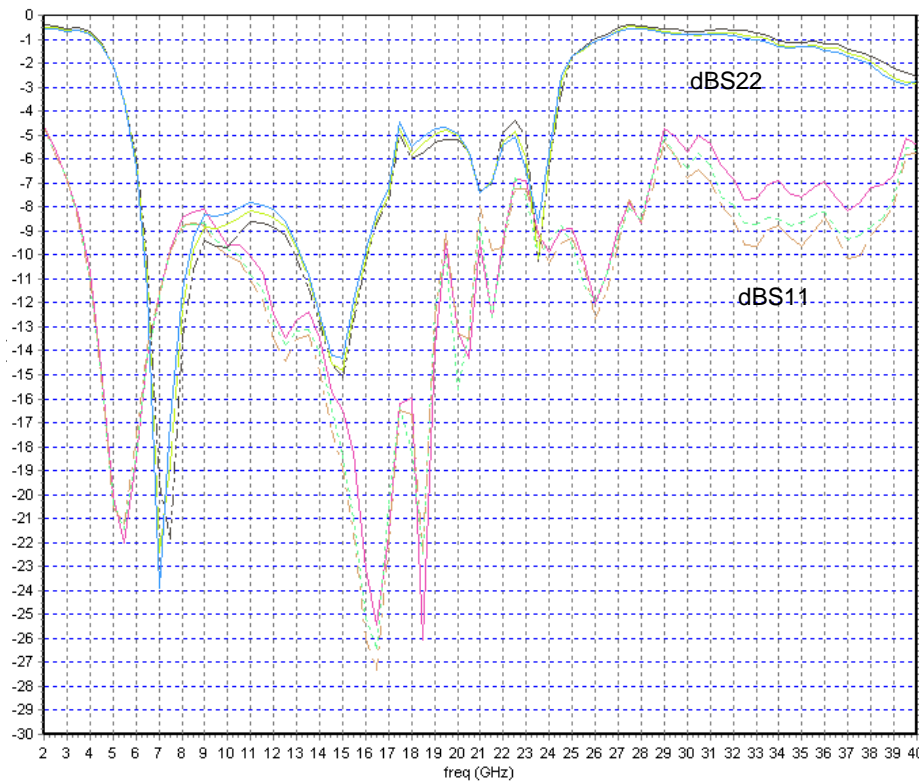
$I_d$  versus  $P_{in}$

## In test jig Measurements (one channel):

Vd=8V, Id (Quiescent)=0.6A, S parameters, CW mode:



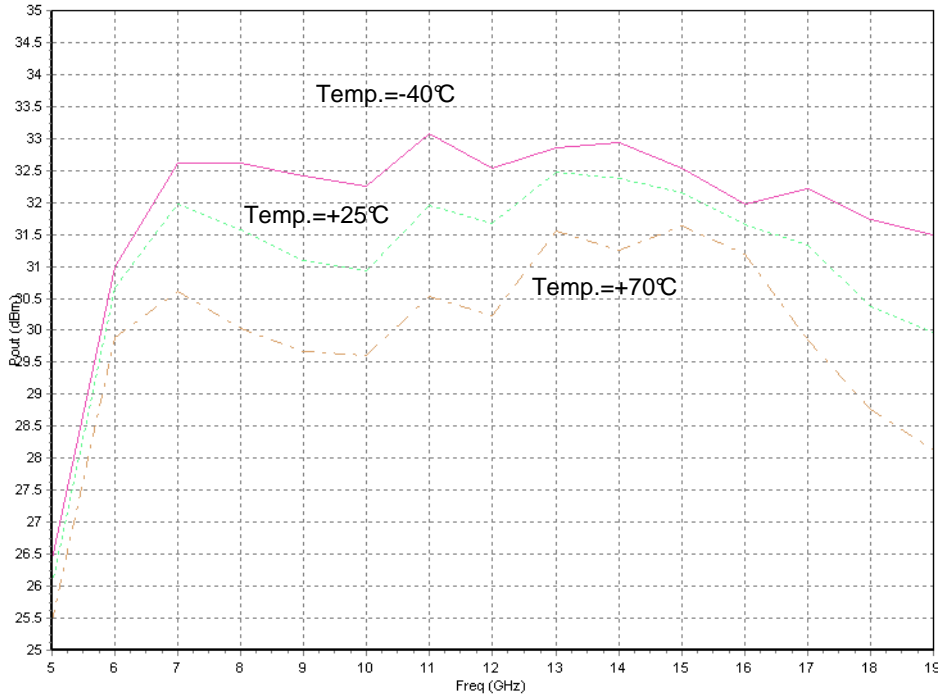
Gain versus Frequency and Temperature (-40°C, +25°C and +70°C)



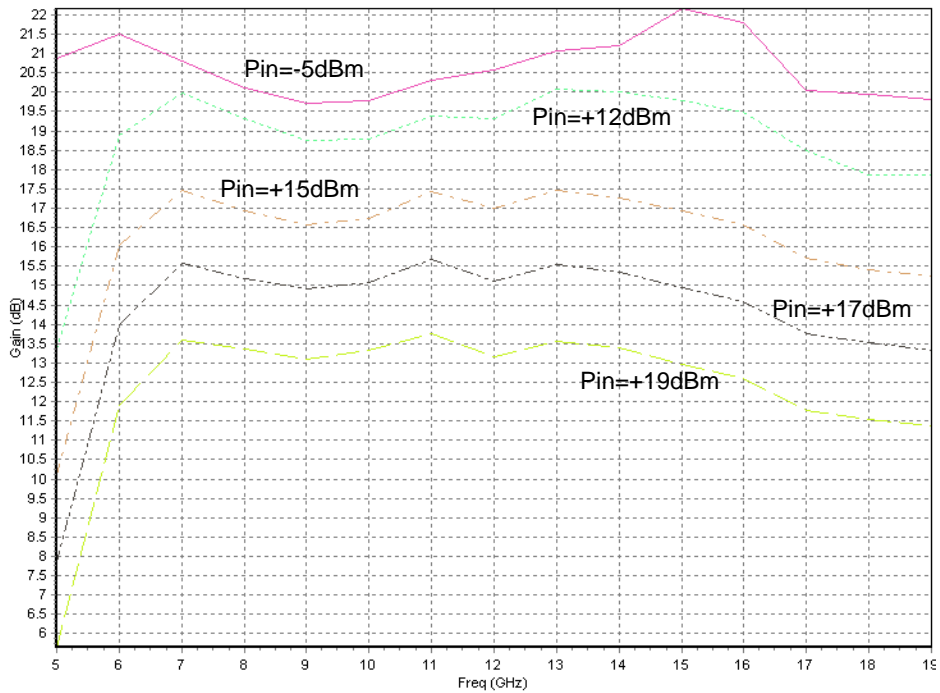
Input and Output Return losses versus Frequency and Temperature

### In test jig Measurements (one channel):

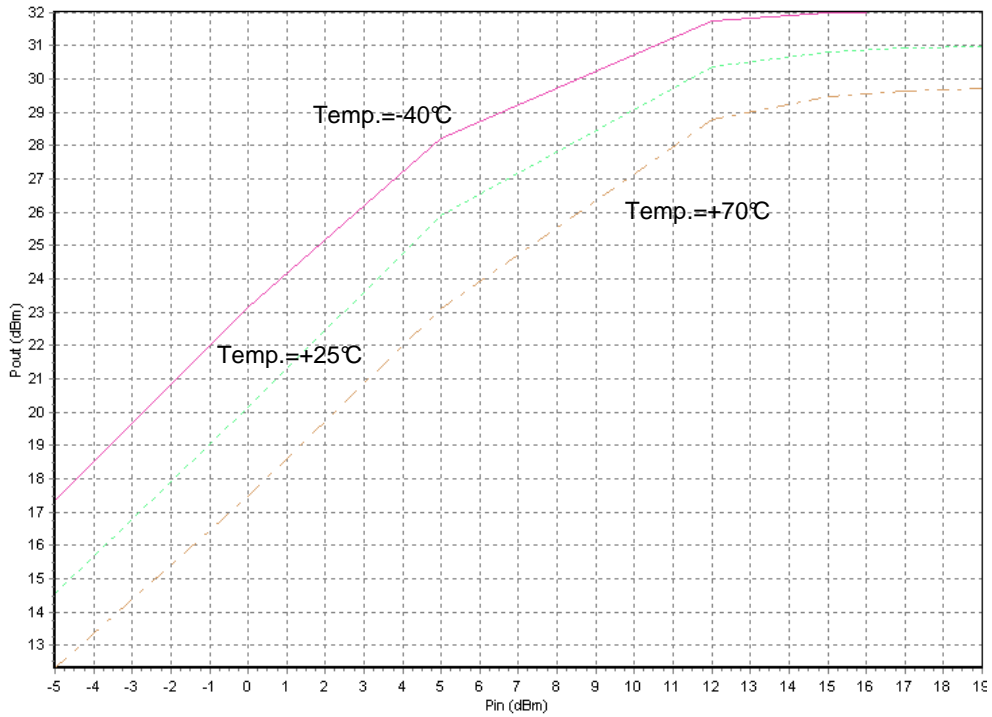
Vd=8V, Id (Quiescent)=0.6A, Power measurements, CW mode



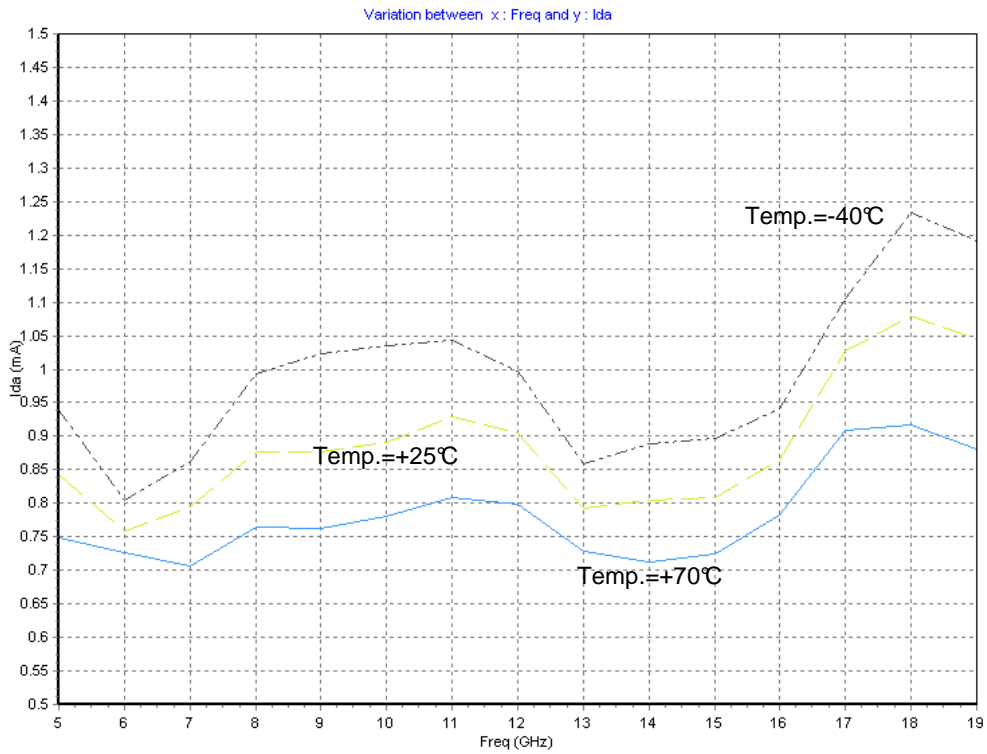
Output power versus Frequency and Temperature (Pin=+12dBm)



Gain versus Frequency and Input power (Temp.=+25°C)

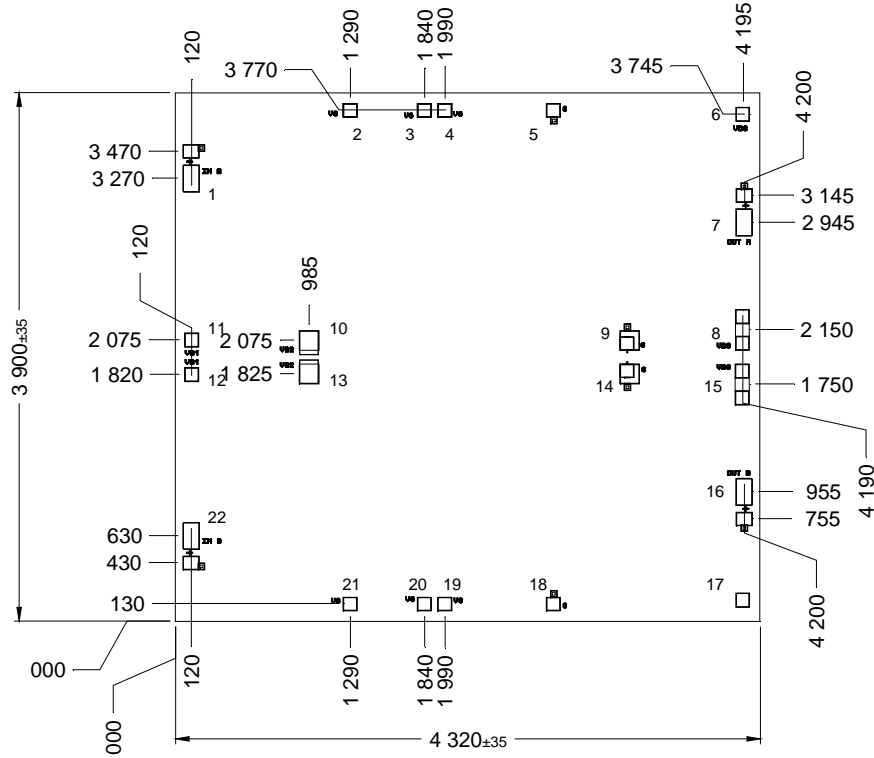


Output power versus Frequency and Temperature (Freq=18GHz)



Id current versus Frequency and Temperature (Pin=+17dBm)

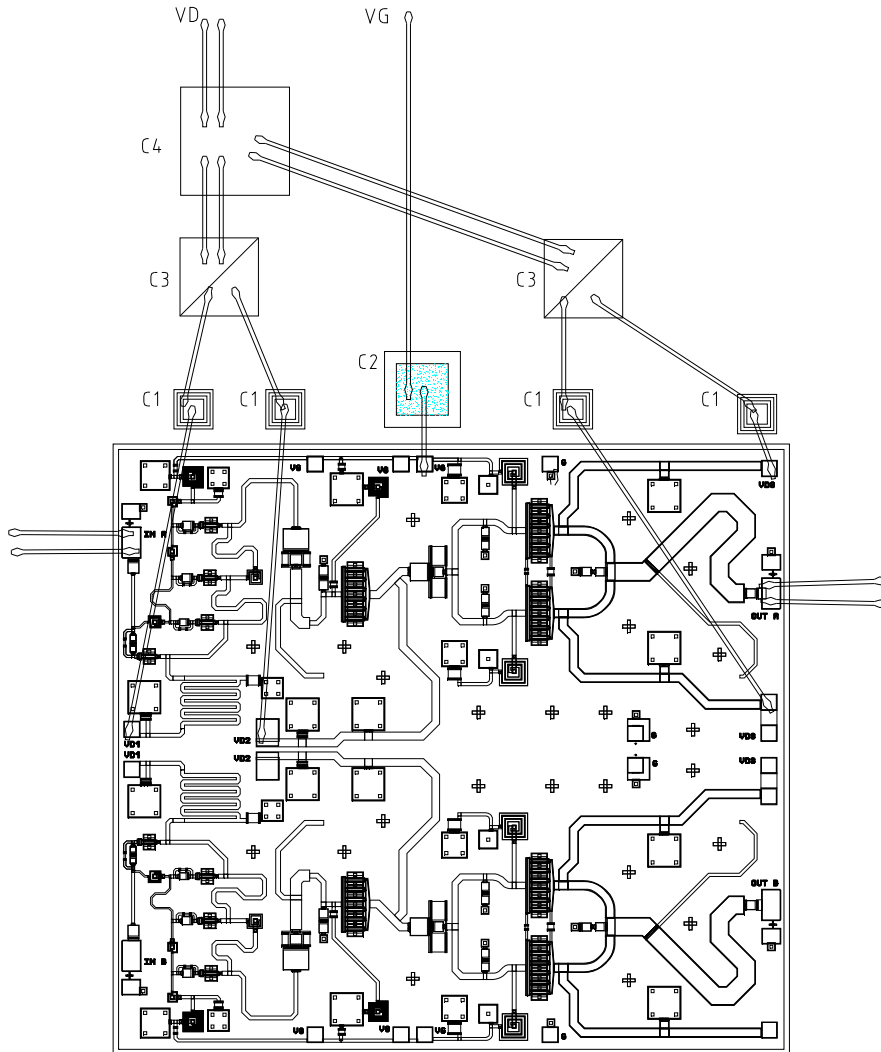
## Chip Mechanical Data and Pin references



UNITS :  $\mu\text{m}$   
 Tol :  $\pm 35\mu\text{m}$

Chip thickness =  $70\mu\text{m} \pm 10\mu\text{m}$   
 HF pads (1, 7, 16, 22) =  $118 \times 196$   
 DC pads =  $96 \times 96$

Pin number	Pin name	Description
1, 22	IN	Input RF port
2, 3, 4, 19, 20, 21	VG	Negative supply voltage
5, 9, 14, 18	GND	Ground (NC)
11, 12	VD1	Positive supply voltage
10, 13	VD2	Positive supply voltage
6, 8, 15, 17	VD3	Positive supply voltage
7, 16	OUT	Output RF port



**Assembly recommendations (one channel)**

For thermal and electrical considerations, the chip should be brazed on a metal base plate. The RF and DC connections should be done according to the following table:

Port	Connection	External capacitor
IN (1, 22) OUT (7, 16)	Inductance (L <sub>bonding</sub> )=0.3nH	
VD (6, 8, 10, 11, 12, 13, 15, 17)	Inductance ≤1nH	C1 ~ 22pF C3~ 1nF C4~100nF
VG (2, 3, 4, 19, 20, 21)	Inductance ≤1nH	C2~ 120pF

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

## Ordering Information

Chip form : CHA6517-99F/00

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