

Multifunction K-band VCO and Q-band Multiplier

GaAs Monolithic Microwave IC

Description

The CHV2240 is a monolithic multifunction proposed for frequency generation at 38GHz. It integrates a K-band Voltage Controlled Oscillator, a Q-band frequency multiplier and buffer amplifiers. For performance optimisation, an external port (ERC) allows a passive resonator coupling to the oscillator (at half output frequency). This chip has been especially designed to be coupled to a high Q dielectric resonator. All the active devices are internally self biased.

The circuit is manufactured with the pHEMT process 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.

Main Features

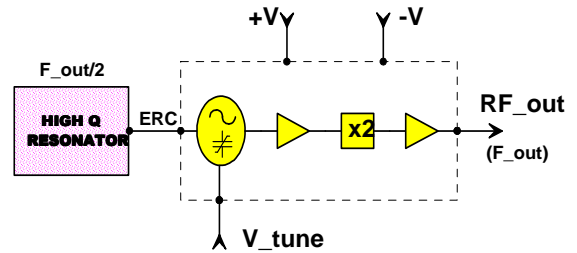
- K-band VCO + Q-band frequency multiplier
- External resonator for centre frequency control and phase noise optimisation
- High quality oscillator when coupled to a dielectric resonator
- On-chip varactor for electronic control
- Chip size 2.68 x 1.4 x 0.1 mm

Main Characteristics

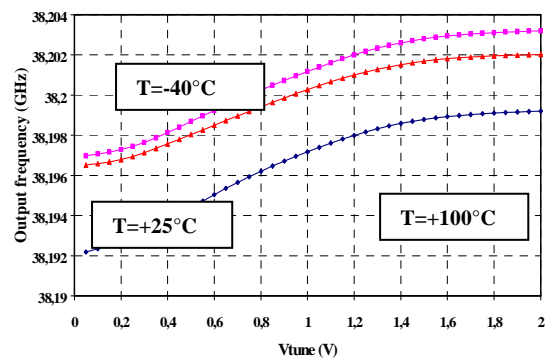
Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency	37.5	38.25	39	GHz
F_t	Frequency tuning range (high Q resonator)		5		MHz
Pn	Oscillator phase noise @ 100kHz (38GHz)		-100		dBc/Hz
Pout	Output power		9		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !



Multifunction block diagram



Typical tuning characteristic

Electrical Characteristics

Full temperature range, used according to section "Typical assembly and bias configuration"

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency	37.5	38.25	39	GHz
F_osc	Oscillator frequency (1)	F_out/2			
F_stab	Frequency stability (1) , (2)		4		ppm/°C
Pn	Phase noise @ 100kHz @ 38GHz (2)		-100		dBc/Hz
P_out	Output power	6	9		dBm
F_t	Frequency tuning range (2)		5		MHz
Vt	Voltage tuning range			0-2	V
I_vt	Tuning current			0.5	mA
VSWR_out	VSWR at output port		2:1		
+V	Positive supply voltage	4.4	4.5	4.6	V
+I	Positive supply current		120	180	mA
-V	Negative supply voltage	-4.6	-4.5	-4.4	V
-I	Negative supply current		3	10	mA
Top	Operating temperature range	-40		+100	°C

(1) The centre frequency is given by the external passive resonator

(2) This characteristic is obtained by using an external dielectric resonator (see section "Proposed External High Q resonator")

Absolute Maximum Ratings (1)

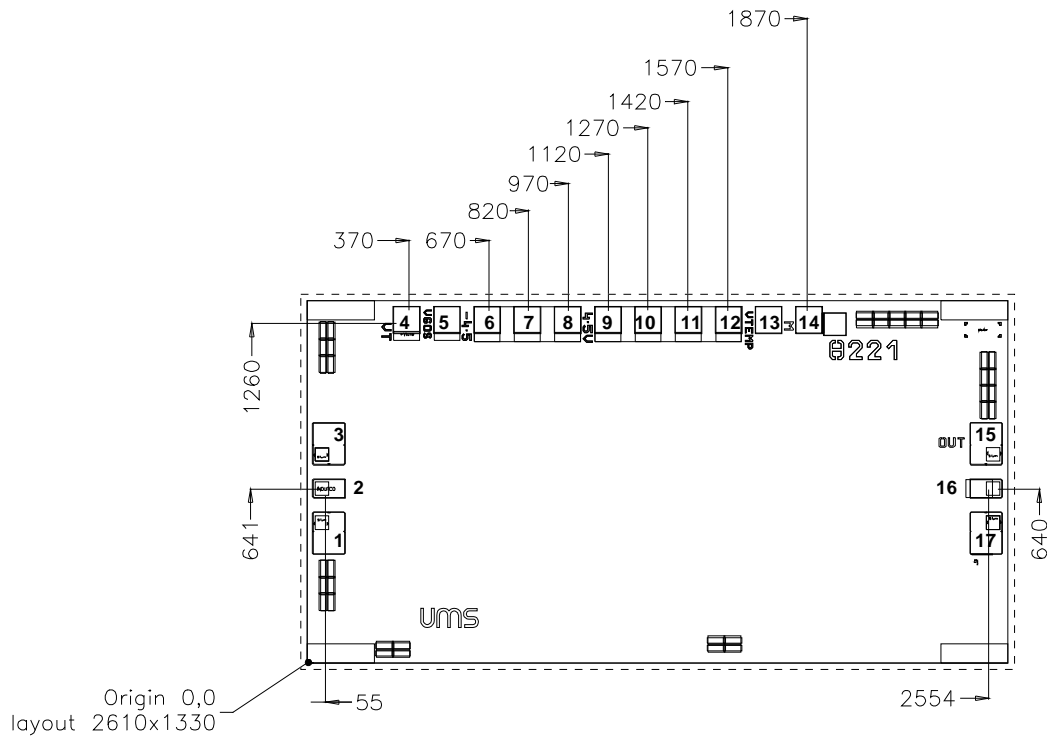
Tamb = +25°C

Symbol	Parameter	Values	Unit
P_erc	RF input power on ERC port (2)	13	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	200	mA
-I	Negative supply current	10	mA
Top	Operating temperature range	-40 to +100	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s

Chip Mechanical Data and Pin References



Unit = μm

External chip size (layout size + dicing streets) = 2680 x 1400

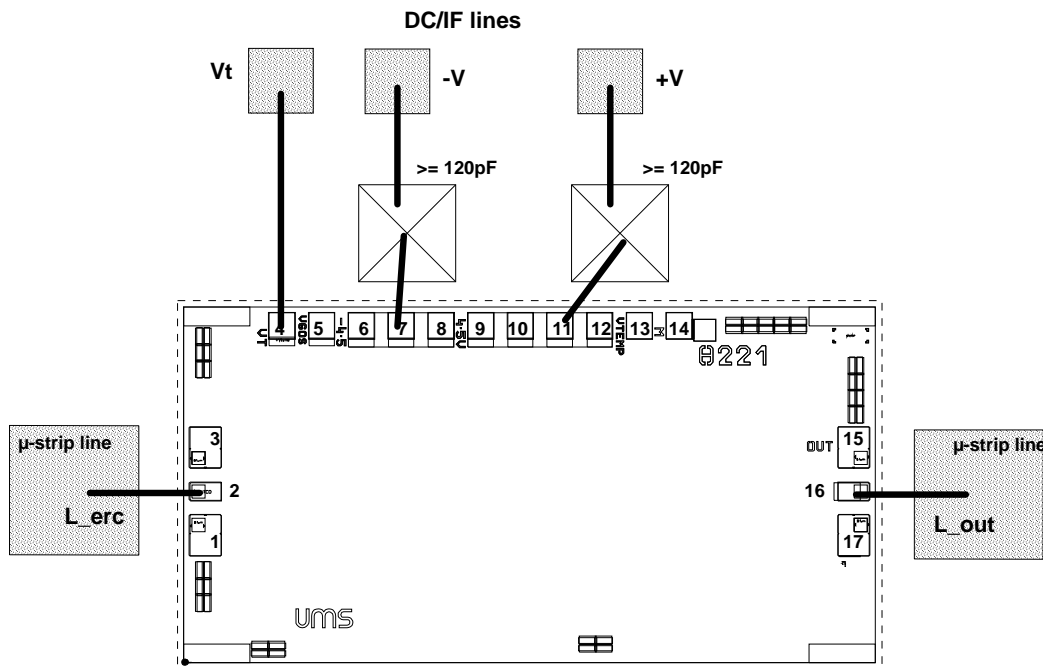
Chip thickness = 100 +/- 10

HF Pads (2, 16) = 68 x 118

DC/IF Pads = 100 x 100

◆ Pin number	Pin name	Description
1,3,15,17		Ground : should not be bonded. If required, please ask for more information.
2	ERC	External Resonator Coupling Port
4	Vt	Tuning voltage
5,13		NC
6,7,8	-V	Negative supply voltage (connected together)
9,10,11,12	+V	Positive supply voltage (connected together)
14	GND	Ground (optional)
16	RF_out	RF output

Typical Assembly and Bias Configuration



This drawing shows an example of assembly and bias configuration. All the transistors are internally self biased.

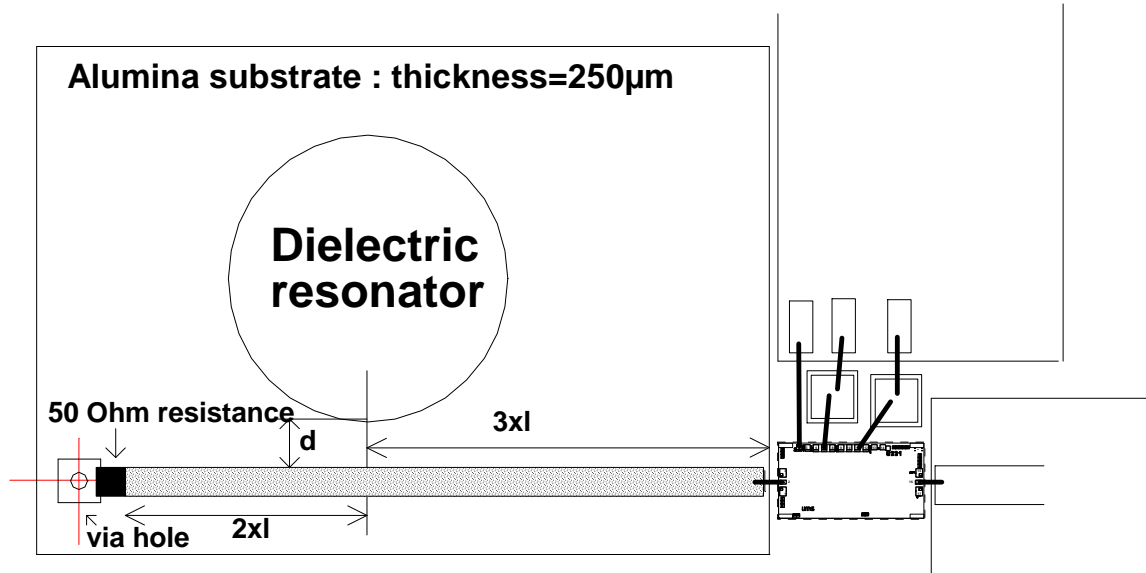
For the RF pads the equivalent wire bonding inductance (diameter=25 μ m) have to be according to the following recommendation.

Port	Equivalent inductance (nH)	Approximated wire length (mm)
ERC (2)	$L_{erc} = 0.4$	0.5
RF_out (16)	$L_{out} = 0.4$	0.5

For a micro-strip configuration a hole in the substrate is recommended for chip assembly.

Proposed external high Q resonator

This chip has been especially designed to be coupled to a high Q dielectric resonator. The resonance is given by a dielectric cylinder coupled to a 50Ω line. The size of the resonator gives the centre frequency and the space between the resonator and the line gives the loaded quality factor. The following drawing shows an example of external configuration.



Additional information

- **Resonator reference** example = MURATA /DRD036EC016. As the exact frequency is given by the resonator size but also by the environment (cavity size, substrate characteristics, parasitic couplings ...), the final dimensions of the resonator have to be defined according to the definitive module design. Other kind of resonators can be used (from TEKELEC or TRANS-TECH). The temperature coefficient has to be chosen according to the environment.
- **Resonator coupling:** $d=0.2$ to 0.3mm , $l=1.5\text{mm}$ (quarter wave). These values have been used in the test fixture, of course they can be modified if the environment is different. The distance between the resonator and the edge of the substrate (close to MMIC) is proposed to be $3xl=4.5\text{mm}$ (3 quarter waves), theoretically only one is necessary but in this case the distance between resonator and MMIC is too low for automatic assembly.
- **50Ω line width** on alumina (height= 0.25mm) = 0.238mm
- **50Ω load** on alumina: this load has to be as good as possible (low parasitic inductance).
- **Cavity size** (mm) : $18 \times 17 \times 7$
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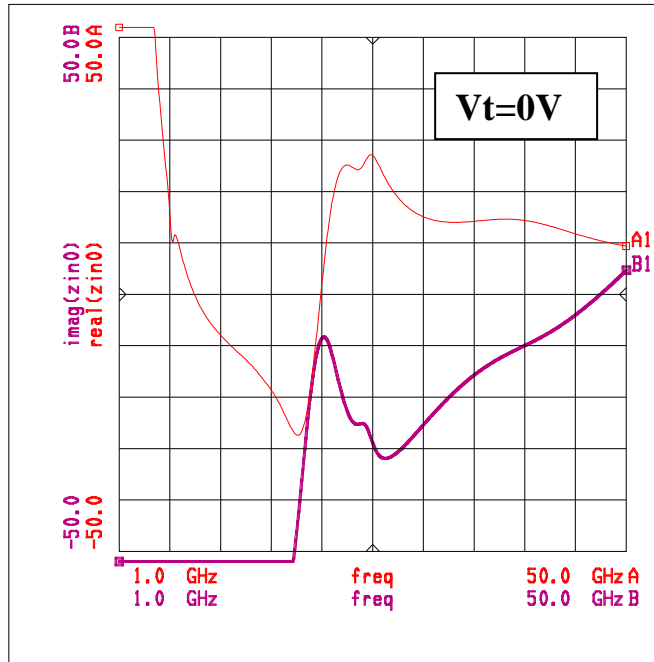
Recommendation for Frequency stability

In order to ensure a good frequency stability (versus temperature, external resonator aging,...), it is recommended to use an external frequency locked loop with a low frequency loop filter (below modulation frequency), or a PLL for both frequency modulation and stability.

External Resonator Coupling Port Information

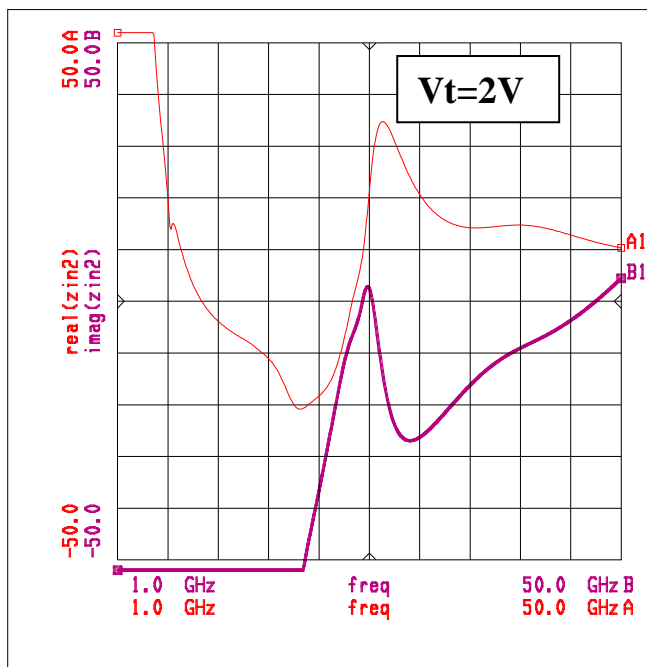
The external resonator has to be an equivalent series resonance. However, this impedance must also be compatible to the negative impedance of the oscillator ERC port in order to obtain the oscillation conditions and to avoid parasitic oscillations. Typical impedance of ERC port (Z_{erc}) is given in the following tables. The diagrams show this impedance in a wider band. These values don't include the wire bonding (self L_{erc} given in the section "Typical Assembly and Bias Configuration").

freq	real(zin0)	imag(zin0)
17.00E+09	-23.414	-63.610
17.42E+09	-25.203	-58.098
17.84E+09	-26.725	-51.603
18.26E+09	-27.432	-43.934
18.68E+09	-26.461	-35.282
19.10E+09	-23.188	-26.530
19.52E+09	-17.590	-18.853
19.94E+09	-10.427	-13.027
20.36E+09	-2.368	-9.437
20.78E+09	5.754	-8.297
21.21E+09	13.008	-9.432
21.63E+09	18.621	-12.212
22.05E+09	22.279	-15.663
22.47E+09	24.348	-18.997
22.89E+09	25.148	-21.911
23.31E+09	25.017	-24.027
23.73E+09	24.497	-25.129
24.15E+09	24.283	-25.275
24.57E+09	25.095	-25.153
25.00E+09	26.625	-26.170



Vt=0V

freq	real(zin2)	imag(zin2)
17.00E+09	-15.142	-74.139
17.42E+09	-17.030	-70.563
17.84E+09	-18.863	-66.355
18.26E+09	-20.255	-61.523
18.68E+09	-20.842	-56.382
19.10E+09	-20.675	-51.447
19.52E+09	-20.053	-46.950
19.94E+09	-19.374	-42.816
20.36E+09	-18.704	-38.785
20.78E+09	-17.968	-34.696
21.21E+09	-17.030	-30.468
21.63E+09	-15.724	-26.112
22.05E+09	-13.937	-21.747
22.47E+09	-11.627	-17.424
22.89E+09	-8.593	-13.313
23.31E+09	-4.905	-9.826
23.73E+09	-1.009	-7.189
24.15E+09	2.510	-5.036
24.57E+09	5.881	-2.230
25.00E+09	11.191	1.416



Vt=2V

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Ordering Information

Chip form : CHV2240-99F/00

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