

25-45 GHz Attenuator

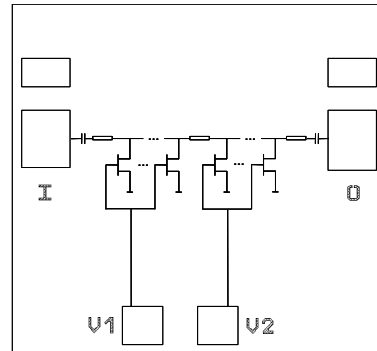
GaAs Monolithic Microwave IC

Description

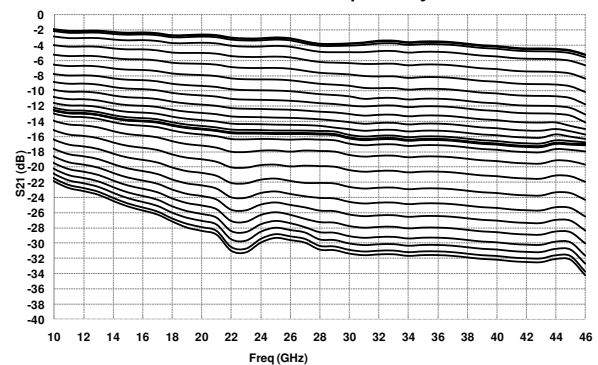
The CHT4694 is a variable 25-45GHz attenuator designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a MESFET process, 0.7 μ m gate length, via holes through the substrate and air bridges.

It is supplied in chip form.



Attenuation versus Frequency & V1, V2



Main Features

- Broadband performance: 25-45GHz
- 22dBm typical input 1dB compression point (any attenuation)
- 25dB dynamic range
- DC bias: $-5V < V1 < 0V$; $-5V < V2 < 0V$
- Chip size: 1.5x1.39x0.1mm

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	25		45	GHz
Min Att.	S21 (V1=-5V;V2=-5V) (25 to 30GHz)		3	4	dB
	S21 (V1=-5V;V2=-5V) (30 to 40GHz)		4	5.5	dB
	S21 (V1=-5V;V2=-5V) (40 to 45GHz)		4	7	dB
Max Att.	S21 (V1=0V;V2=0V) (25 to 30GHz)	20	23		dB
	S21 (V1=0V;V2=0V) (30 to 45GHz)	25	28		dB
Pin1dB	Input 1dB compression point (any attenuation) (25-40 GHz)	20	22		dBm
	Input 1dB compression point (any attenuation) (40-45 GHz)	18	20		dBm

ESC Protections: Electrostatic discharge sensitive device observe handling precautions!

Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	25		45	GHz
Min Att.	S21 (V1=-5V;V2=-5V) (25 to 30GHz)		3	4	dB
	S21 (V1=-5V;V2=-5V) (30 to 40GHz)		4	5.5	dB
	S21 (V1=-5V;V2=-5V) (40 to 45GHz)		4	7	dB
Max Att.	S21 (V1=0V;V2=0V) (25 to 30GHz)	20	23		dB
	S21 (V1=0V;V2=0V) (30 to 45GHz)	25	28		dB
RLin	Input Return loss (any attenuation) (25 to 30GHz)			-10	dB
	Input Return loss (any attenuation) (30 to 45GHz)			-6	dB
RLout	Ouput Return loss (any attenuation) (25 to 30GHz)			-5	dB
	Ouput Return loss (any attenuation) (30 to 45GHz)			-3	dB
Pin1dB	Input 1dB compression point (any attenuation) (25 to 40 GHz)	20	22		dBm
	Input 1dB compression point (any attenuation) (40 to 45 GHz)	18	20		dBm
IIP3	Input 3 rd order Intercept Point (any attenuation)(25 to 40 GHz, Pin DCL > -4dBm)	25	30		dBm
	Input 3 rd order Intercept Point (any attenuation)(25 to 40 GHz, Pin DCL > -4dBm)	23	26		dBm

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V1	V1 control voltage	-6V to +0.6V	V
V2	V2 control voltage	-6V to +0.6V	V
Pin	RF input power	30	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V1	V1 control voltage	-5 to 0	V
V2	V2 control voltage	-5 to 0	V

Typical on-wafer Sij parameters

Tamb = +25°C - V1 = -5V & V2= -5V – Minimum attenuation

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
25.0	-17.8	-45.3	-2.4	67.5	-2.3	69	-18.8	-15.8
26.0	-17.0	-45.6	-2.7	55.6	-2.5	55.5	-17.0	-29.5
27.0	-16.2	-47.6	-2.6	43.3	-2.7	41.6	-15.5	-40.1
28.0	-16.0	-57.3	-2.6	28.2	-2.8	28.6	-15.1	-50.7
29.0	-16.4	-61.1	-2.8	15.2	-2.9	15.2	-14.5	-61.3
30.0	-16.9	-69.0	-2.9	1.1	-3.0	1.8	-14.6	-68.0
31.0	-18.8	-81.3	-3.4	-12.0	-3.3	-11.9	-14.1	-73.2
32.0	-23.2	-88.2	-3.6	-24.1	-3.6	-25.5	-14.8	-81.6
33.0	-33.0	-68.8	-3.6	-36.8	-3.7	-37.8	-16.3	-88.2
34.0	-23.5	46.0	-3.7	-51.2	-3.8	-51.3	-17.8	-83.1
35.0	-16.9	30.8	-4.1	-64.7	-4.3	-67.0	-19.3	-66.4
36.0	-13.2	23.6	-3.9	-78.0	-4.8	-78.1	-19.8	-55.3
37.0	-10.6	6.1	-4.1	-94.8	-4.3	-92.3	-16.5	-40.0
38.0	-9.2	-6.2	-4.8	-109.5	-4.8	-108.0	-15.3	-38.1
39.0	-8.0	-19.3	-4.6	-121.1	-5.0	-116.4	-12.9	-53.0
40.0	-8.2	-31.8	-5.1	-137.5	-5.3	-135.8	-12.8	-58.6
41.0	-8.2	-44.3	-4.8	-149.6	-5.5	-146.6	-11.2	-64.6
42.0	-9.9	-46.2	-5.3	-170.7	-5.7	-167.3	-12.3	-70.1
43.0	-10.3	-48.9	-5.9	177.1	-5.9	178.5	-12.9	-69.6
44.0	-11.1	-50.0	-6.0	162.5	-6.4	163.8	-13.6	-70.6
45.0	-11.4	-44.1	-6.6	145.4	-6.9	150.5	-14.6	-60.8

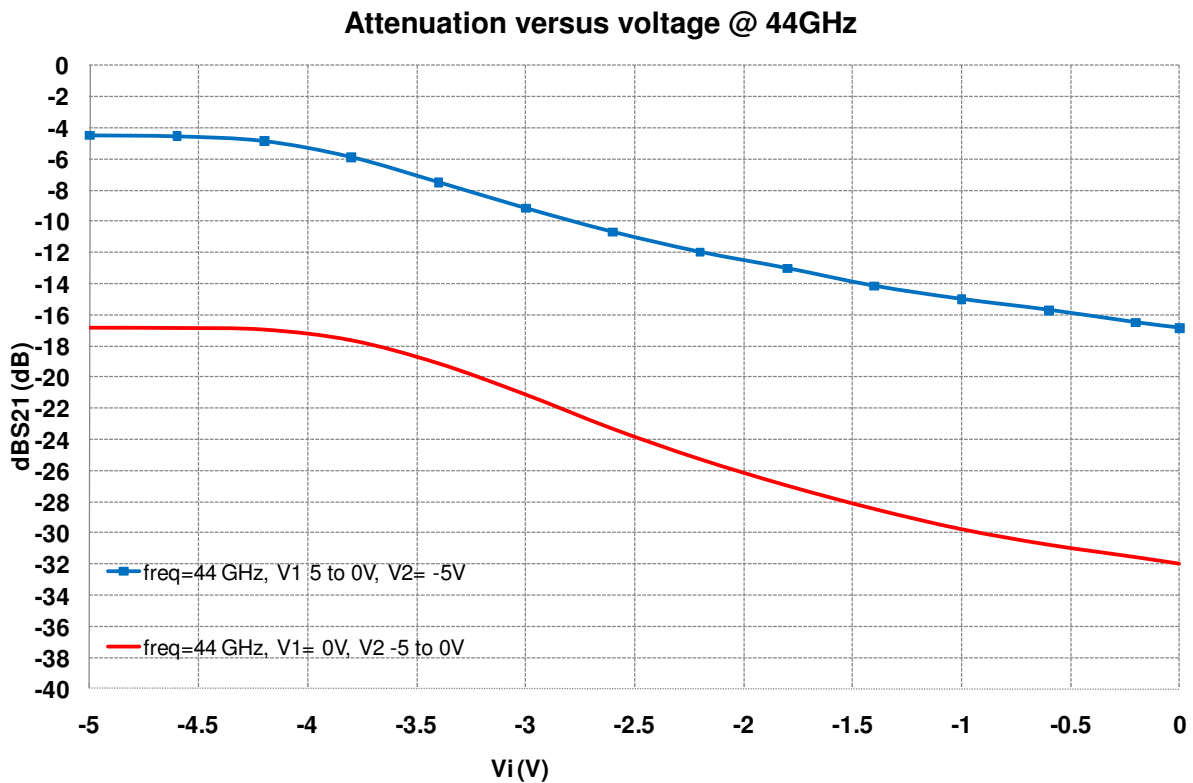
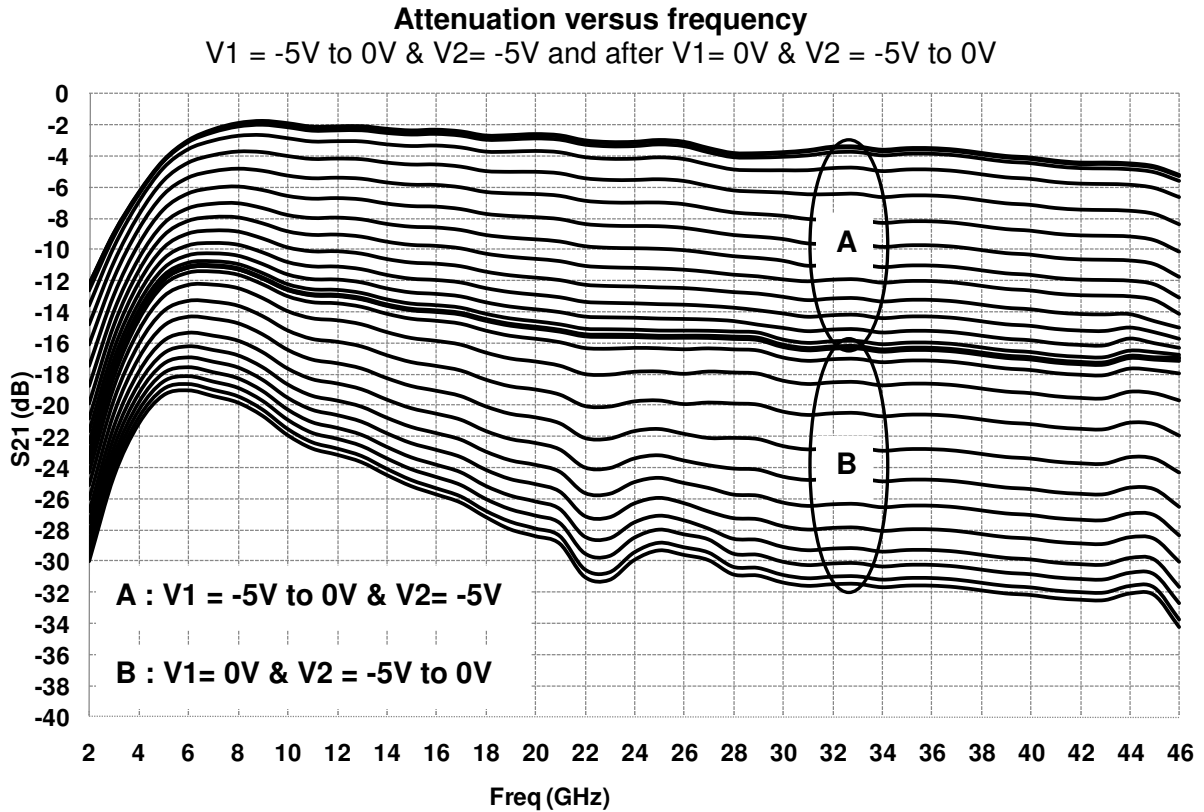
Typical on-wafer Sij parameters

Tamb = +25°C - V1 = 0V & V2= 0V – Maximum attenuation

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
25.0	-12.9	10.5	-26.0	76.7	-25.5	78.9	-5.6	45.8
26.0	-12.5	7.3	-26.5	67.6	-26.0	67.8	-5.7	36.8
27.0	-12.1	5.3	-26.9	57.3	-26.3	54.2	-5.5	29.0
28.0	-11.8	1.8	-27.5	45.0	-27.3	42.6	-5.5	21.2
29.0	-11.5	0.7	-27.9	35.9	-27.7	-33.9	-5.4	13.7
30.0	-10.8	-2.1	-28.5	21.6	-28.5	19.8	-5.3	6.6
31.0	-10.5	-5.0	-30.2	8.6	-29.9	10.9	-5.1	-0.5
32.0	-10.2	-6.7	-30.8	0.9	-30.5	-2.8	-5.0	-7.7
33.0	-9.5	-9.8	-31.9	-9.3	-31.6	-14.1	-4.9	-13.8
34.0	-9.0	-12.0	-33.0	-23.7	-32.5	-26.4	-4.8	-21.0
35.0	-8.3	-15.4	-34.5	-31.0	-34.0	-40.9	-4.7	-25.7
36.0	-7.8	-20.1	-33.8	-44.4	-34.8	-50.3	-4.9	-38.5
37.0	-7.5	-25.3	-34.5	-71.3	-34.5	-75.6	-4.9	-35.0
38.0	-7.2	-28.5	-36.9	-96.1	-36.8	-97.7	-4.9	-38.5
39.0	-6.8	-34.2	-34.7	-109.6	-35.1	-110.2	-4.7	-46.4
40.0	-6.7	-38.0	-36.0	-134.7	-36.5	-137.6	-4.9	-57.3
41.0	-6.6	-44.1	-33.6	-152.7	-35.5	-154.5	-4.9	-54.3
42.0	-6.9	-44.6	-34.4	176.6	-35.3	176.5	-4.7	-57.3
43.0	-6.5	-48.5	-34.3	174.4	-34.3	170.7	-4.8	-59.6
44.0	-6.5	-54.8	-32.7	151.7	-33.8	151.2	-4.3	-64.3
45.0	-6.7	-57.8	-33.7	129.3	-33.6	134.7	-4.9	-69.7

Typical on test fixture measurements

Tamb.= +25°C

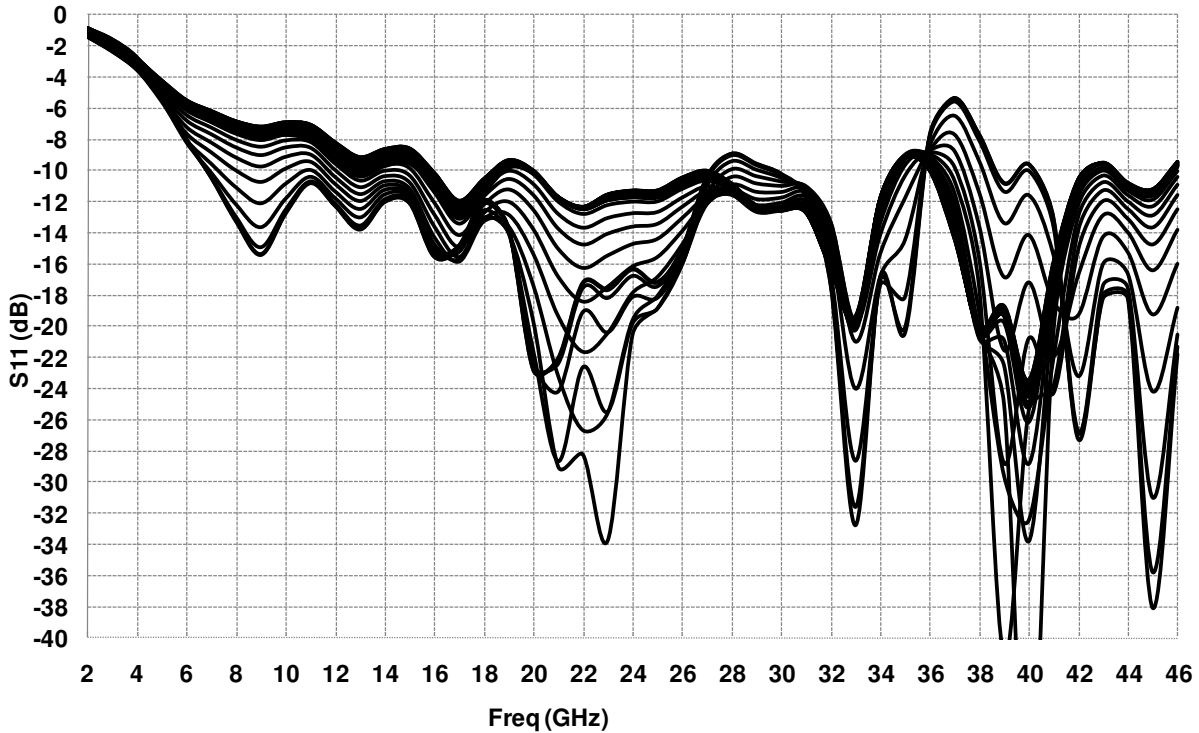


Typical on test fixture measurements

Tamb.= +25°C

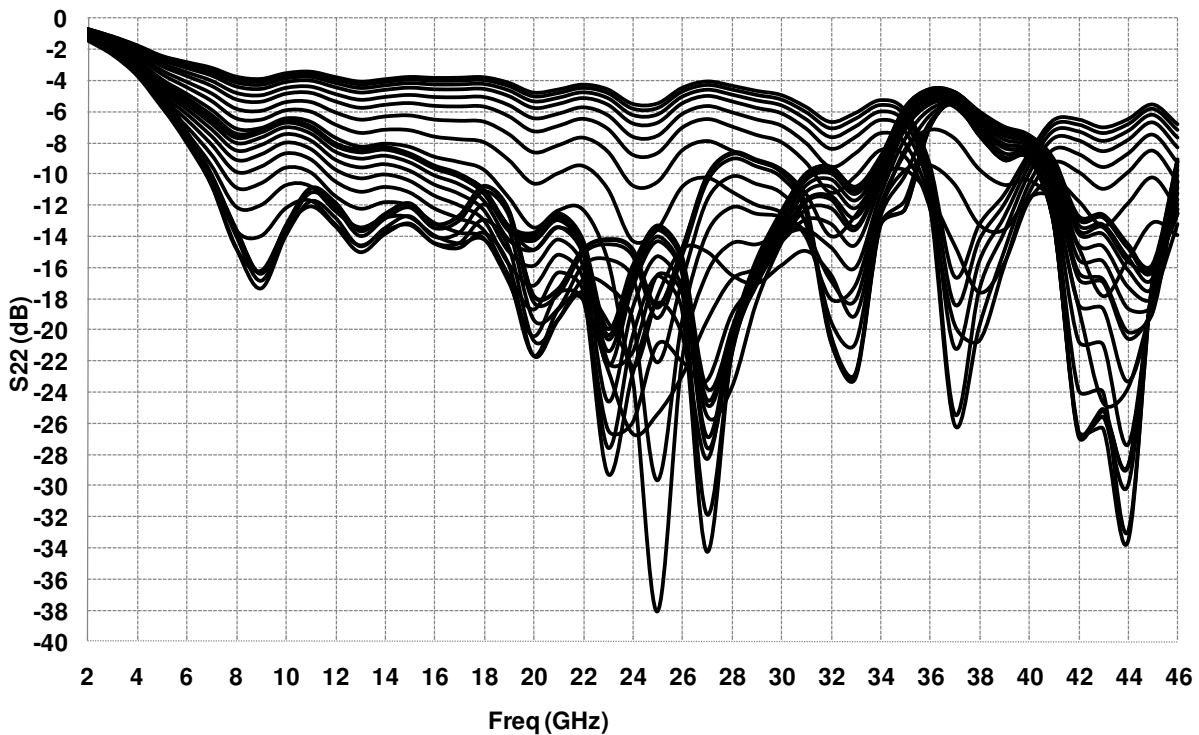
Input return loss versus frequency

V1 = -5V to 0V & V2= -5V and after V1= 0V & V2 = -5V to 0V



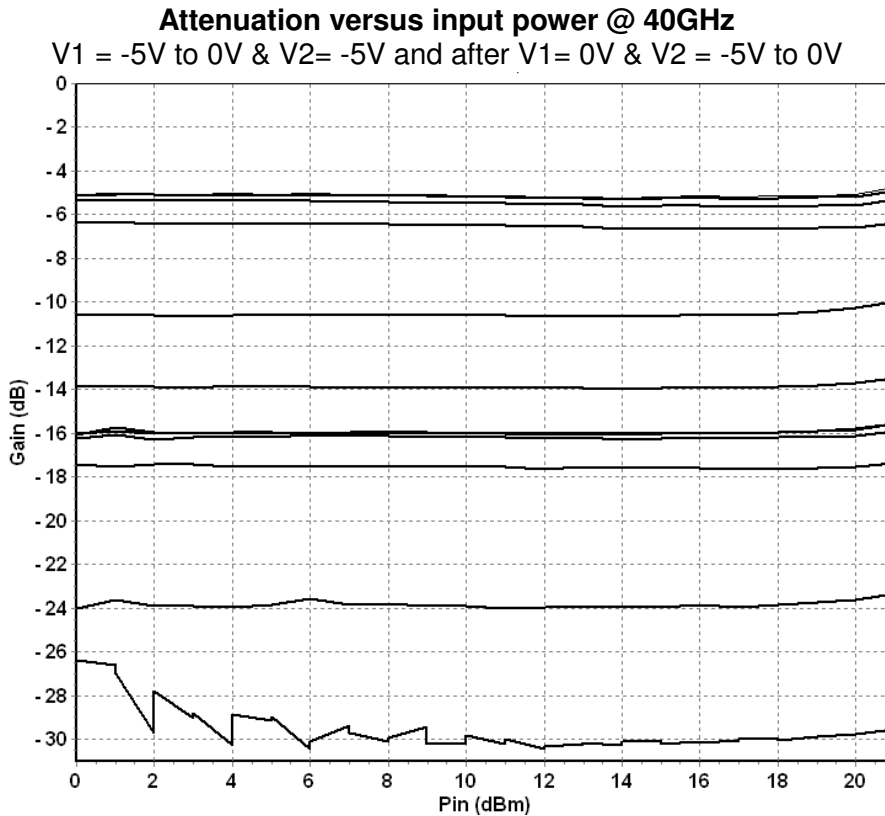
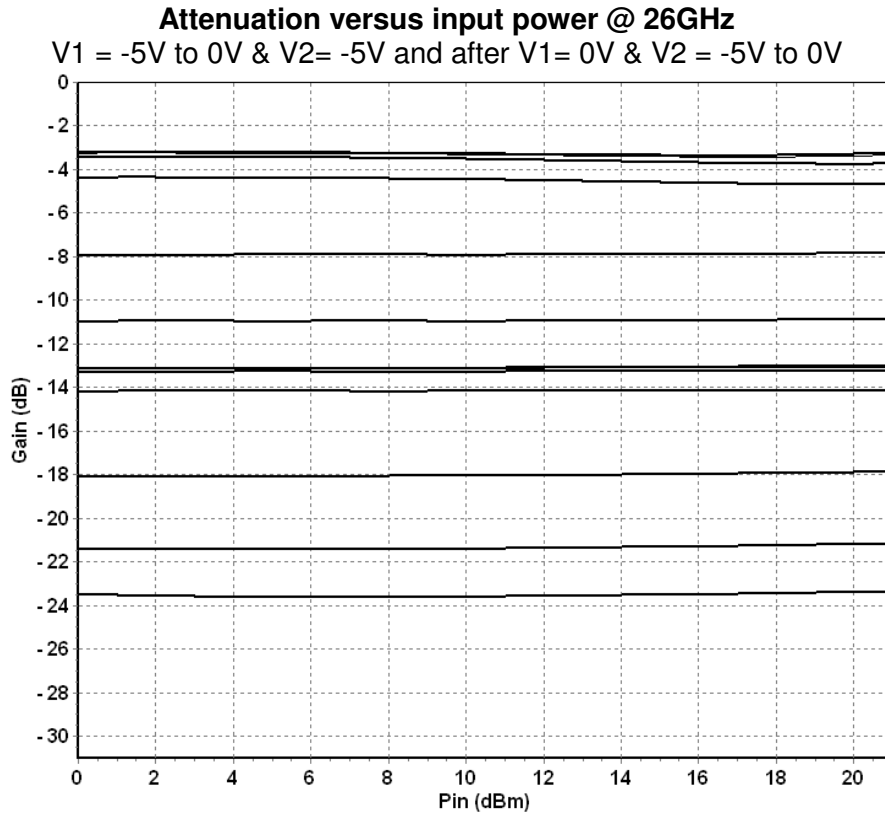
Output return loss versus frequency

V1 = -5V to 0V & V2= -5V and after V1= 0V & V2 = -5V to 0V

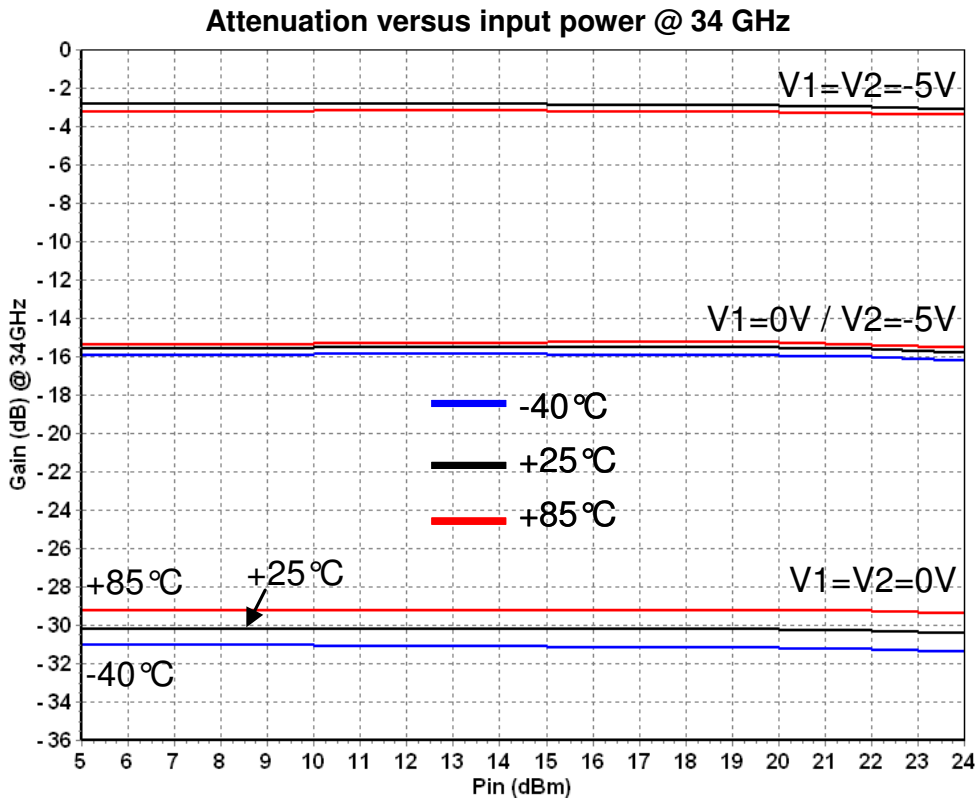
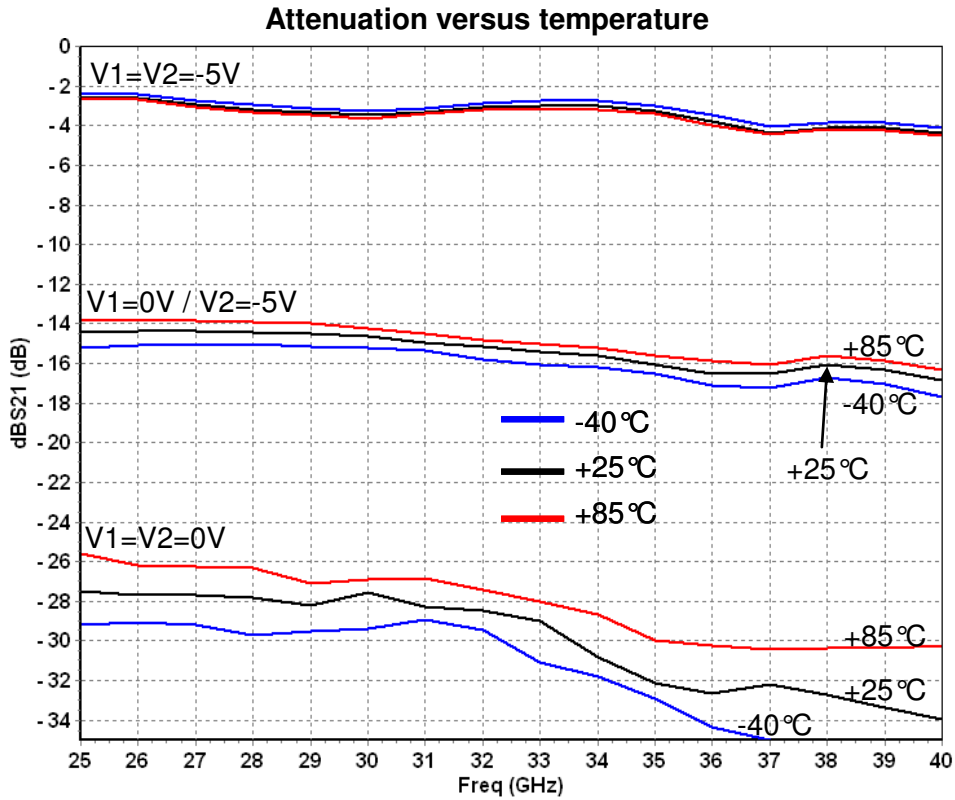


Typical on test fixture measurements

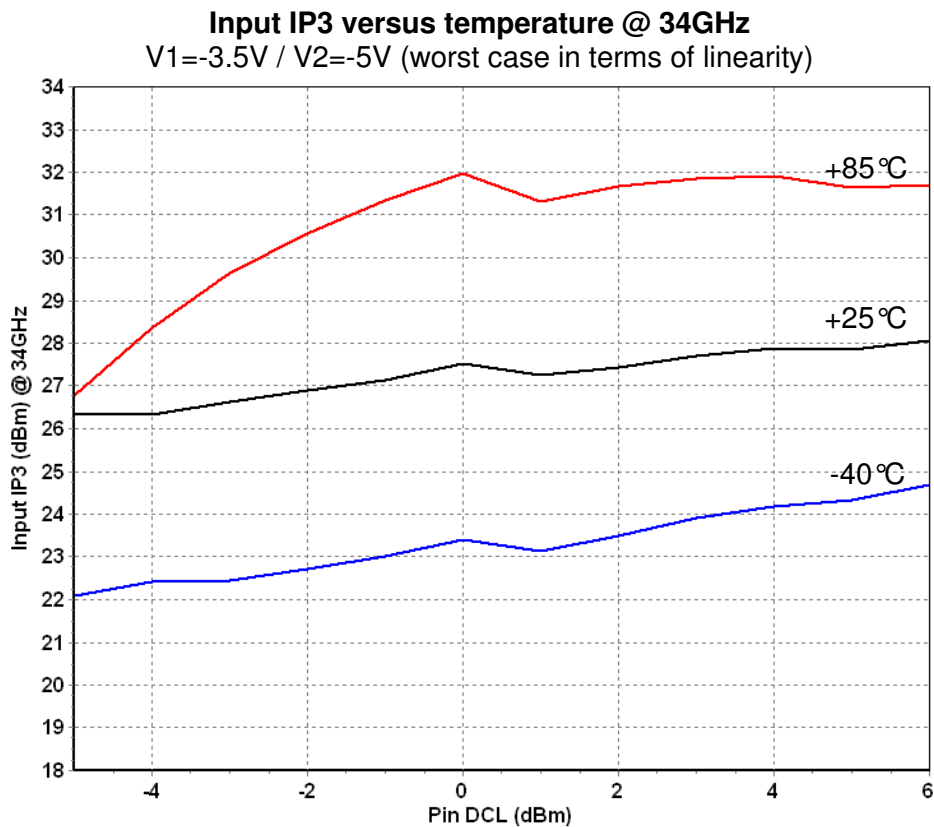
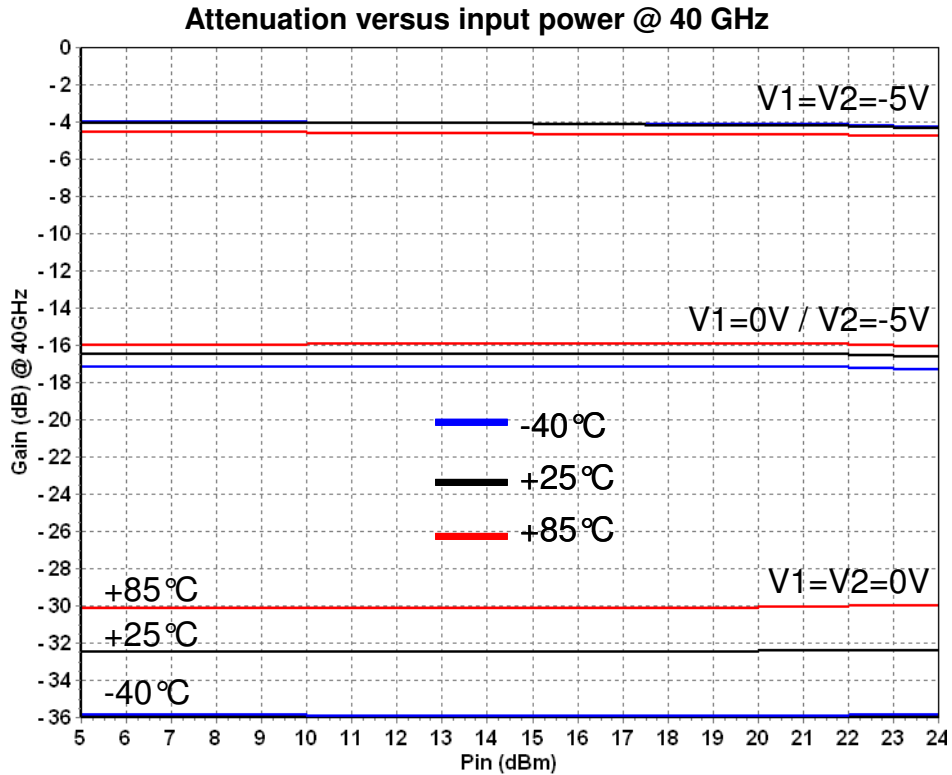
Tamb.= +25°C



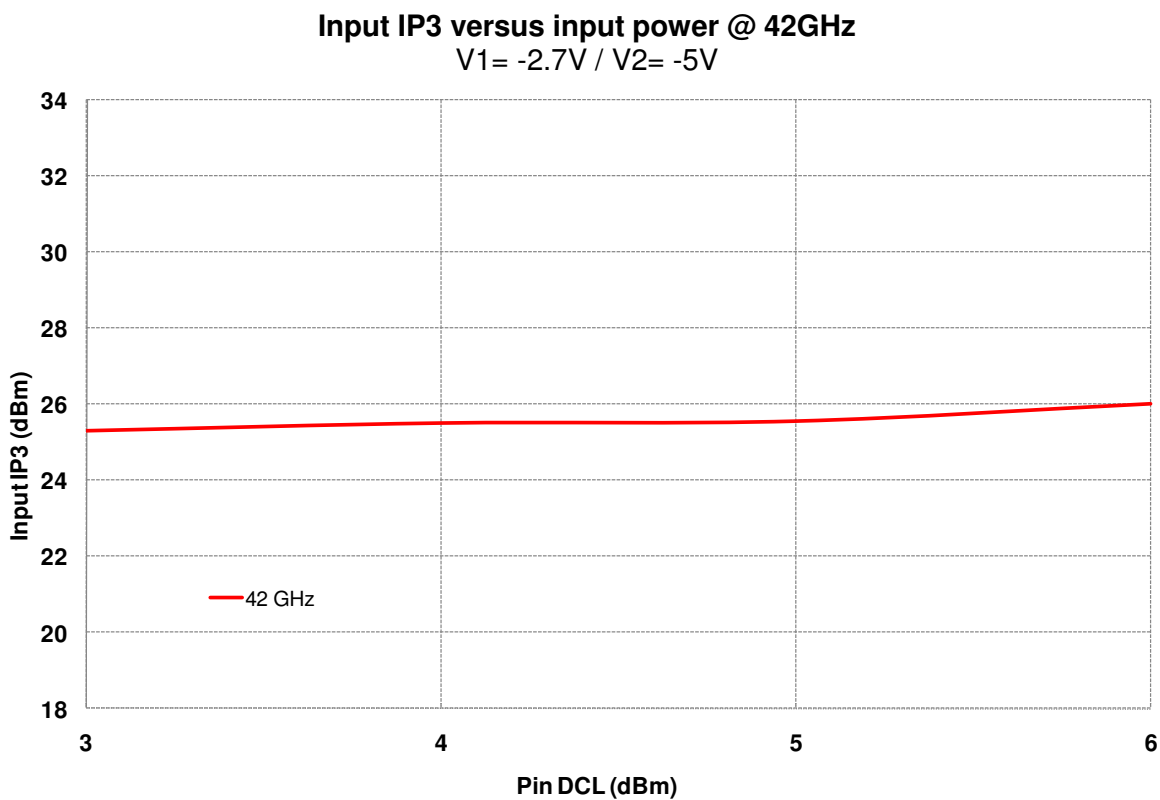
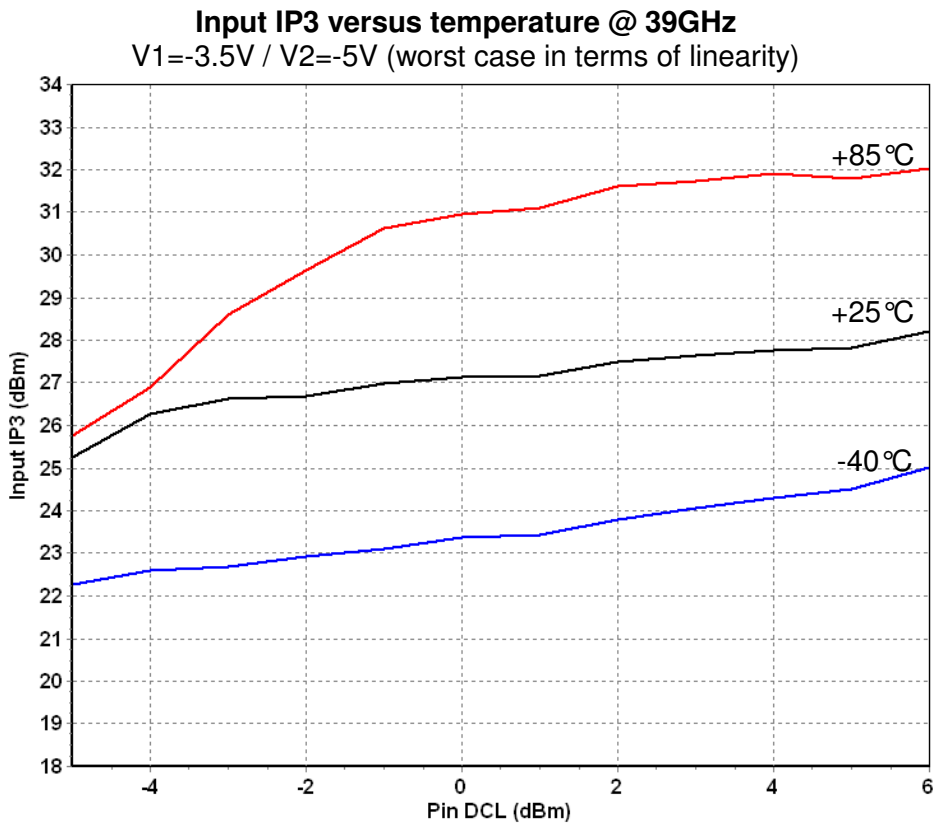
Typical on test fixture measurements



Typical on test fixture measurements



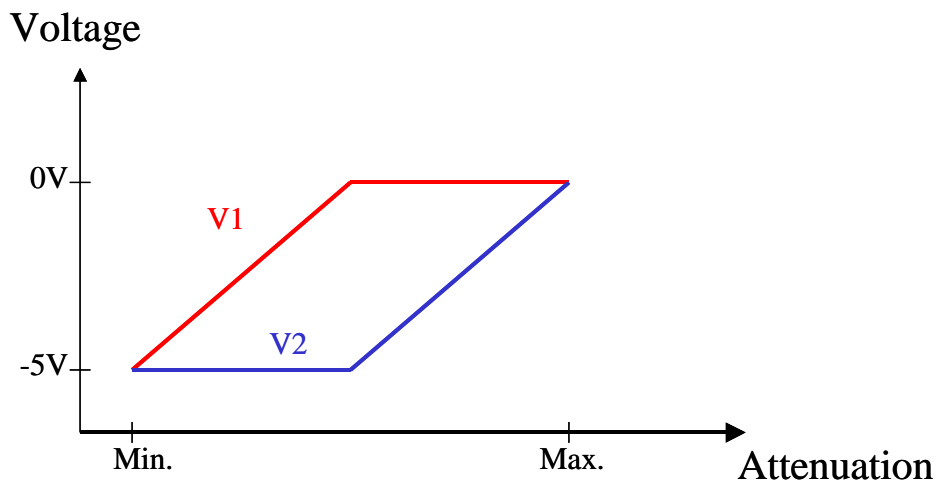
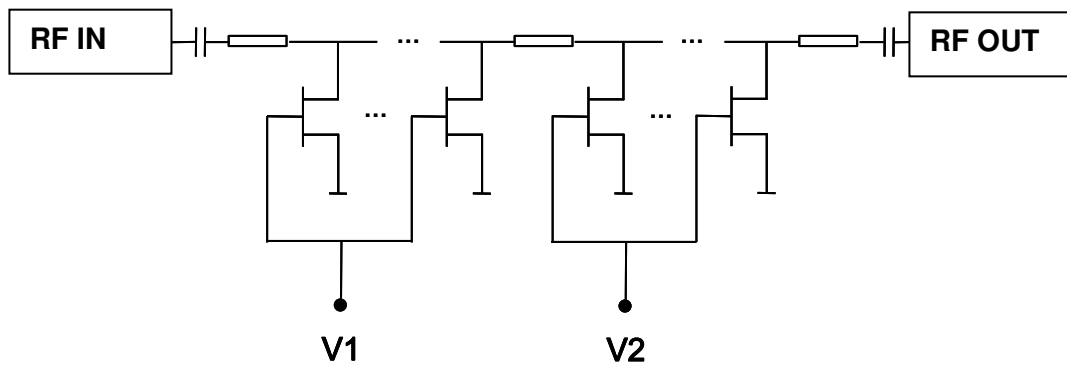
Typical on test fixture measurements



Biasing sequence

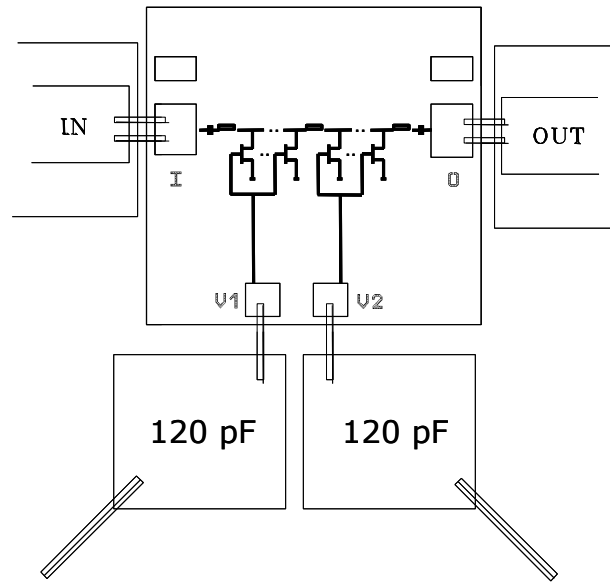
To obtain good performances in linearity, biasing voltage should be applied as following:

- Control of 1st stage attenuation with V1 from -5V to 0V, with V2 fixed at -5V
- Control of 2nd stage with V2 from -5V to 0V, with V1 fixed at 0V



This part could be also driven in Single Voltage Control, applying the same voltage from -5V to 0V on V1 and V2, leading to lower linearity performances

Chip Assembly and Mechanical Data

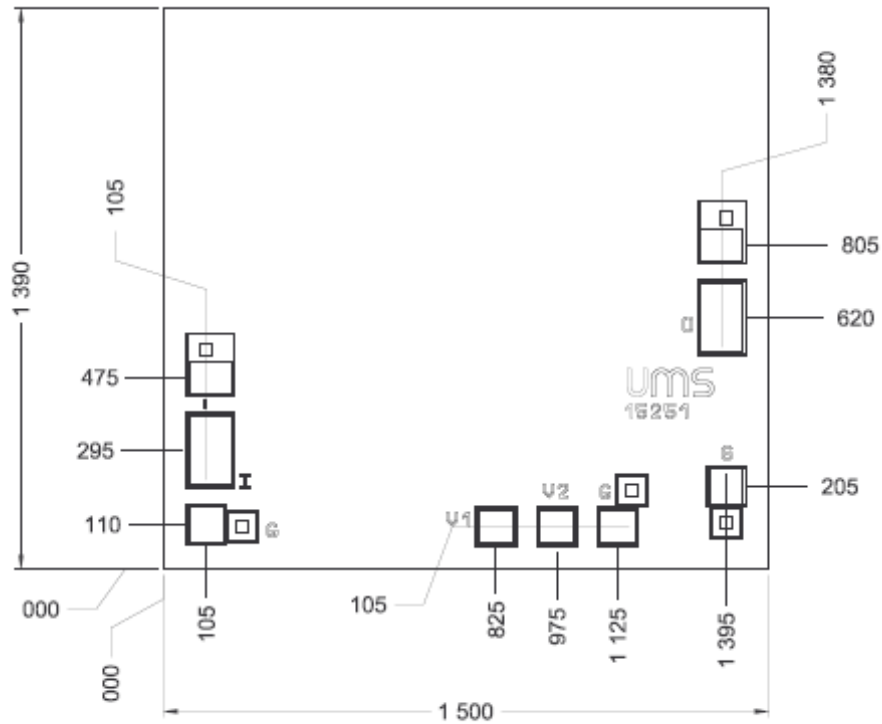


to V1 DC gate supply feed

to V2 DC gate supply feed

Note: Supply feed might be bypassed. 25 μ m diameter gold wire is to be preferred.

Bonding pad positions



UNITS μm
Tol $\pm 35\mu\text{m}$

(Chip thickness: 100 μm . All dimensions are in micrometers)

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Ordering Information

Chip form:

CHT4694-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**