0.6-4.5VIN, 1.8-5.25VOUT, 3.5µA, Low Input Voltage, High-Efficiency Boost + LDO

FEATURES

- Combines Low-power Boost + Low Dropout Linear Regulator (LDO)
- Boost Regulator
  - Input Voltage: 0.6V- 4.5V
  - Output Voltage: 1.8V- 5.25V
  - Efficiency: Up to 84%
  - No-Load Supply Current: 3.5µA
  - Delivers >100mA at $1.8V_{BO}$ from $1.2V_{BI}$
  - Shutdown Control
- Anti-Crush Capability
  - Prevents Input Voltage Collapse when powered with Weak/High Impedance power Sources
- Single-Inductor, Discontinuous Conduction Mode Scheme with Automatic Peak Current Adjustment
- LDO
  - Adjustable LDO Output Voltage: 1.8V- 5V
  - Dropout Voltage: 255mV @ 100mA
- 16-Pin, Low-Profile, Thermally-Enhanced 3mm x 3mm TQFN Package

APPLICATIONS

Coin Cell-Powered Portable Equipment
Single Cell Li-ion or Alkaline Powered Equipment
Solar or Mechanical Energy Harvesting
Wireless Microphones
Wireless Remote Sensors
RFID Tags
Blood Glucose Meters
Personal Health-Monitoring Devices

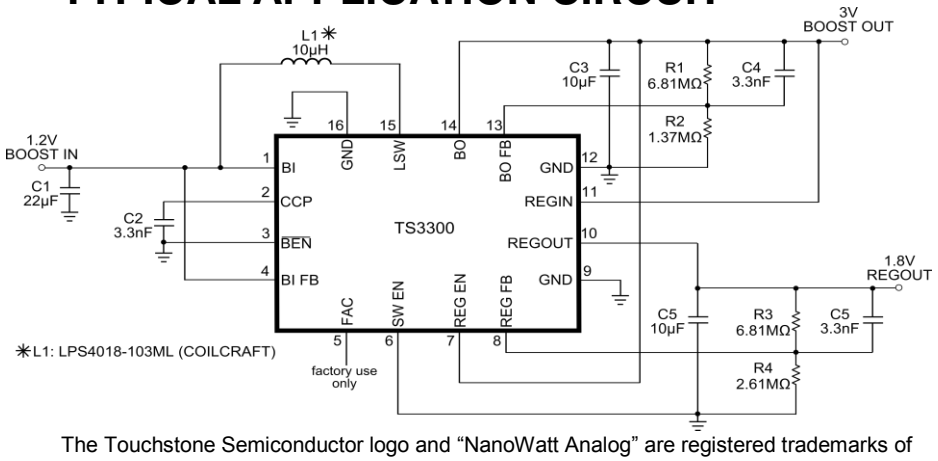
DESCRIPTION

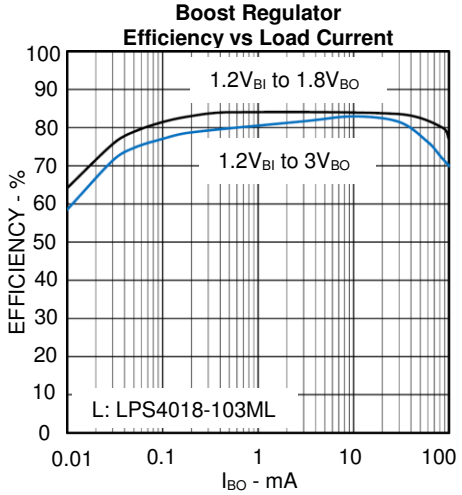
The TS3300 is a 1st-generation Touchstone Semi power management product that combines a high-efficiency boost regulator and a low dropout linear regulator (LDO) in one package. The boost regulator operates from a supply voltage as low as 0.6V and can deliver at least 75mA at $1.2V_{BI}$ to $3V_{BO}$, an industry first. The TS3300 LDO's input is connected to the output of the boost regulator, serving as a post-regulator for the boost, enabling a number of useful functions such as a buck-boost function. In power harvesting or peak load buffering applications, the LDO may post-regulate voltage buffered in a large capacitor or supercapacitor at boost's output. Finally, the LDO may be operated simply as an on/off load switch. The LDO can deliver up to 100mA output current at a dropout voltage of 255mV and reduce the ripple voltage out of the boost regulator by a factor of 3.

The TS3300's boost section includes an *anti-crush*™ feature to prevent the collapse of the input voltage to the boost regulator when the input is a weak (high impedance) source. If the input voltage drops below a determined voltage threshold (settable by a resistor divider), the boost regulator switching cycles are paused, effectively limiting the minimum input voltage. *Anti-crush*™ is useful in applications where a buffer capacitor at the boost's output can service burst loads, and the input source exhibits substantial source impedance (such as with an old battery, or at cold temperatures).

The TS3300 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, thermally-enhanced 16-pin 3x3mm TQFN package with an exposed back-side paddle.

TYPICAL APPLICATION CIRCUIT





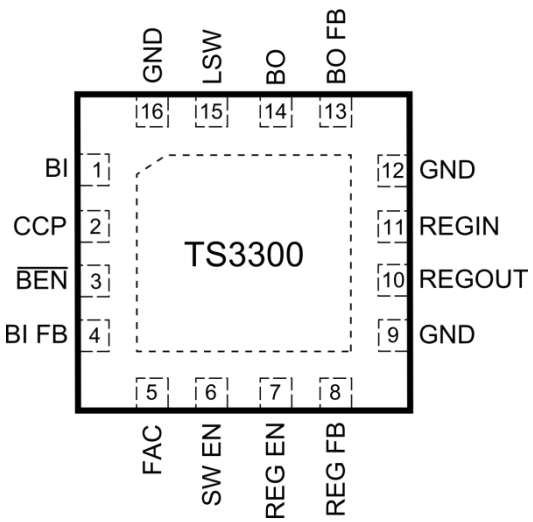
ABSOLUTE MAXIMUM RATINGS

BI to GND ..... -0.3V to V_{BO} +0.1V
CCP ..... -0.3V to +2.5V
$\overline{BEN}$ to GND ..... -0.3V to +5.75V
BI FB, REG FB, BO FB to GND ..... -0.3V to +5.75V
SW EN, REG EN to GND ..... -0.3V to +5.75V
BO, REG OUT, REG IN to GND ..... -0.3V to +5.75V
LSW to GND ..... -0.3V to +5.75V

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (Derate at 17.5mW/°C above +70°C) 1398mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Electrical and thermal stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



3mm x 3mm x 0.75mm QFN-EP 16L
TQ1633 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS3300ITQ1633TP	3300I	Tape & Reel	-----
TS3300ITQ1633T		Tape & Reel	3000

Lead-free Program: Touchstone Semiconductor supplies only lead-free packaging.

Consult Touchstone Semiconductor for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{BI} = 1.2V, V_{BO} = 3V, $V_{\overline{BEN}}$ = LOW, I_{BO}= 20mA, L = 10µH, C_{BO} = 22µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted. See Note 1.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST REGULATOR						
Minimum Input Boost Voltage	V_{BI_MIN}	I_{BO} = 0mA. T_A=25ºC		0.6	0.75	V
Maximum Input Boost Voltage	V_{BI_MAX}	Guaranteed by design	4.5			V
Output Boost Voltage Range	V_{BO}		1.8		5.25	V
Current Measured at BO	I_{B_Q}	I_{BO} = 0mA, $V_{BO\ FB}$ = 0.6V T_A =25°C		3.5		µA
Current Measured at BI				0.07		µA
Current Measured at BO		I_{BO} = 0mA, $V_{BO\ FB}$ = 0.6V, -40°C < T_A < +85°C			6	µA
Current Measured at BI					0.9	µA
Efficiency	Eff	V_{BI}= 1.2V, V_{BO}=1.8, I_{BO}=30mA		84		%
Boost Shutdown Supply Current	$I_{SHUTDOWN}$	Measured at BI. $V_{\overline{BEN}}$ = V_{BI} $V_{\overline{BEN}}$ = 0V T_A =25°C			100	nA
Boost Feedback Voltage during operation	$V_{BO\ FB}$	Output voltage accuracy: ± 4%	0.489	0.505	0.521	V
Boost Feedback Pin Current	$I_{BO\ FB}$			±0.1	±1	nA
Anti-Crush Feedback Voltage	$V_{BI\ FB}$	V_{BI} ≥ 0.6V	0.363	0.392	0.425	V
Anti-Crush Feedback Voltage Hysteresis	$V_{BI\ FB\_HYST}$			50		mV
Boost Enable Threshold	$V_{\overline{BEN}}$	V_{IL}	0.2			V
		V_{IH}			V_{BI} -0.05	V
Boost Enable Hysteresis	$V_{\overline{BEN}\_HYST}$			200		mV
Inductor Peak Current	I_{PK}	No Load	365			mA
Inductor Valley Current	I_V			10		mA
N-channel ON Resistance	$Rds_{N\text{-}CH}$			0.27		Ω
P-channel ON Resistance	$Rds_{P\text{-}CH}$			0.48		Ω

ELECTRICAL CHARACTERISTICS

V_{REGIN} = V_{BO} = 3V, V_{REGOUT} = 1.8V, $V_{REG\ EN}$ = HIGH, I_{REGOUT} = 20mA, C_{REGOUT} = 10µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted. See Note 1.

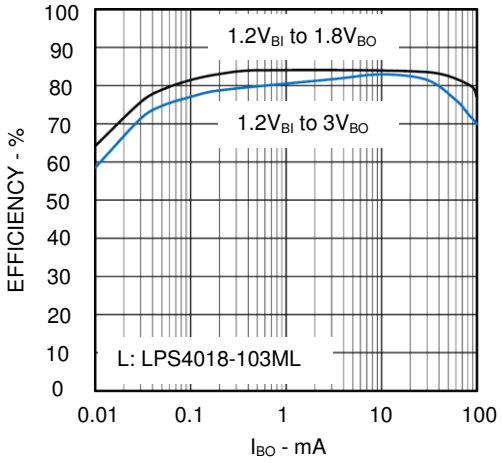
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR							
DC Output Accuracy	V_{REGOUT}	2.3V ≤ V_{REGIN} ≤ 5V 0mA ≤ I_{REGOUT} ≤ 20mA $V_{REG\ FB}$ = 505mV			2.5		%
			-40ºC ≤ T_A ≤ 85ºC	-3.5		3.5	%
Input Voltage Range	V_{REGIN}	Guaranteed by design		1.8		5.25	V
Output Voltage Range	V_{REGOUT}			1.8		5	V
Input Supply Current	I_{REGIN}	I_{REGOUT} = 0mA, $V_{REG\ EN}$ = V_{REGIN}			0.4	1	µA
Line Regulation	$\Delta V_{REGOUT}/\Delta V_{REGIN}$	V_{REGOUT} +0.5V ≤ V_{REGIN} ≤ 5V		-1		1	%
Load Regulation	$\Delta V_{REGOUT}/\Delta I_{REGOUT}$	10mA ≤ I_{REGOUT} ≤ 20mA		-1		1	%
		0mA ≤ I_{REGOUT} ≤ 20mA		-1.5		1.5	%
Drop Out Voltage	VDO				40		mV
Output Current Limit	ICL				150		mA
Power Supply Rejection Ratio	PSRR	C_{REGOUT} = 22µF I_{REGOUT} = 100mA	f = 10Hz		-70		dB
			f = 100Hz		-50		dB
			f = 1kHz		-36		dB
Startup Time	t_{STR}					1	ms
Linear Regulator Enable Voltage	$V_{REG\ EN}$	V_{IL} (CMOS logic)				0.2 x V_{REGIN}	V
		V_{IH} (CMOS logic)		0.8 xV_{REGIN}			V
Linear Regulator Enable Hysteresis	$V_{REG\ EN\_HYST}$				100		mV
Enable Pin Current	$I_{REG\ EN}$					10	nA
SWITCH Rds_{ON}	R_{SW}	$V_{SW\ EN}$ = HIGH. Measured from REGIN to REGOUT			0.9	1.2	Ω
SWITCH Enable Voltage	$V_{SW\ EN}$	V_{IL} (CMOS logic)				0.2 x V_{REGIN}	V
		V_{IH} (CMOS logic)		0.8 xV_{REGIN}			V
Regulator Feedback Pin Current	$I_{REG\ FB}$				±0.1	±1	nA

Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by characterization for T_A = T_{MIN} to T_{MAX}, as specified.

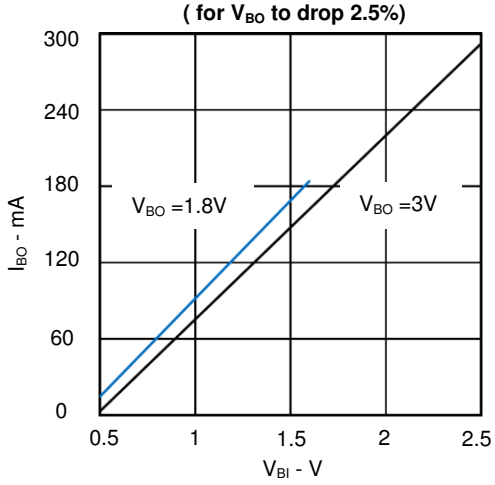
TYPICAL PERFORMANCE CHARACTERISTICS

V_{BI} = 1.2V, V_{BO} = 3V, $V_{\overline{BEN}}$ = LOW, I_{BO} = 0A, L = 10µH (LPS4018-103ML), C_{BO} = 22µF, C_{BI} = 22µF, V_{REGIN} = V_{BO} = 3V, V_{REGOUT} = 1.8V, I_{REGOUT} = 0A, C_{REGOUT} = 10µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

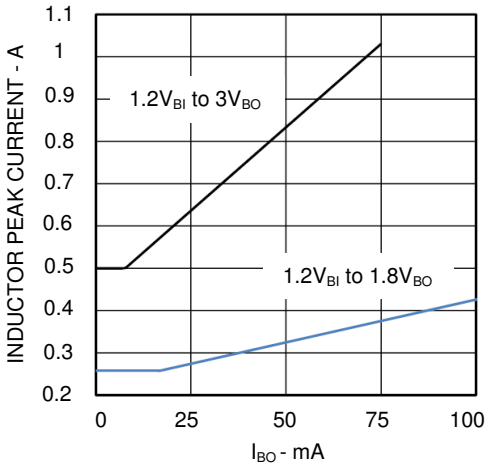
Boost Regulator Efficiency vs Load Current



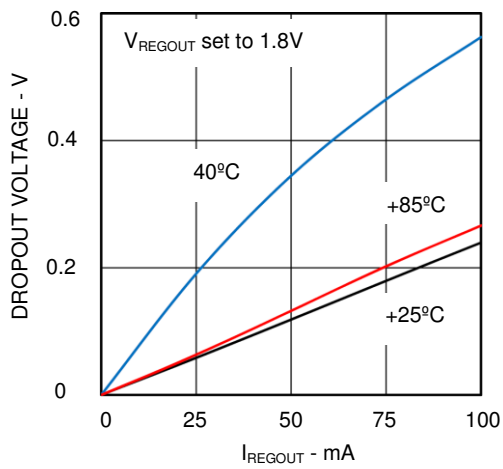
Boost Regulator Maximum Output Current vs V_{BI} (for V_{BO} to drop 2.5%)



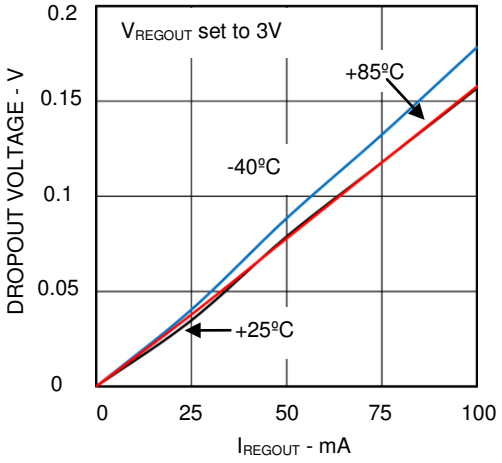
Inductor Peak Current vs Load Current



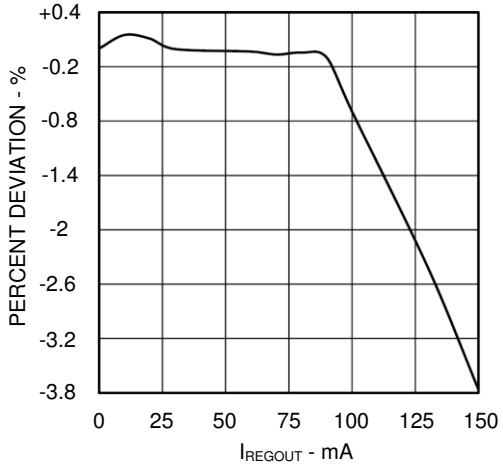
LDO Dropout Voltage vs Load Current



LDO Dropout Voltage vs Load Current



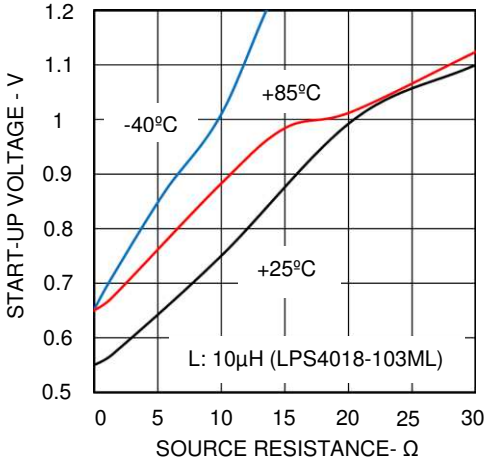
LDO Output Voltage Accuracy vs Load Current



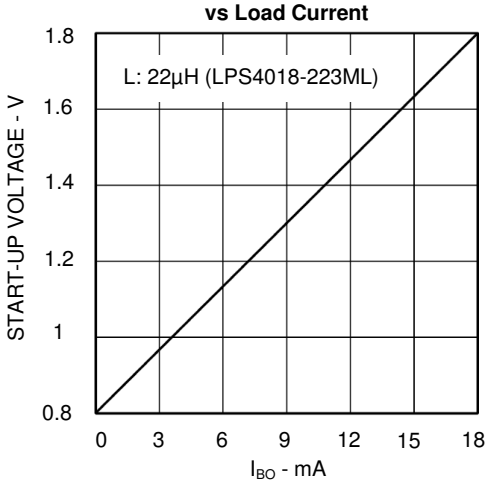
TYPICAL PERFORMANCE CHARACTERISTICS

V_{BI} = 1.2V, V_{BO} = 3V, $V_{\overline{BEN}}$ = LOW, I_{BO} = 0A, L = 10µH (LPS4018-103ML), C_{BO} = 22µF, C_{BI} = 22µF, V_{REGIN} = V_{BO} = 3V, V_{REGOUT} = 1.8V, I_{REGOUT} = 0A, C_{REGOUT} = 10µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

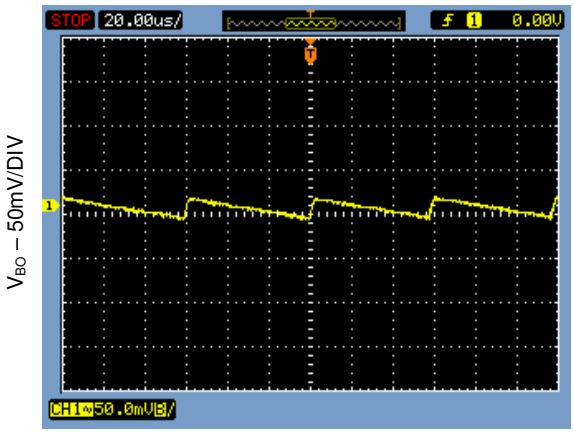
Boost Minimum Start-Up Voltage vs Source Resistance



Boost Minimum Start-Up Voltage vs Load Current

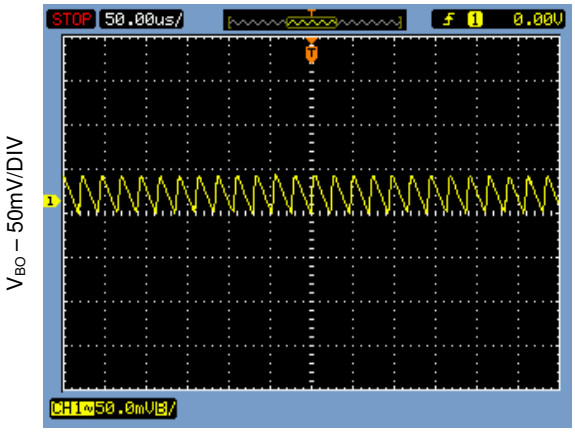


Boost Regulator Output Voltage Ripple
V_{BI} = 1.2V, V_{BO} = 1.8V, C_{BO}= 22µF, I_{BO} = 5mA



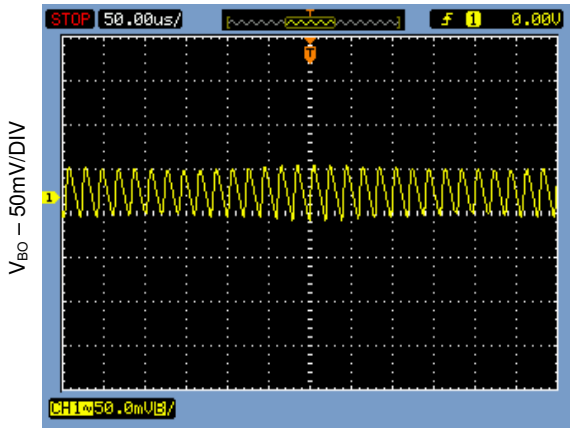
20µs/DIV

Boost Regulator Output Voltage Ripple
V_{BI} = 1.2V, V_{BO} = 1.8V, C_{BO}= 22µF, I_{BO} = 40mA



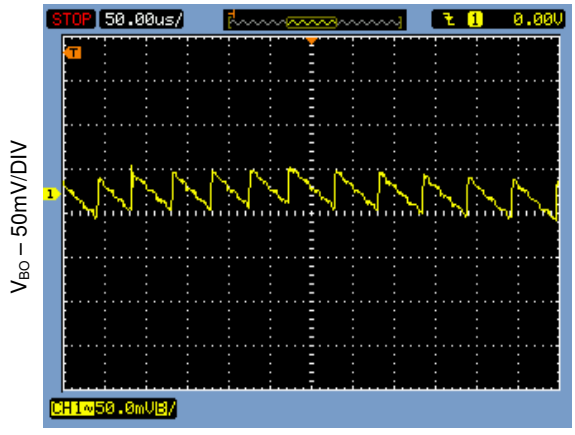
50µs/DIV

Boost Regulator Output Voltage Ripple
V_{BI} = 1.2V, V_{BO} = 1.8V, C_{BO}= 22µF, I_{BO} = 80mA



50µs/DIV

Boost Regulator Output Voltage Ripple
V_{BI} = 1.2V, V_{BO} = 3V, C_{BO}= 22µF, I_{BO} = 5mA

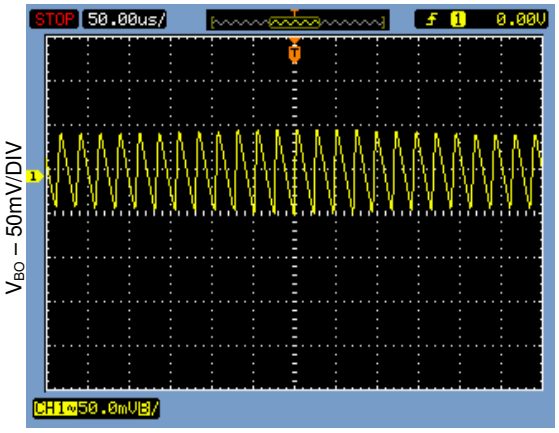


50µs/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

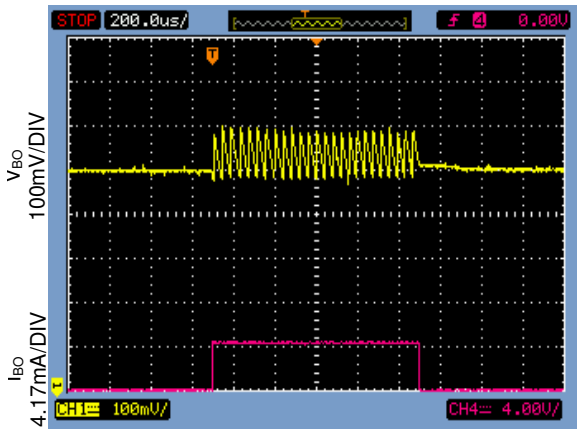
V_{BI} = 1.2V, V_{BO} = 3V, $V_{\overline{BEN}}$ = LOW, I_{BO} = 0A, L = 10µH (LPS4018-103ML), C_{BO} = 22µF, C_{BI} = 22µF, V_{REGIN} = V_{BO} = 3V, V_{REGOUT} = 1.8V, I_{REGOUT} = 0A, C_{REGOUT} = 10µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

Boost Regulator Output Voltage Ripple
V_{BI} = 1.2V, V_{BO} = 3V, C_{BO}= 22µF, I_{BO} = 80mA



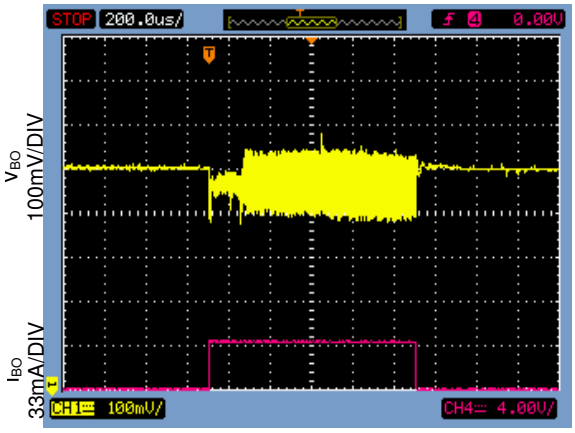
50µs/DIV

Boost Regulator Load Step Response
V_{BI} = 1.2V, V_{BO} = 3V, C_{BO}= 10µF, I_{BO} = 5mA



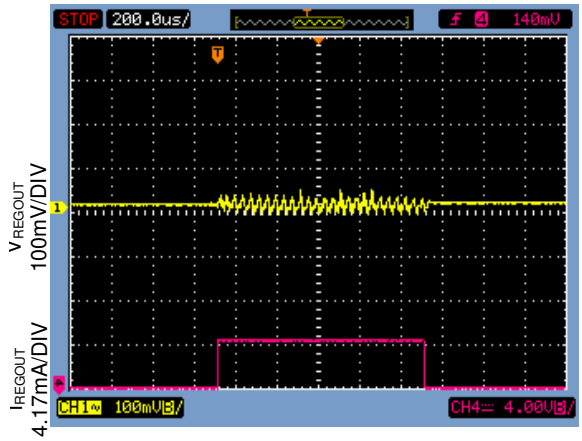
200µs/DIV

Boost Regulator Load Step Response
V_{BI} = 1.2V, V_{BO} = 3V, C_{BO}= 10µF, I_{BO} = 40mA



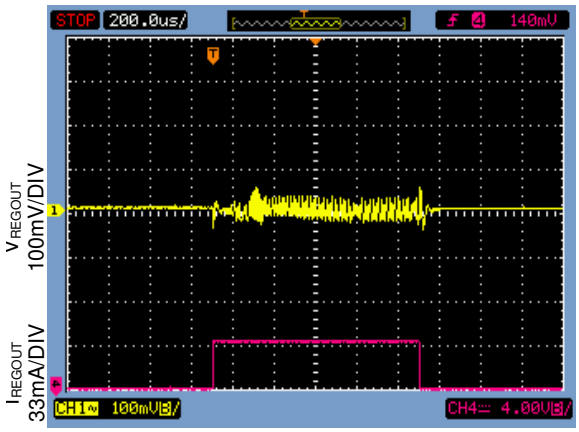
200µs/DIV

LDO Load Step Response
V_{BI} = 1.2V, V_{BO} = 3V, C_{REGOUT}= 10µF, I_{BO} = 5mA



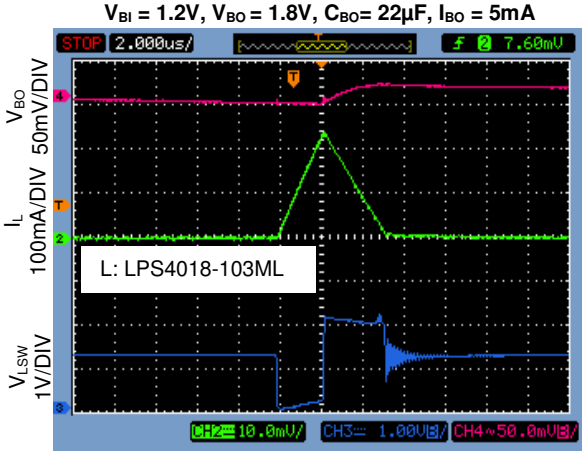
200µs/DIV

LDO Load Step Response
V_{BI} = 1.2V, V_{BO} = 3V, C_{REGOUT}= 10µF, I_{BO} = 40mA



200µs/DIV

Boost Regulator Output Voltage Ripple, Inductor Current, and LSW Voltage
V_{BI} = 1.2V, V_{BO} = 1.8V, C_{BO}= 22µF, I_{BO} = 5mA

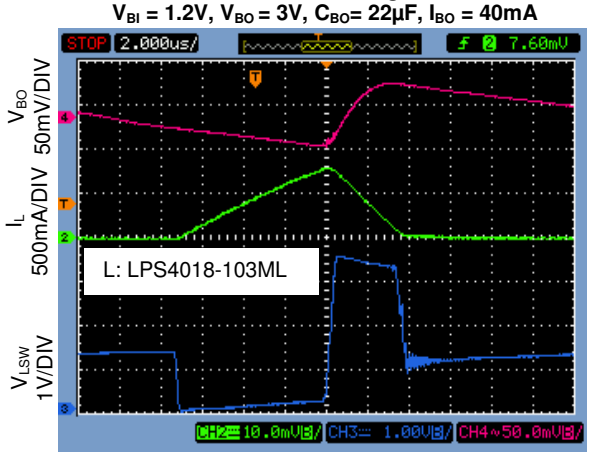


2µs/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

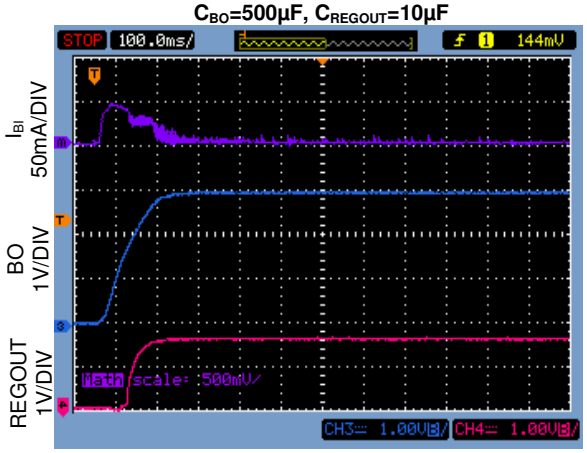
V_{BI} = 1.2V, V_{BO} = 3V, $V_{\overline{BEN}}$ = LOW, I_{BO} = 0A, L = 10µH (LPS4018-103ML), C_{BO} = 22µF, C_{BI} = 22µF, V_{REGIN} = V_{BO} = 3V, V_{REGOUT} = 1.8V, I_{REGOUT} = 0A, C_{REGOUT} = 10µF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

Boost Regulator Output Voltage Ripple, Inductor Current, and LSW Voltage
V_{BI} = 1.2V, V_{BO} = 3V, C_{BO}= 22µF, I_{BO} = 40mA



2µs/DIV

Large Output Capacitor Start-up with Anti-Crush at 0.9V
V_{BI}=1.2V, ESR of V_{BI}=10Ω, V_{BO}=V_{REGIN}=3V, V_{REGOUT}=1.8V, C_{BO}=500µF, C_{REGOUT}=10µF

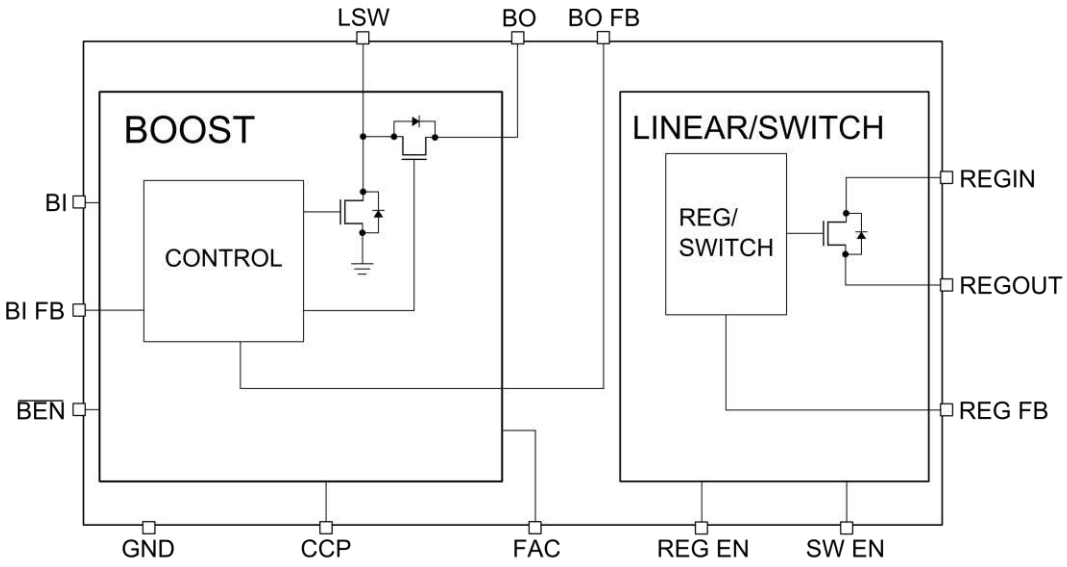


100ms/DIV

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	BIN	Boost Input. Bypass this pin with a 22µF ceramic capacitor in close proximity to the TS3300.
2	CCP	Charge Pump Capacitor. Place a 3.3nF capacitor between this pin and GND
3	$\overline{BEN}$	Boost Enable (active low). To enable the TS3300, connect this to GND. To disable the TS3300, set the voltage to greater than V_{BI} – 50mV.
4	BI FB	Boost Input Feedback for Anti-Crush Voltage Setting. The BI FB pin voltage is 392mV. To set the anti-crush voltage, refer to the *Applications Information* section and to Figure 7.
5	FAC	Factory use only. Do not connect to GND or VDD. Leave open.
6	SW EN	Switch Enable. When SW EN is high and REG EN is low, the internal FET/SWITCH connects the LDO output to the LDO input. The internal FET has an Rds_{ON} = 1.2Ω. Refer to Table 1.
7	REG EN	LDO Regulator Enable. When REG EN is high and SW EN is low, the LDO is under normal operation. Refer to Table 1.
8	REG FB	LDO Regulator Output Feedback. The REG FB pin voltage is 505mV. REG FB coupled with a voltage divider circuit sets the LDO output voltage. Refer to Figure 3.
9	GND	Ground. Connect this pin to the analog ground plane
10	REGOUT	LDO Regulator Output Voltage. A minimum output capacitance of 10µF is recommended to be placed from this pin to GND. To set the LDO output voltage, use a voltage divider circuit along with the REG FB pin as shown in Figure 3.
11	REGIN	LDO Regulator Input/Boost Output. REGIN should always be connected to the boost regulator output voltage pin BO. BO is always the input to the LDO. Do not apply an external supply voltage to this pin.
12	GND	Ground. Connect this pin to the analog ground plane.
13	BO FB	Boost Output Feedback. The BO FB pin voltage is 505mV. BO FB coupled with a voltage divider circuit sets the boost regulator output voltage. Refer to Figure 2.
14	BO	Boost Regulator Output Voltage. A minimum output capacitance of 10µF is recommended to be placed from this pin to GND. To set the boost regulator output voltage, use a voltage divider circuit along with the BO FB pin. Refer to Figure 2.
15	LSW	Coil is a low-ESR, high-saturation current, shielded inductor. A 10µH inductor is recommended for most applications and is to be placed from this pin to the input of the boost regulator BI. Furthermore, there should exist at least an 8% margin between the saturation current of the inductor and the peak inductor current for a given set of operating conditions.
16	GND	Ground. Connect this pin to the analog ground plane.
EP	–	For best electrical and thermal performance, connect exposed paddle to GND.

BLOCK DIAGRAM



THEORY OF OPERATION

The TS3300 is a power management product that combines a high-efficiency boost regulator and a linear regulator into one package. It is the industry's 1st boost regulator + linear regulator where the boost regulator can operate from supply voltages as low as 0.6V and can deliver at least 75mA at $1.2V_{BI}$ and $3V_{BO}$. Under no-load conditions, the boost regulator idles at 3.5µA. The internal, low-dropout linear regulator is driven by the output of the boost regulator. It can deliver up to 100mA output current at a dropout voltage of 255mV and reduce the ripple voltage out of the boost regulator by a factor of 3.

BOOST REGULATOR

At start-up, an internal low voltage oscillator in the start-up control circuitry drives the gate of the internal FET to charge the load capacitor. Once the output voltage reaches approximately 1.1V, the main control circuitry starts to operate.

With an adjustable peak inductor current, the TS3300 can provide up to 84% efficiency with a $1.2V_{BI}$ and $3V_{BO}$. Refer to Figure 1. The input and output supply voltage range for the boost regulator is from 0.6V to 4.5V and 1.8V to 5.25V, respectively.

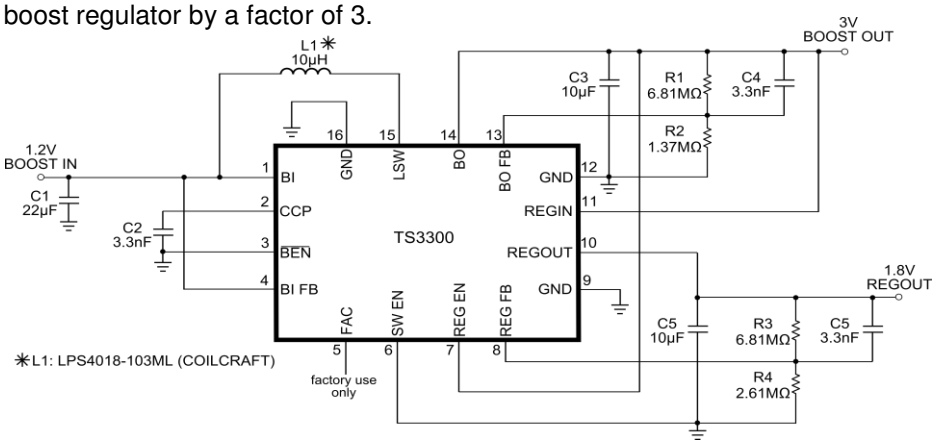


Figure 1: 1.2V Input to 3V Boost Regulator Output Voltage and to 1.8V LDO Output Voltage Circuit

The output voltage can be set via a voltage divider circuit as shown in Figure 2. The output feedback (BO FB) pin is 505mV. It is recommended to use

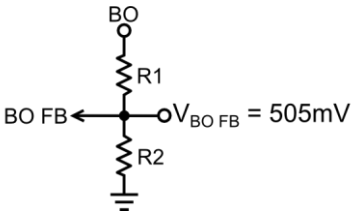


Figure 2: Setting the Boost Output Voltage with a Voltage Divider

large resistor values to minimize additional current draw at the output. Resistors values less than 8MΩ are recommended. Using the following equation to solve for R1 for a given R2 value, the output voltage can be set:

$$R1 = \frac{(V_{BO} - 0.505)R2}{0.505}$$

To set a 3V output voltage with R2 = 1.37MΩ, R1 is calculated to be 6.77MΩ. A 1% standard resistor value of 6.81MΩ can be selected. This results in an output voltage of 3.02V.

A shutdown ($\overline{BEN}$) pin is also available to shutdown the boost regulator. The boost regulator is in shutdown mode when $\overline{BEN}$ is LOW and supply current reduces to 0.1µA.

LDO Post-Regulator

The input and output supply voltage range for the LDO is from 2.3V to 5.25V and 1.8V to 5V, respectively, where the LDO input is driven by the output of the boost regulator. The output voltage can be set via a voltage divider circuit as shown in Figure 3.

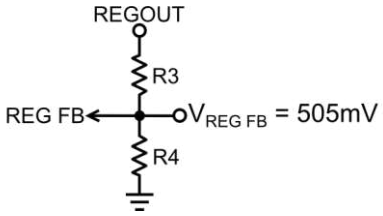


Figure 3: Setting the LDO Output Voltage with a Voltage Divider

The output feedback (REG FB) pin is 505mV. It is recommended to use the largest resistor values to minimize additional current draw at the output. Using the following equation to solve for R3 for a given R4 value, the output voltage can be set:

$$R3 = \frac{(V_{REGOUT} - 0.505)R4}{0.505}$$

To set a 1.8V output voltage with R4 = 2.61MΩ, R3 is calculated to be 6.69MΩ. A 1% standard resistor value of 6.81MΩ can be selected. This results in an output voltage of 1.82V.

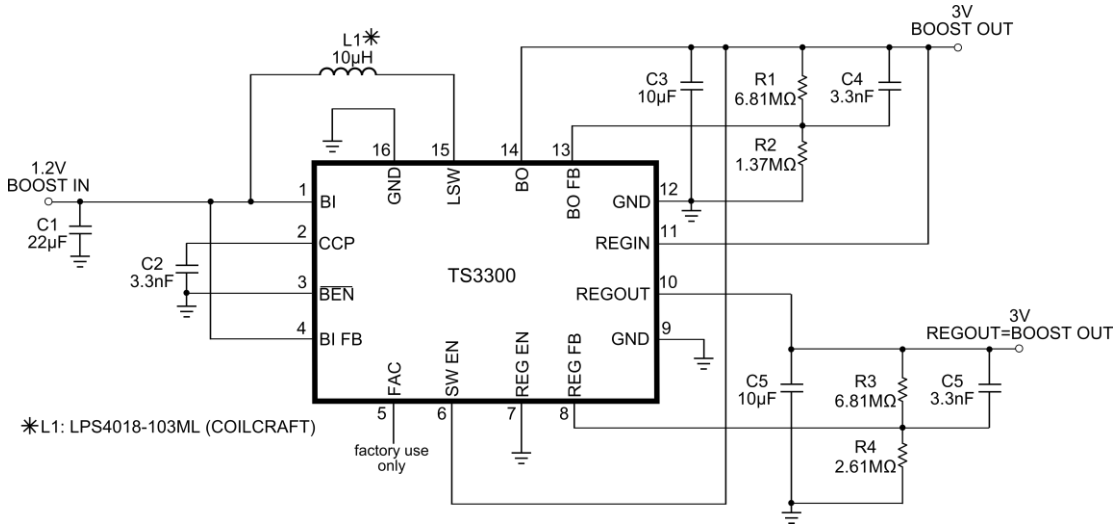


Figure 4: TS3300 LDO FET/Switch Enabled Circuit

The LDO was designed to operate in conjunction with the boost regulator where the output of the boost regulator is connected to the input to the linear regulator. The LDO can provide an output voltage based on the resistor divider circuit as shown in Figure 3 or the output voltage can be set to the input voltage where the internal switch/FET is fully enhanced. Table 1 summarizes the settings for pins REG EN and SW EN. Figure 4 shows the configuration where the internal switch/FET is fully enhanced (SW EN =high, REG EN = low) so the boost output is equal to the LDO output. The LDO can be shutdown by connecting the REF FB pin to BO when SW EN = low and REG EN = high.

SW EN	REG EN	CONDITION	FUNCTION
low	high	Connect REG EN pin to BO pin	LDO Normal Operation
		Connect REG FB pin to BO pin	LDO Shutdown
high	low	Connect SW EN pin to BO pin	Internal FET Hard-on

Table 1. LDO REG EN and SW EN Settings

APPLICATIONS INFORMATION

Inductor Selection

A low ESR, shielded 10µH inductor is recommended for most applications and provides the best compromise between efficiency and size. A low loss ferrite and low dc resistance (DCR) inductor is best for optimal efficiency. Furthermore, there should exist at least an 8% margin between the saturation current of the inductor and the peak inductor current for a given set of operating conditions. Table 2 provides a list of inductor manufactures. Refer to the Inductor Peak Current vs Load Current plot in the "Typical Performance Characteristics" section. This plot shows how the inductor peak current varies with load current with a LPS4018-103ML inductor from Coilcraft.

Inductors	
Supplier	**Website**
Coilcraft	www.coilcraft.com
Murata	www.murata.com
Sumida	www.sumida.com
Capacitors	
Taiyo Yuden	www.t-yuden.com
Murata	www.murata.com
AVX	www.avxcorp.com
TDK	www.component.tdk.com

Table 2. Inductor and Capacitor Manufactures

Input and Output Capacitor Selection

For the boost regulator, a low ESR ceramic input and output capacitor of at least 10µF is recommended to be placed as close as possible to the BI and BO pin. Output voltage ripple can be reduced by increasing the value of the output capacitor while providing improved transient response. Ceramic capacitors with X5R dielectric are recommended.

For the LDO, a low ESR ceramic input and output capacitor of at least 10µF is recommended to be placed as close as possible to the REG OUT pin. Refer to Table 2 for a list of inductor and capacitor manufacturers.

Buck-Boost Function

The TS3300 can act as a buck-boost device. For instance, if two 1.5V alkaline cells are used to power the TS3300, the boost output voltage (V_{BO}) can be set to 5V and the LDO output voltage (V_{REGOUT}) can be set to 2.5V. The output voltage for the boost regulator and the LDO can be set according to Figure 2 and 3, respectively.

Boost Input Anti-Crush™ Feature

The TS3300 includes an *anti-crush™* feature to prevent the collapse of the input voltage to the boost regulator when the input is a weak (high impedance) source. If the input voltage drops below a determined voltage threshold (settable by a resistor divider), the boost regulator switching cycles are paused, effectively limiting the minimum input voltage. *Anti-crush™* is useful in applications where a buffer capacitor at the boost's output can service burst loads, and the input source exhibits substantial source impedance (such as with an old battery, or at cold temperatures).

To set the anti-crush™ voltage, a feedback pin (BI FB) in conjunction with a voltage divider circuit can be implemented as shown in Figure 7. The feedback pin voltage is 392mV. It is recommended to use large resistor values to minimize additional current draw at the input.

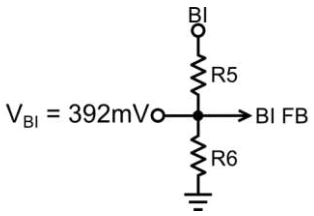


Figure 7: Setting the Anti-Crush™ Voltage with a Voltage Divider

Using the following equation to solve for R5 for a given R6 value, the output voltage can be set:

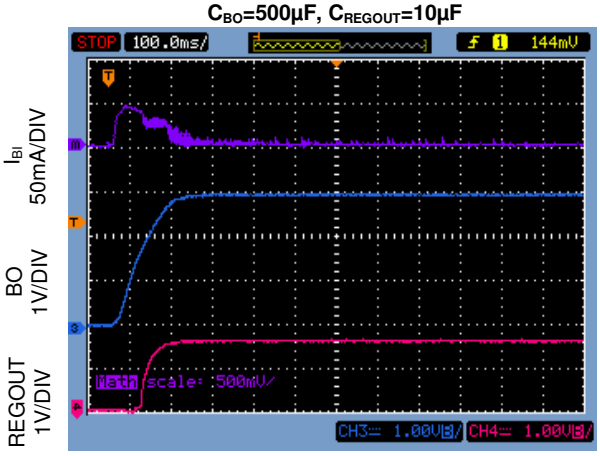
$$R5=\frac{(V_{ANTI\text{-}CRUSH™} - 0.392)R6}{0.392}$$

To set a 0.8V output voltage with R6 = 1.37MΩ, R5 is calculated to be 1.42MΩ. A 1% standard resistor value of 1.37MΩ can be selected. This results in an anti-crush voltage of 784mV. The anti-crush™ voltage is to be set above the minimum input voltage specification of the TS3300.

Figure 5 shows a scope capture of the anti-crush™ feature in action at start-up under a heavy capacitive load of 500µF and an input source impedance of 10Ω. A high source impedance is typical of a weak battery source. The measurement was performed with the anti-crush™ voltage set to 0.9V. The purple, blue, and pink trace represent the input current, boost output voltage, and LDO output voltage, respectively. At start-up, the current rises up to 50mA and drops to approximately 30mA for approximately 40ms in order to charge the output capacitor. At this point, the voltage to the input of the TS3300 is 0.9V until the boost output achieves regulation and in turn, the LDO output voltage achieves regulation as well.

Figure 6 shows a scope capture of the load step response. The measurement was performed with the anti-crush™ voltage set to 0.9V. As the output of the LDO is pulsed with a 100mA load every 100ms for 1ms as shown by the pink curve, the input voltage after a battery impedance of 10Ω drops from 1.2V to 0.9V as shown by the blue curve and the boost output voltage drops by only 160mV as shown by the yellow curve. The TS3300 quickly replenishes the 500µF capacitor and the output of the boost regulator returns to 3V. Note that the LDO remains regulated and is unaffected by the load step.

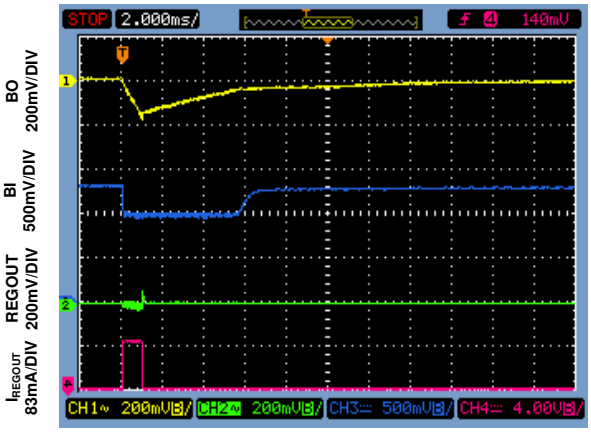
Large Output Capacitor Start-up with Anti-Crush™ at 0.9V
V_{BI}=1.2V, ESR of V_{BI} =10Ω, V_{BO}=V_{REGIN}=3V, V_{REGOUT}=1.8V, C_{BO}=500µF, C_{REGOUT}=10µF



100ms/DIV

Figure 5: Using the Anti-Crush™ Feature under a Heavy Capacitive Load (500µF) and a 10Ω Boost Input Source Impedance at Start-up

Load Step Response with Anti-Crush™ at 0.9V
V_{BI}=1.2V, ESR of V_{BI} =10Ω, V_{BO}=V_{REGIN}=3V, V_{REGOUT}=1.8V, C_{BO}=500µF, C_{REGOUT}=10µF, I_{REGOUT}=100mA pulse



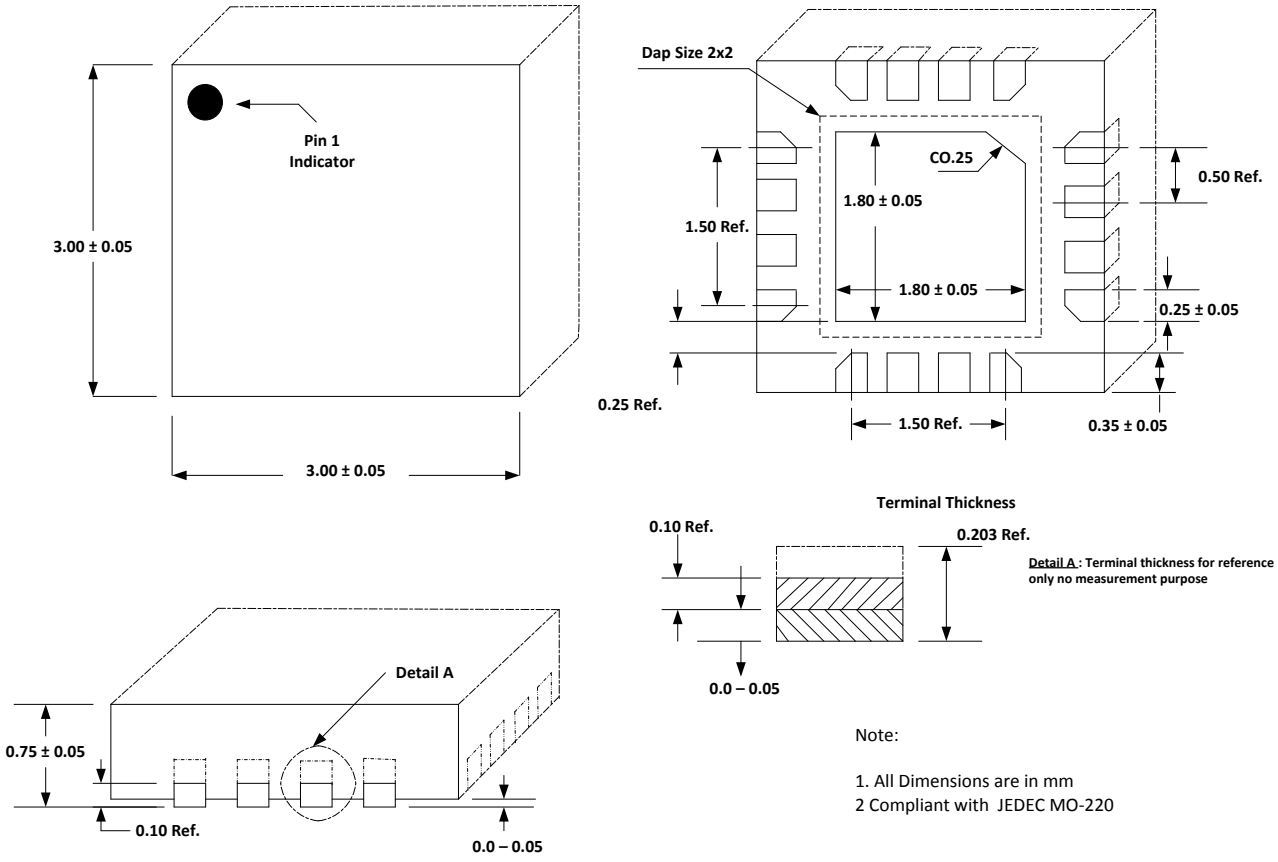
2ms/DIV

Figure 6: Using the Anti-Crush™ Feature to Maintain Regulation of the Boost Regulator and LDO Output Voltage

PACKAGE OUTLINE DRAWING

16-Pin TQFN33 Package Outline Drawing

(N.B., Drawings are not to scale)



Note:

1. All Dimensions are in mm
2 Compliant with JEDEC MO-220