YAMAR Electronics Ltd
Preliminary *Data Sheet*

SIG61 - Smart Slave for Multiplex Powerline Network

This information is preliminary and may be changed without notice

1 GENERAL

The SIG61 is an independent slave in a Powerline communication network controlled by a SIG60 master device. The SIG61 has 4 identification (ID) pins, used to set the device address, 8 input pins and 8 output pins. The master can access any SIG61 device independently by using the proper device address. Data received from a remote SIG60 Master device is reflected to its output pins. The Master device can read the SIG61 input pins remotely. Its small footprint integrates most of the components needed for proper operation allowing small-size control solutions.

The SIG61 is an economical slave device for applications such as controlling motors, reading sensors etc., eliminating the need for dedicated control wires and a host controller for its operation. It helps reducing the harness size and increase reliability. The SIG61 has a sleep mode that enables power saving; special Wakeup messages on the AC or DC line are used to signal the sleeping devices to return to normal operation mode.

The SIG61 is useful for a wide range of Automotive, Avionics and Industrial applications such as sensor reading, actuator activation, doors, seats, mirrors, climate control, lights, Truck-Trailer, etc.

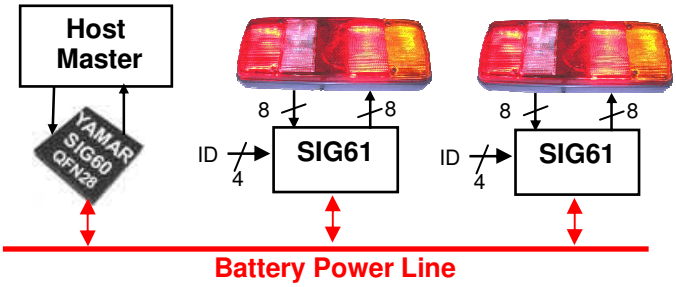

Figure 1.1 - SIG61 Application example

Applications

- **Truck-Trailer sub-bus**
- **Door module**
- **Climate control network**
- **Front and back Lights**
- **Sensors Actuators network**
- **Entertainment control**
- **Renewal Energy / Battery management Microgrid**
- **Security Monitoring**

Features

- **7 selectable Carrier frequencies 1.75MHz - 13MHz**
- **Selectable bit rate between 9.6 Kbps to 115.2 Kbps.**
- **8 output and 8 input pins**
- **Eliminates data wires and transceiver.**
- **Operates over wide range of noisy power supply / battery lines.**
- **Byte oriented communication.**
- **Sleep Mode for low power consumption.**
- **Allows Master - Slave multiplex networks**
- **Several independent networks can operate over the same wire using different carrier frequencies.**
- **Small footprint QFN 64 pin package**

2 OVERVIEW

The SIG61 is an independent slave in a Master-Slaves network operating on a selected narrow band channel. A single SIG60 master controls all the slaves in a network; the slaves may be SIG61 devices as well as SIG60 devices operating as slaves.

Proper Network operation is maintained by employing 5 types of command messages: *Read*, *Read-change*, *Write*, *Sleep* and *Change-Frequency*. The command format is similar to the standard Universal Asynchronous Receiver Transmitter (UART).

The SIG61 has internal narrow band modem, capable of operating in noisy environments. The receiver listens to the Powerline on its preset frequency. It filters out the signal from noise and interference and tries to recover the original command. If the checksum is correct, the SIG61 extracts the ID, Command and the Data.
If the received ID matches its own ID, the SIG61 proceeds to detect the received command. When a Write command is received, the data part of the command is directed to the corresponding 8 output pins. When a Read command is detected, the SIG61 responds by transmitting a dedicated message towards the master containing an image of its 8 input pins.
Multiple networks can operate concurrently on the same wire using different carrier frequencies.

2.1 Channels and Network

The SIG60-SIG61 network supports 16 combinations of frequency pairs. When set to such a pair, it is easy to switch from one frequency to the other when such need arises. Each channel accommodates a single SIG60 master and up to 15 SIG61/SIG60 slave devices. Additional SIG60-SIG61 networks can coexist on the same power line by employing different frequencies for each network, thus allowing different applications.

Channel frequencies: 1.75MHz, 4.5MHz, 5.5MHz, 6.0MHz, 6.5MHz, 10.5MHz and 13.0MHz.
Data transfer rate: 9.6Kbps up to 115.2Kbps.
Cable length: Dependant on external AC loads connected to the AC/DC Powerline.

2.2 The SIG61 Device

Figure 2.1 outlines the building blocks of the SIG61 device.

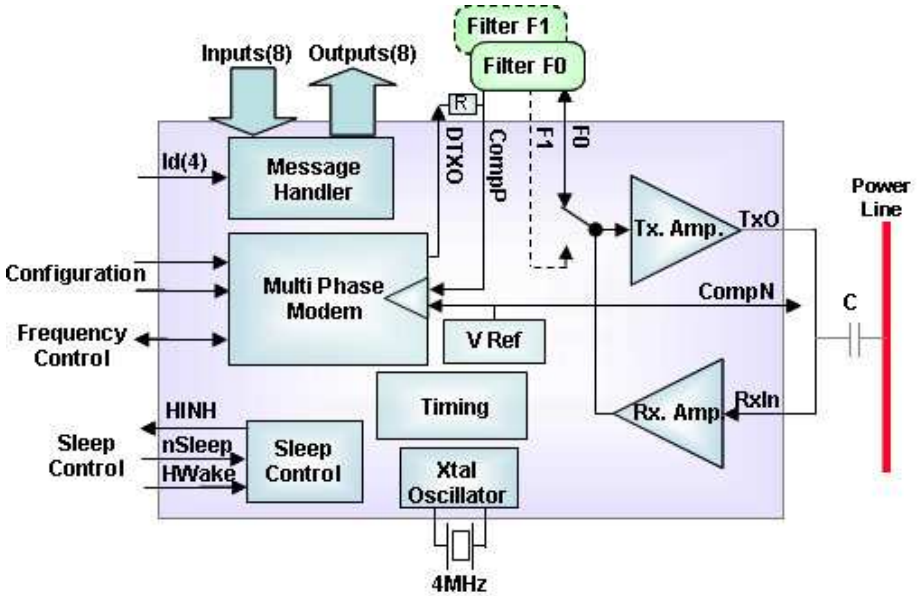

Figure 2.1 - SIG61 Logical Blocks

3 SIG61 SIGNALS

Device signals are described in table 3.1.

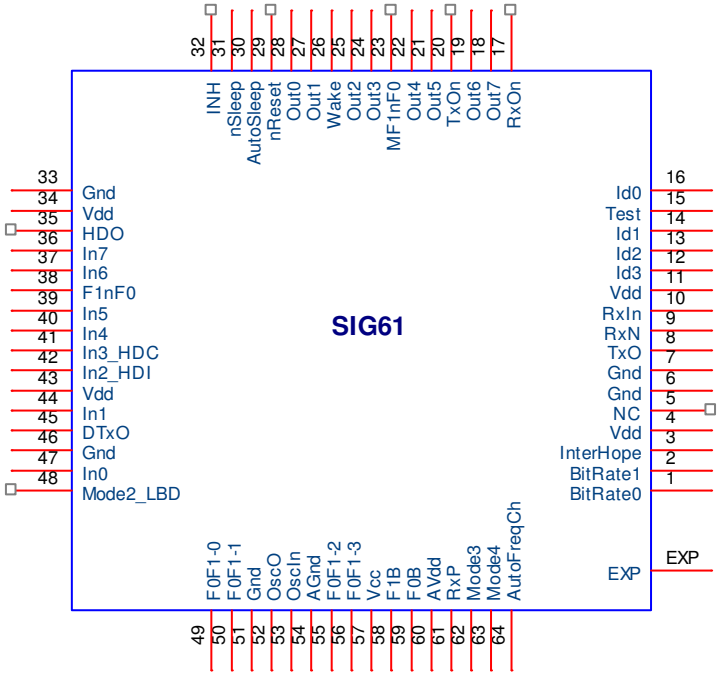

Figure 3.1 - SIG61 Pin-out

Pin name	Pin#	Pin type	Description
			Control Signals
HDO	35	Output 8mA	Digital data output signal. Output the received data from the powerline to the host.
INH	32	Output 8mA	Inhibit output for enabling the host or an external voltage regulator powering the host. This signal is HIGH in the normal and standby modes and LOW in sleep mode.
nSleep	31	Input	Sleep control input. Pulling this signal to LOW puts the SIG61 in sleep mode. Should be pulled to Vdd.
Wake	26	Input	Local wakeup input. Negative or positive edge triggered. This pin can be connected to an external switch in the application. When the pin is triggered the device will wake up and send a wake up message to all the devices on the network. When not in use, this pin should be pulled Up or Down.
nReset	29	Input, PU	Reset Input
InterfHop	3	Input, PD	Allows automatic frequency hoping whenever an interference signal is detected on the power line. When HIGH, detection of interference switches the operating frequency between F0 and F1. If at the new frequency, no reception occurred for 2 sec, the operating frequency is switched back. For designs with a single channel this pin should be tied to ground.
Test	15	Input, PD	Should be connected to Gnd
MF1nF0	23	Output 12mA	Output indicating the operating frequency. F1 when HIGH and F0 when LOW.
			Line Interface signals
OscO	52	Analog Output	Crystal Output
OscIn	53	Analog	Crystal Input

		Input	
RxN	9	Analog Output	The internal comparator negative pin. Its value is internally pulled to Vdd/2. Bypass RxN to Ground with a 1nF capacitor.
RxP	61	Analog Input	Positive pin input signal. Should be tied to RxN with a 1K Ohm resistor.
DTxO	45	Tristate/ Output 2mA	Modulated digital transmit signal output to both ceramic filters.
RxIn	10	Analog Input	Receive input from the power line to the RX operational amplifier. This input is pulled internally to Vdd/2.
TxO	8	Analog Output	Transmit output.
F0B	59	Analog, Bi directional	F0 External filter I/O. Its value is internally pulled to Vdd/2.
F1B	58	Analog, Bi directional	F1 External filter I/O. Its value is internally pulled to Vdd/2.
TxOn	20	Output 12mA	HIGH when the device is transmitting a message.
RxOn	17	Output 12mA	HIGH when the device is in receive mode.
			I/O Signals
In0	47	Input PD	The pin is read by the Master with a Read or Read-Change command.
In1	44	Input PD	The pin is read by the Master with a Read or Read-Change command.
In2_HDI	42	Input	The pin is read by the Master with a Read or Read-Change command. When in SIG60 mode, HDI input.
In3_HDC	41	Input	The pin is read by the Master with a Read or Read-Change command. When in SIG60 mode, HDC input.
In4	40	Input PD	The pin is read by the Master with a Read or Read-Change command.
In5	39	Input PD	The pin is read by the Master with a Read or Read-Change command.
In6	37	Input PD	The pin is read by the Master with a Read or Read-Change command.
In7	36	Input PD	The pin is read by the Master with a Read or Read-Change command.
Out0	28	Output 8mA	Output of data bit 0 when the Write command received from Master.
Out1	27	Output 8mA	Output of data bit 1 when the Write command received from Master.
Out2	25	Output 8mA	Output of data bit 2 when the Write command received from Master.
Out3	24	Output 8mA	Output of data bit 3 when the Write command received from Master.
Out4	22	Output 8mA	Output of data bit 4 when the Write command received from Master.
Out5	21	Output 8mA	Output of data bit 5 when the Write command received from Master.
Out6	19	Output 8mA	Output of data bit 6 when the Write command received from Master.
Out7	18	Output 8mA	Output of data bit 7 when the Write command received from Master.
			Configuration Signals
Id0	16	Input PD	SIG61 bit 0 ID address in the network.
Id1	14	Input PD	SIG61 bit 1 ID address in the network.
Id2	13	Input PD	SIG61 bit 2 ID address in the network.
Id3	12	Input PD	SIG61 bit 3 ID address in the network.
F0F1-0	49	Input PD	Frequency selection pins. See Table 4.2.

F0F1-1	50	Input PD	Frequency selection pins. See Table 4.2.
F0F1-2	55	Input PD	Frequency selection pins. See Table 4.2.
F0F1-3	56	Input PD	Frequency selection pins. See Table 4.2.
BitRate0	1	Input PD	Bit rate selection pins. See Table 4.3.
BitRate1	2	Input PD	Bit rate selection pins. See Table 4.3.
NC	5	---	Not connected.
Mode2	48	Input PD	Should be left unconnected.
Mode3	62	Input PD	Should be connected to Vdd.
Mode4	63	Input PD	Should be connected to Vdd
AutoFreqCh	64	Input PD	Automatic Frequency Change. When HIGH, the device automatically switches frequency after about 4 seconds without bus activity.
AutoSleep	30	Input PD	When this pin is set to HIGH, the device will automatically enter sleep mode after about 8 seconds without bus activity.
F1nF0	38	Input PD	Selects between F0 / F1. HIGH – F1, LOW – F0
			Power signals
Vdd	4,11, 34,43, 57	Power	3.3V power supply.
GND	6,7,33, 46,51	Power	Ground
AGnd	54	Power	Analog Ground
AVdd	60	Power	3.3V Analog Power. Separate from Vdd with a 6.8 to 10 Ohm resistor and bypass to Ground with 1nF and 10nF capacitor.
Exp	Exp		May be connected to GND

PD – Pull down resistor 100K ohm ±%30
PU – Pull up resistor 100K ohm ±%30

Table 3.1 - Device signals

3.1 Power Signals

Vdd and Gnd layout traces should be as wide as possible. It is recommended to connect a 0.1uF capacitor between each Vdd and ground pins, as close as possible to the pins.
Analog Vdd pin, AVdd, should be connected to Vdd. AGnd should be connected to ground. The Analog supply has to be sufficiently powerful (capable of current driving), to avoid any fluctuations of supply voltage level. It is recommended to keep the lines connecting the 3.3V power supply to Vdd pins as short as possible with wide PCB traces.

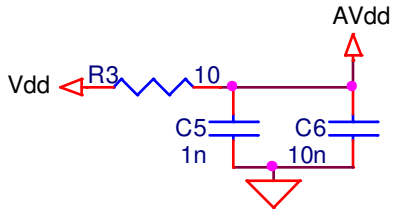

Figure 3.2 - Recommended AVdd circuitry

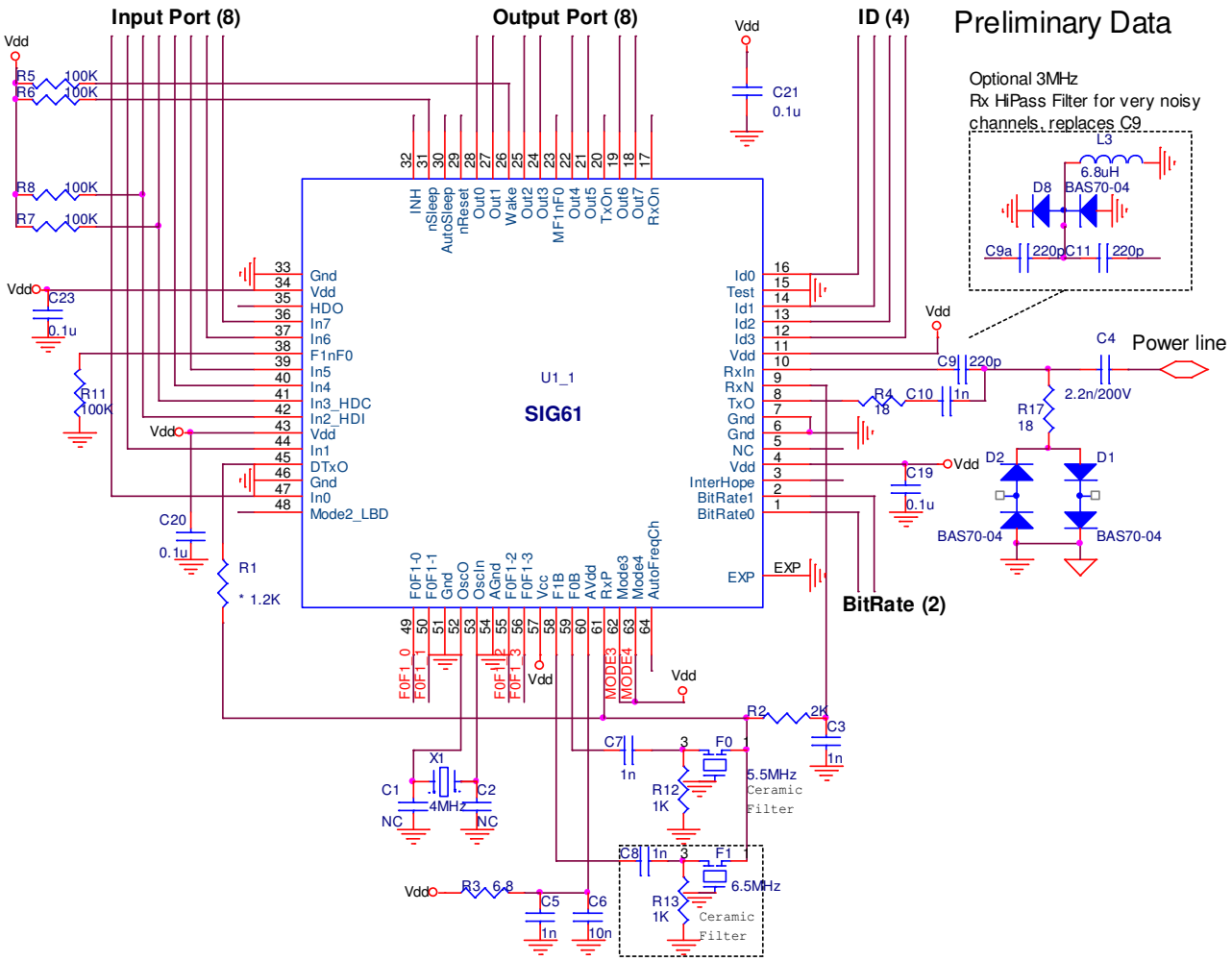

Figure 3.3 – Typical SIG61 dual channel circuit

Notes:

- *All input the signals should be tied either to Gnd, or Vdd, according to the desired mode of operation.*
- *F0 and F1 are ceramic filters*
- *Adjust R1 for maximal output level without distortion on powerline.*
- *C1 and C2 values depend on crystal used. Usually values are between 0pF (NC) to 1.5pF.*
- *Optional 3MHz HPF for very noisy channels, replace C9 with C9a, C11, D8 and L3*
- *F1 is an optional communication channel*

3.2 Ceramic Filter

3.2.1 Ceramic Filter Considerations

The SIG61 is designed to operate with one ceramic filter for transmission and reception. However, if switching between two channels is desired, two ceramic filters are required. The minimum allowable bandwidth of the ceramic filters is +/-60 kHz @ 3dB. Narrow bandwidth limits the maximal bit rate.
The SIG61 selectable frequencies meet market available ceramic filters. It is important to select the widest bandwidth available. 1.75MHz, 10.5MHz and 13MHz may use discrete filters.
Through hole ceramic filters are available from Oscilent.

Nominal freq.	3 db BW	20db BW	Insertion loss	Stop band attenuation	In/Out imped.	Oscilent part #
MHz	KHz min.	KHz max.	dB max.	dB min.	Ohm	
*1.75	+/-70	750	6.0		330-1000	discrete filters
4.50	+/-70	750	6.0	30	1000	773-0045
5.50	+/-80	750	6.0	30	600	773-0055
6.00	+/-80	750	6.0	30	470	773-0060
6.50	+/-80	800	6.0	30	470	773-0065
**10.50	+/-150	1500	4.5		330	discrete filters
**13.00	280 +/-50	1500	4.5		330	discrete filters

**** 1.75MZ can operate only at 9.6Kbps***
***** 10.5MHz and 13.00MHz operates at 115.2Kbps instead of 9.6Kbps.***

SMD ceramic filters are available from Murata.

Nominal freq.	3 db BW	20db BW	Insertion loss	Stop band attenuation	In/Out imped.	Murata part #
MHz	KHz min.	KHz max.	dB max.	dB min.	Ohm	
4.50	+/-60	600	6.0	20	1000	SFSKA4M50CF00-R3
5.50	+/-60	600	6.0	25	600	SFSKA5M50CF00-R3
6.00	+/-60	600	6.0	25	470	SFSKA6M00CF00-R3
6.50	+/-60	600	6.0	25	470	SFSKA6M50CF00-R3

3.3 Oscillator

The SIG61 is designed to operate with a low cost 4MHz crystal connected between OscIn and OscOut pins. Each of these pins should be connected to the ground via a capacitor. All the corresponding PCB traces should be as short as possible.
Recommended crystals are:

1. NDK AT-51 GW.
2. Epson MA-506.

The values of C1, and C2 in Figure 3.3, pertaining to the oscillator circuitry, should be determined according to the crystal manufacturer recommendations. Values between 0pF and 1.5pF may serve as good starting point.

The overall frequency tolerance should not exceed 200ppm.

3.4 Communication performance

The maximum cable length between two devices depends mainly on the AC impedance of loads connected to that line and number of nodes. The Powerline cable length has less effect on communication. The SIG61 requires a minimum received signal of 20mVpp for proper reception.

4 DEVICE OPERATION

4.1 Protocol

The device operation is controlled via 5 types of commands:

***Write* command** - Upon receiving a *Write* command with the SIG61 specific ID, the device shall output the data byte content as indicated by the command to its Output pins.

***Read* command** - Upon receiving a *Read* massage with the SIG61 specific ID, the device shall respond by sending a message containing the status of its Input pins (followed by an appropriate checksum).

***Read-Change* command** - When receiving a *Read-Change* massage with the SIG61 specific ID, the device shall respond to the command by indicating if a pulse upon detecting the first change on its input pins. The response message shall contain the new status of the input pins followed by an appropriate checksum.

***Sleep* command** - Upon receiving a *Sleep* command, the device shall enter a low power-consumption (sleep) mode. A wakeup message generated by the master, or by any of the slaves, wakes up all the devices on the network. This is a global message targeting all the slaves in the network.

***Change-Frequency* command** - Upon receiving *Change-Frequency* command, the device shall switch from its current operational frequency to the other. This command is a global command targeting all the slaves in the network.

4.1.1 Command structure

The structure of the five types of commands is detailed below.

Command type 1: Write command.

The *Write* command consists of 5 bytes: sync break, sync field, Identifier, data and checksum.
Upon receiving a write command, if checksum and protection bits calculations are successful, the data byte content is transferred to the corresponding output pins.

Sync break: Sync break length is at least 13 bit times with compliance to Lin protocol.

Identifier byte: Consist of 2 protection bits (MSB),"01" bits and 4 ID bits - {P1, P0, '0','1', ID [3:0]}

Protection bits calculation:

P0 = (Identifier [0]) XOR (Identifier [1]) XOR (Identifier [2]) XOR (Identifier [4])
P1 = ~ ((Identifier [1]) XOR (Identifier [3]) XOR (Identifier [4]) XOR (Identifier [5]))

Checksum calculation:

The checksum is an inverted **8** bit sum of the Identifier and Data byte including (own) carry:
Checksum = ~ (Identifier Byte + Data Byte + Carry)

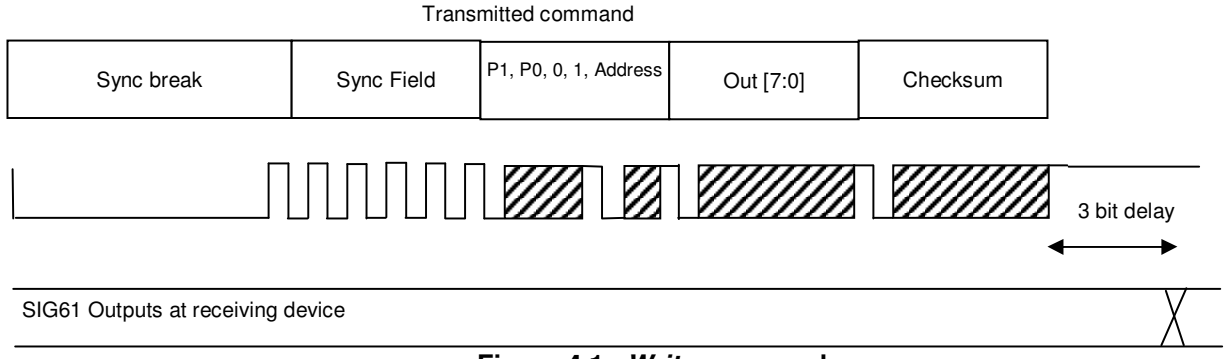

Figure 4.1 - *Write* command

Write Command Example

Sending Write command of Data byte 0xFF to a device with ID '4' will be calculated the following way:

P0 = ('0' XOR '0' XOR '1' XOR '1') = '0'
P1 = ~ ('0' XOR '0' XOR '1' XOR '0') = '0'
Identifier Byte = '00'-'01'-'0100' = 0x14
Checksum = ~ (0x14 + 0xFF + (Carry ='1')) = 0xEB

⇓

Transmitted Command = [Sync Break - 0x55 - 0x14 - 0xFF - 0xEB]

Command type 2: Read command.

The *Read* command, initiated by the Master, requests the status of the SIG61 input pins.

The *Read* command from the master consists of 3 bytes: sync break, sync field and identifier.
Identifier byte**:** consist of 2 protection bits (MSB),"00" bits and 4 ID bits - {P1, P0, '0','0', ID [3:0]}
The two protection bits are calculated as described above.

If header detection is correct (including protection bits), the SIG61 device (whose ID matches the one in the command) shall respond by sending two bytes. A data byte containing the status of its eight input Signal pins followed by a checksum byte. The checksum calculation is carried out as in the description above while part of it, the identifier byte, was transmitted by the Master. Figure 4.2 shows a generic *Read* command.

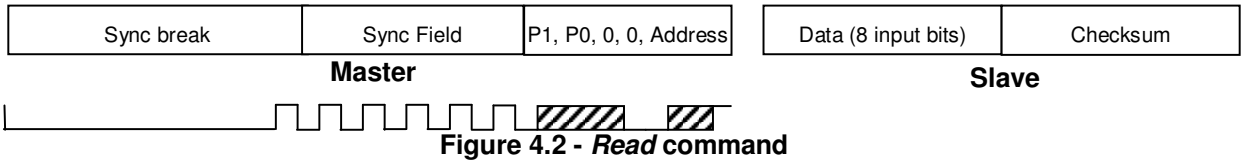

Figure 4.2 - *Read* command

Command type 3: Read-change

The *Read-change* command is similar to the *Read* command. However, it enables to detect any change in the input pins (pulse-like behavior) that may have occurred between two consecutive *Read* or *Read-change* commands. The command from the master instructs the SIG61 to send back information on changes of its input pins since the last *Read* or *Read-change* command. The first change on the pin after the *Read* command sets its bit value.
Figure 4.3 shows the process of determining the sent bit value of an input pin.

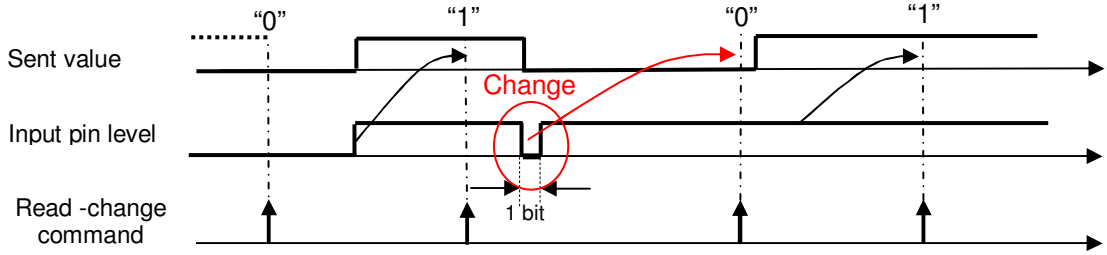

Figure 4.3 - Determining the recent changed value of an input pin

The *Read-change* command from the master has 3 bytes: sync break, sync field and identifier.
Identifier byte: consist of 2 protection bits (MSB),"10" bits and 4 ID bits - {P1, P0, '1','0', ID [3:0]}
The response for this command is a data byte containing the SIG61`s input pins recent changed value, followed by the checksum byte. See checksum and protection bits calculation description above. Figure 4.4 shows a *Read-changes* command.

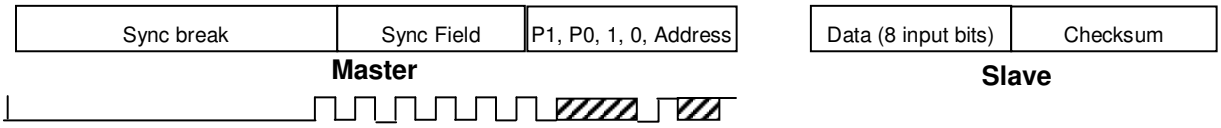

Figure 4.4 - *Read-change* command

Command type 4: Sleep command.

This type of command consist of 5 bytes: sync break, sync field, “3C” Hex, “00” Hex and checksum.
The sleep command identifier is “3C”Hex as in LIN2.0 specifications and the following data byte “00”Hex.
Upon reception of sync break, sync field, “3C”Hex and “00”Hex bytes, a device enters sleep mode immediately and as a result it’s the following command bytes are ignored.

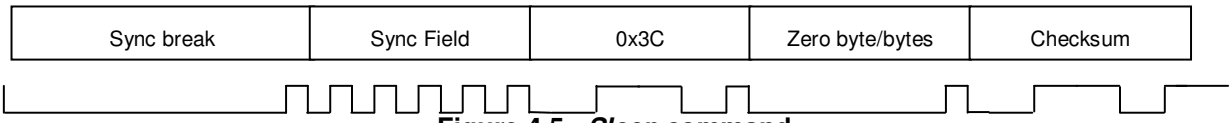

Figure 4.5 - *Sleep* command

Command type 5: Change Frequency command.

This type of command consists of 5 bytes - sync break, sync field, “FE” Hex, “00” Hex and checksum.
The *change frequency* command identifier is “FE” Hex and the following data byte is “00”Hex.
Upon reception of sync break, sync field, “FE” Hex and “00” Hex bytes the frequency changes from F1 to F0, or vise versa. Checksum calculation follows the description above.

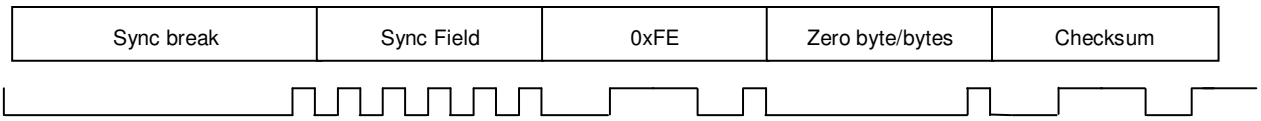

Figure 4.6 - *Frequency Change* command

4.2 Power Management

The SIG61 device features Sleep mode for power saving. Entering the Sleep mode, as well as waking up, can be initiated locally, by means of dedicated input pins, or remotely through activity (proper messages) over the bus.

4.2.1 Entering Sleep mode

The SIG61 can enter sleep mode by any of the following ways:

1. The device nSleep pin is lowered.
2. *Sleep command* from a remote master is received.
3. The AutoSleep pin is set HIGH and no reception occurred for about 8 seconds.

4.2.2 Device Outputs during Sleep

During Sleep mode, the SIG61 8 output pins remain unchanged if the device has entered this mode due to a Sleep command from the Master or by lowering the Pin nSleep.
However if the device entered the Sleep mode due to the AutoSleep function, SIG61 will lower all the outputs to "0".

4.2.3 Remote wake up process

The SIG61 can be awakened by a remote SIG60 master, or SIG61 slave, device transmitting a wakeup message over the bus. During Sleep Mode, the SIG61 wakes up periodically, every 32mSec, to sense for bus activity. If a *wakeup* message is detected, the SIG61 device raises pin INH and lowers pin HDO. If nSleep pin is low upon remote waking up, the local host (a device controlling the SIG61) which initially pulled nSleep pin down, must raise the nSleep back high. Figure 4.7 provides the signal description.

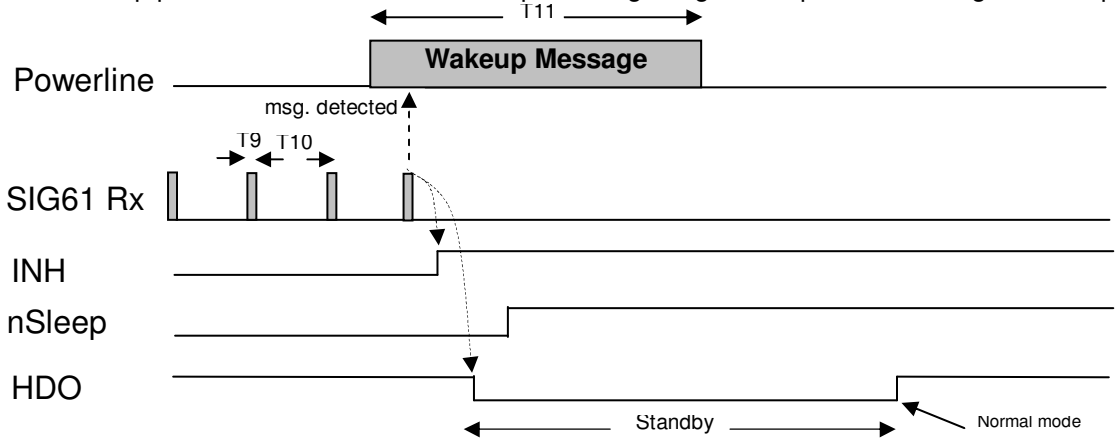

Figure 4.7 - Wakeup from bus message

4.2.4 Wakeup from *Wake* pin

A transition seen on the *Wake* pin (caused by an external source) is used to wake up the device. The device then enters Standby mode, it rises pin INH, and transmits a wakeup message to the bus. While transmitting the wakeup message, the device lowers pin HDO. After the transmission is completed the device raises pin HDO. This is depicted in Figure 4.8. After the transmission is completed the device enters Normal mode. If nSleep pin is low upon waking up, the local host which initially pulled nSleep pin down, must raise the nSleep back to high.

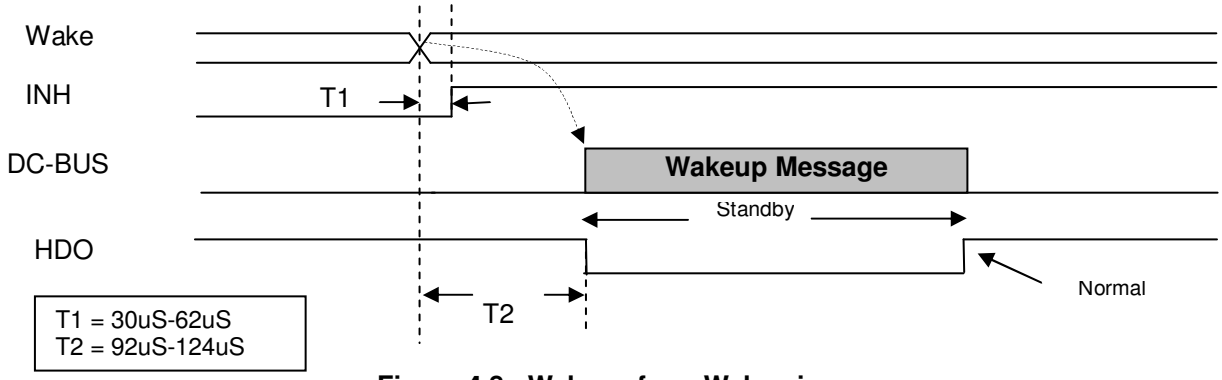

Figure 4.8 - Wakeup from Wake pin

4.3 Timing Characteristic

Symbol	Figure	Characteristics	Min	Max
T_1	4.3,4.4	Drop of HDC to drop of HDI	200nS	
T_2	4.3	Raise of HDC to drop of HDI	200nS	
T_3	4.3	Command stop bit to raise of HDC	Half bit rate	
T_4		Drop of nSleep to drop of INH	30uS	62uS
T_5	4.5	Raise of nSleep to raise of INH	30uS	62uS
T_6	4.4	Transact on Wake to raise of INH	30uS	62uS

T_7	4.3	Raise of nSleep to drop of HDO	92uS	124uS
T_8	4.4	Transact on Wake to drop of HDO	92uS	124uS
		Power Up or Reset to Normal mode		6mS
T9	4.5	Receive duration during sleep mode	1.5mS	
T10	4.5	Receive period during sleep mode	32mS	+/-20%
T11	4.5	Wakeup message		150mS

4.4 SIG61 Configuration

The Pins labeled “Mode 4” and “Mode 3” should be tied up to Vdd.
The SIG61 operates at default with the following parameters:
Bit rate: 19.2Kbps, F0=5.5MHz, F1=6.5MHz
The following configuration bits set the operating frequencies according to table 4.2.

Table 4.2 – F0, F1 select

F0F1 (3:0) pins	F0	F1
1111	1.75Mhz	4.5Mhz
1110	1.75Mhz	5.5Mhz
1101	1.75Mhz	6Mhz
1100	1.75Mhz	6.5Mhz
1011	4.5Mhz	5.5Mhz
1010	4.5Mhz	6.0Mhz
1001	4.5Mhz	6.5Mhz
1000	4.5Mhz	10.5Mhz
0111	10.5Mhz	13.0Mhz
0110	5.5Mhz	10.5Mhz
0101	5.5Mhz	13.0Mhz
0100	6.0Mhz	10.5Mhz
0011	6.0Mhz	13.0Mhz
0010	6.5Mhz	10.5Mhz
0001	6.5Mhz	13.0Mhz
0000	5.5Mhz	6.5Mhz

Table 4.3 – bit rates selection

BitRate (1,0) Pins / Frequency	11	10	01	00
1.75 MHz	-	-	9.6K	19.2K
4.50 MHz	38.4K	57.6K	9.6K	19.2K
5.50 MHz	38.4K	57.6K	9.6K	19.2K
6.00 MHz	38.4K	57.6K	9.6K	19.2K
6.50 MHz	38.4K	57.6K	9.6K	19.2K
10.50 MHz	38.4K	57.6K	115.2	19.2K
13.00 MHz	38.4K	57.6K	115.2	19.2K

Signal	High (“1”)	Low (“0”)
AutoSleep	Auto Sleep On	Auto Sleep Off
ID[3:0]	Defines device ID	
F1nF0	Select F1	Select F0
InterHop	InterHop On	InterHop Off

5 ELECTRICAL PARAMETERS

5.1 Absolute Maximum Rating

Ambient Temperature under bias	-40°C to 125°C
Storage Temperature	-55°C to 150°C
Input Voltage	-0.6V to Vdd+0.3V
Vdd Supply voltage	-0.3V to 4V

5.2 Electrical Operating Conditions

Symbol	Characteristics	Min	Typ	Max	Units	Conditions
Vdd	Supply Voltage	3.0	3.3	3.6	V	
Idd	Supply Current		40		mA	5.5MHz
Idd	Supply Current during Tx		50		mA	5.5MHz
Ipd	Supply Current in Sleep mode		80		uA	

5.3 DC Electrical Characteristics

Symbol	Characteristics	Vdd	Typ	Units	Conditions
V_{IH}	Minimum high level input voltage	3.0	2.1	V	
V_{IL}	Maximum low level input voltage	3.0	0.9	V	
V_{OH}	Minimum high level output voltage	3.0	2.4	V	
V_{OL}	Maximum low level output voltage	3.0	0.4	V	
Iout	Maximum output current, other pins				See pins table
I_{IN}	Maximum input current	3.3	± 10	uA	

5.4 Operating Temperature

Commercial: 0°C to 70°C

Industrial: -40°C to 85°C

5.5 Mechanical Information

Package type - QFN 64 pin

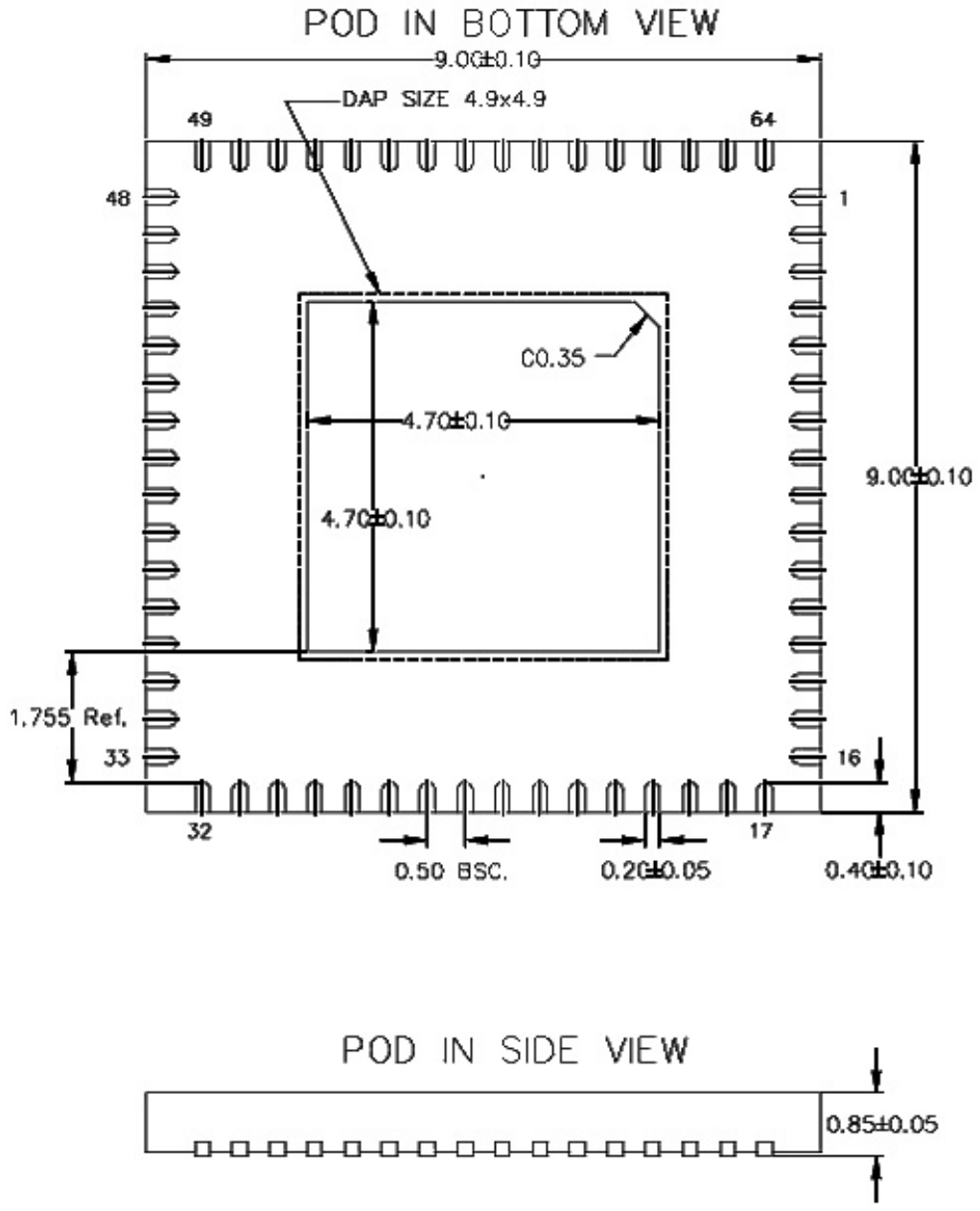

Figure 5.1 – QFN64 mechanical dimensions

Revision changes:

Revision	Date	Comments
0.2	2.3.2008	Detailed description
0.4	22.5.2009	Updated schematic
0.5	25.5.2009	Updated pin information
0.61	22.7.2009	Updated mechanical drawing Added “Outputs during Sleep”
0.7	13.9.2009	Added checksum and parity calculations Renumbering figures
0.8	20.11.2009	Update the Write and Read commands. Update tables 4.2- 4.3 Added 3.4.8 and 3.4.9
0.9	20.12.2009	Updated schematics, protection network, Electrical parameters, pin description table
0.92	28.12.2009	Updated drawings, notations, descriptions.
0.93	7.1.2010	Updated Read-change command explanation
0.932	6.5.2010	Updated drawings, descriptions.
0.94	29.8.2010	Updated ceramic filters, schematics,
0.95	24.10.2010	Updated figures 4.1-4.6
0.96	27.2.2011	Updated figure 3.3 schematic for high noise channels operation
0.961	4.8.2011	Updated figure 3.3 C9 and C11 to 220p
0.97	1.11.2011	Update schema - Connect pins Mode3 and Mode4 to Vdd. Update Table 3.1 - Replace between the GND pins and the Vdd pins, Fix a typo at mode4 pin number.
0.98	30.4.2012	Update figures 4.1 ,descriptions, examples