



BUK9880-55

N-channel TrenchMOS logic level FET

Rev. 03 — 20 April 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

1.3 Applications

- Automotive and general purpose power switching

1.4 Quick reference data

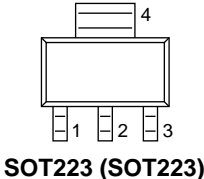
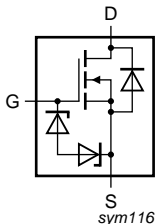
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	55	V
I_D	drain current	$T_{sp} = 25\text{ °C}$	-	-	7.5	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	-	-	1.8	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}$	-	65	80	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}; V_{sup} \leq 25\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	-	30	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT223 (SOT223)</p>	 <p>Sym116</p>
2	D	drain		
3	S	source		
4	D	drain		

3. Ordering information

Table 3. Ordering information

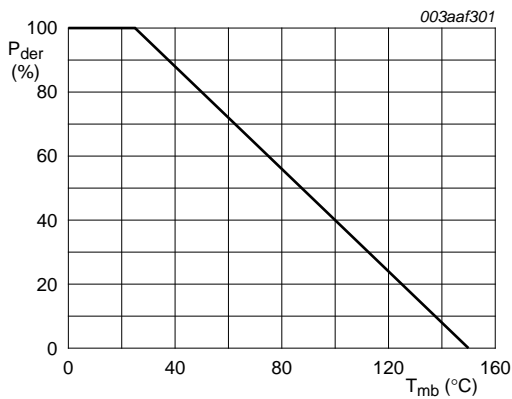
Type number	Package		Version
	Name	Description	
BUK9880-55	SOT223	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

Table 4. Limiting values

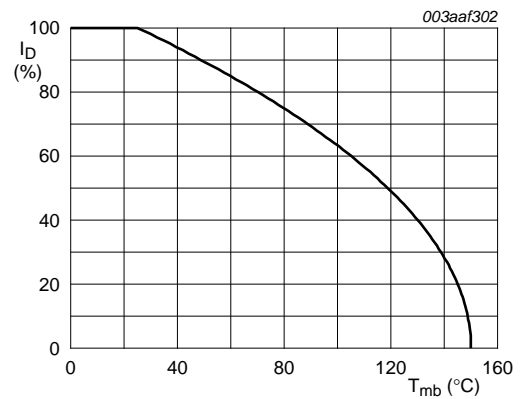
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	$T_{amb} = 25\text{ °C}$	-	3.5	A
		$T_{sp} = 25\text{ °C}$	-	7.5	A
		$T_{amb} = 100\text{ °C}$	-	2.2	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed	-	40	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	-	1.8	W
		$T_{sp} = 25\text{ °C}$	-	8.3	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
V_{esd}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	-	2	kV
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	7.5	A
I_{SM}	peak source current	pulsed; $T_{sp} = 25\text{ °C}$	-	40	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	30	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

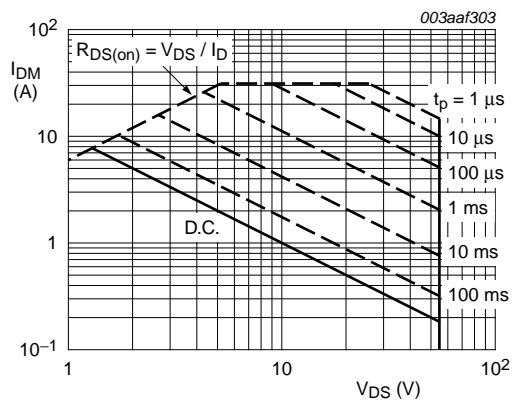
Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

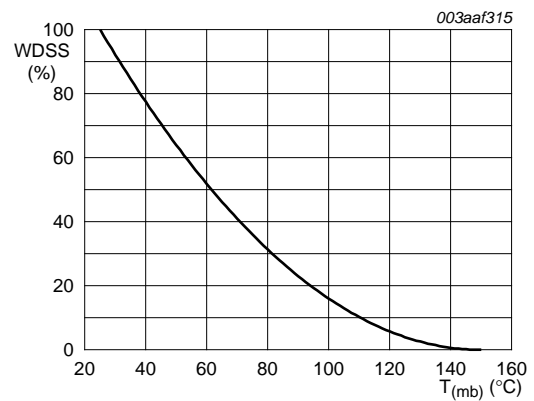
$V_{GS} \geq 5\text{ V}$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25\text{ }^{\circ}\text{C}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



$I_D = 2.5\text{ A}$

Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on any printed-circuit board	-	12	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	-	-	70	K/W

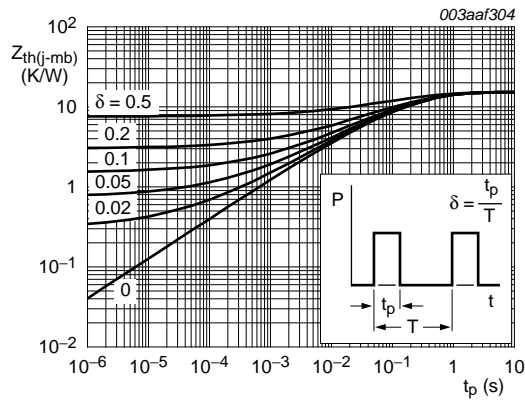


Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.6	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	148	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	65	80	m Ω
$V_{(BR)GSS}$	gate-source breakdown voltage	$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = 1 \text{ mA}$	10	-	-	V
		$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = -1 \text{ mA}$	10	-	-	V
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	500	650	pF
C_{oss}	output capacitance		-	110	135	pF
C_{rss}	reverse transfer capacitance		-	60	85	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 4.29 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 7 \text{ A}$	-	10	15	ns
t_r	rise time		-	30	50	ns
$t_{d(off)}$	turn-off delay time		-	30	45	ns
t_f	fall time		-	30	40	ns
g_{fs}	transfer conductance	$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	4	8	-	S
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j \geq -55 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$	-	0.85	1.1	V
t_{rr}	reverse recovery time	$I_S = 5 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j \leq 175 \text{ }^\circ\text{C}$	-	38	-	ns
Q_r	recovered charge		-	0.2	-	μC

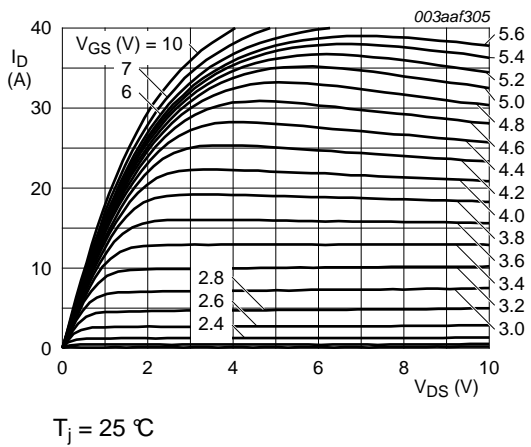


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

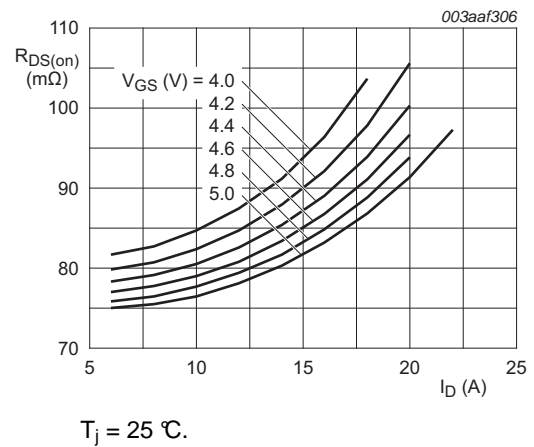


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

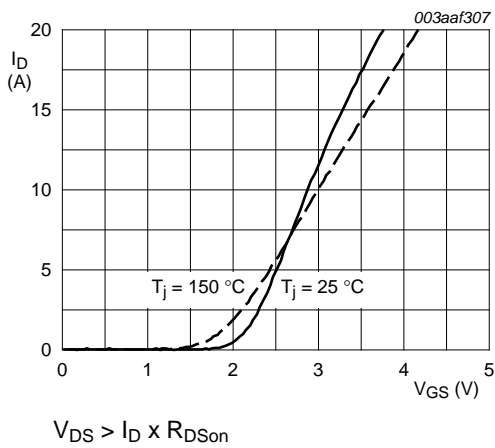


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

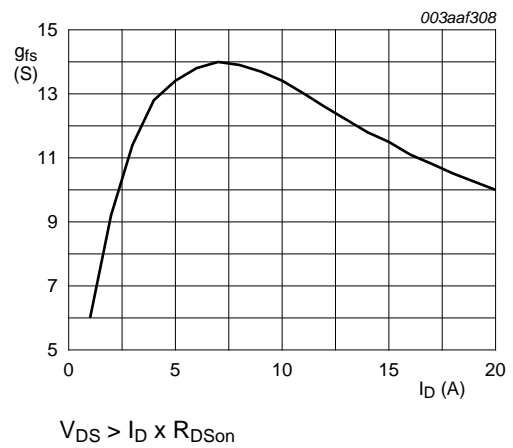
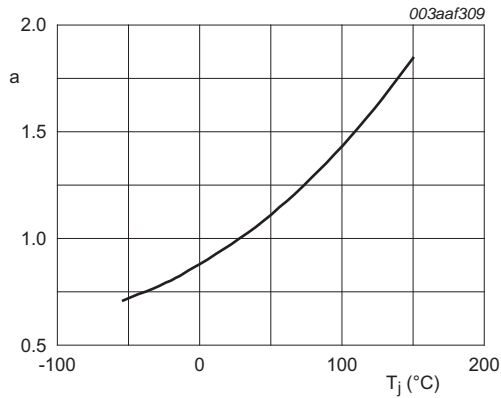


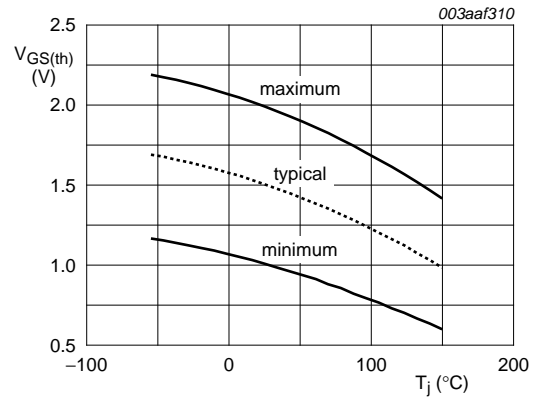
Fig 9. Forward transconductance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

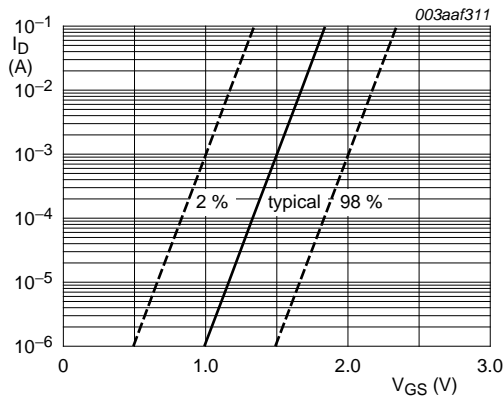
$I_D = 5 \text{ A}; V_{GS} = 5 \text{ V}$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



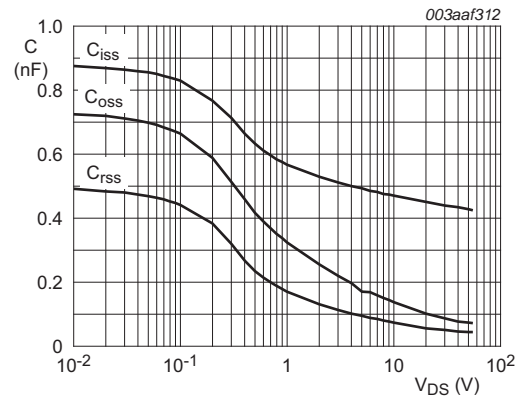
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



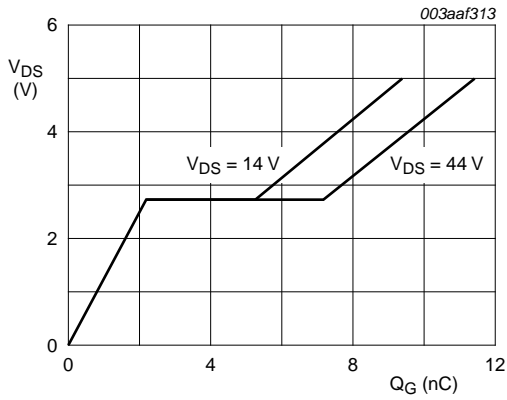
$T_j = 25 \text{ }^{\circ}\text{C}; V_{DS} = V_{GS}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



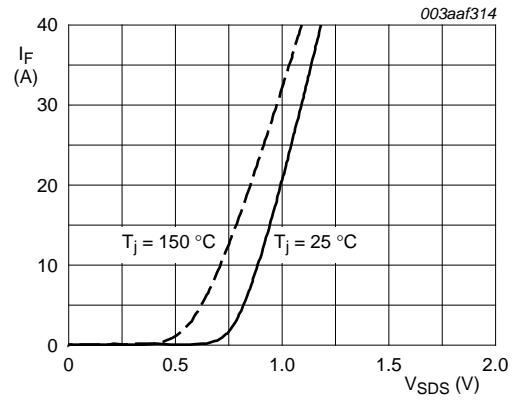
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; I_D = 7\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

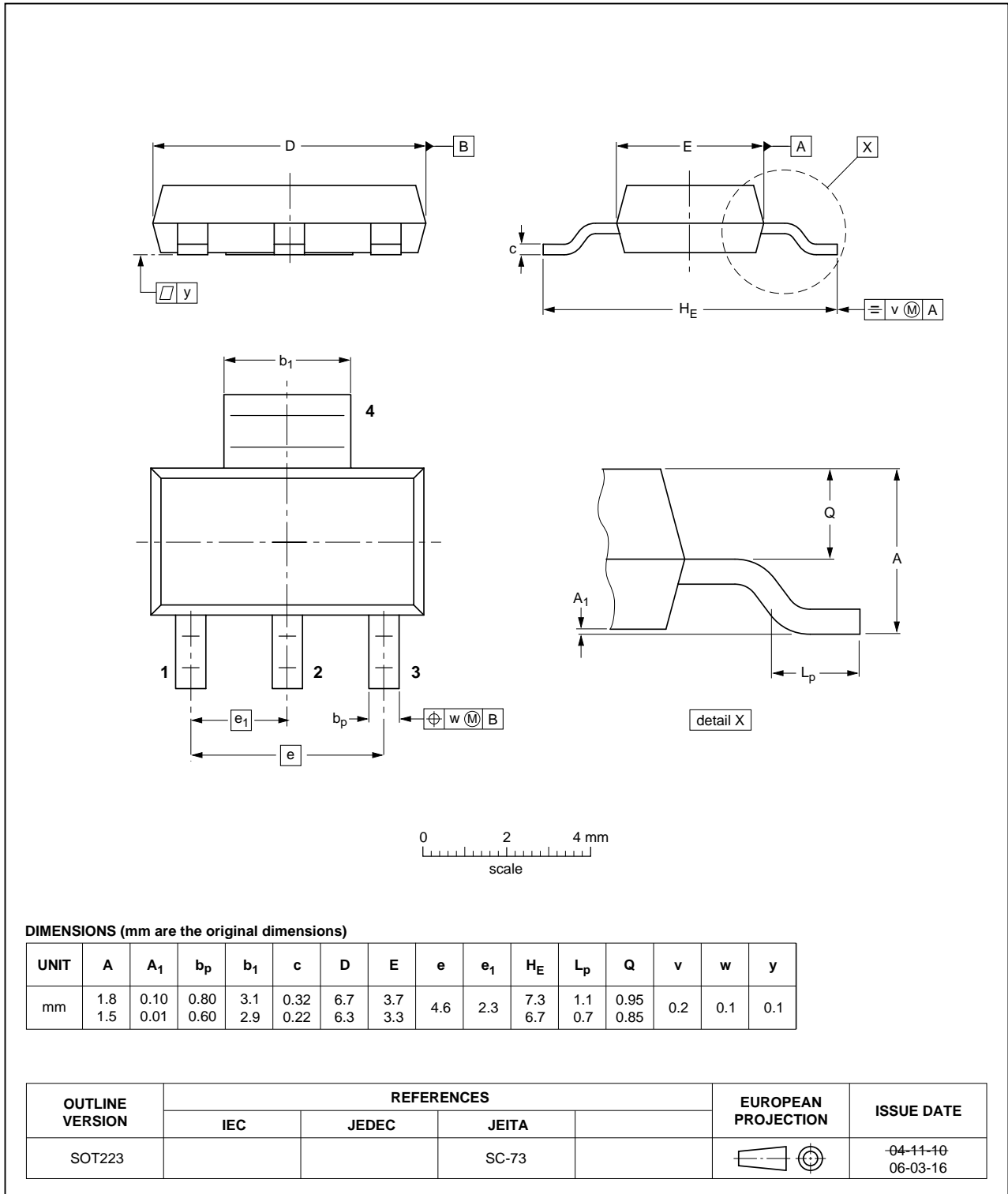


Fig 16. Package outline SOT223 (SOT223)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9880-55 v.3	20110420	Product data sheet	-	BUK9880-55 v.2
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Various changes to content.			
BUK9880-55 v.2	19980401	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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