



CCB LV23100V

Bi-CMOS IC

1-chip Tuner IC incorporating PLL for Portable Audio System

ON Semiconductor®

<http://onsemi.com>

Overview

The LV23100V is a one-chip tuner IC incorporating PLL for portable audio system.

Functions

- AM tuner
- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$	V_{CC}	4.0	V
	$V_{DD\text{ max}}$	V_{DD}	4.0	V
Maximum input voltage	$V_{IN1\text{ max}}$	CE, CI, CL	6.0	V
	$V_{IN2\text{ max}}$	XIN	$V_{DD}+0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$	180	mW
Maximum output voltage	$V_{O1\text{ max}}$	DO	6.0	V
	$V_{O2\text{ max}}$	XOUT, PD	$V_{DD}+0.3$	V
	$V_{O3\text{ max}}$	BO1, BO2, AOUT	12.0	V
Operating temperature	T_{opr}		-20 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Note : This product should be handled with care because the resistance against electrostatic discharge damage is low.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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LV23100V

Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		3.0	V
	V _{DD}		3.0	V
Operating supply voltage range	V _{CC} op		2.2 to 3.6	V
	V _{DD} op		2.2 to 3.6	V

PLL block Allowable Operating Range at Ta = -20°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V _{DD}		2.2		3.6	V
Input high level voltage	V _{IH}	CE, CL, DI	0.7V _{DD}		6.0	V
Input low level voltage	V _{IL}	CE, CL, DI	0		0.3V _{DD}	-
Output voltage	V _{O1}	DO	0		6.0	V
	V _{O2}	BO1, BO2, AOUT	0		10	V
Operating frequency	f _{IN1}	XIN ; V _{IN1}		75		kHz
	f _{IN2}	FMIN ; V _{IN2}	10		160	MHz
	f _{IN3}	AMIN (SNS = 1) ; V _{IN3}	2		40	MHz
	f _{IN4}	AMIN (SNS = 0) ; V _{IN4}	0.5		10	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

Operating Characteristics at Ta = 25°C, V_{CC} = V_{DD} = 3.0V, See the specified circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	I _{CCFM}	No input in FM mode	9	12.5	16	mA
AM tuner block	I _{CCAM}	No input in AM mode	4	6	8	mA
PLL block	I _{DDFM}	fr = 98MHz, No input at tuner	1	2	4	mA
[FM-FE characteristics] : fc = 98MHz, fm = 1kHz, dev = 22.5kHz						
3dB sensitivity	-3dBLS	V _{IN} = 60dBμV EMF reference, -3dB input		10		dBμV EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		13		dBμV EMF
[FM-IF characteristics] : fc = 10.7MHz, fm = 1kHz, dev = 75kHz (L+R = 90%, Pilot = 10%)						
Demodulation output	V _O	V _{IN} = 100dBμV	140	180	210	mVrms
3dB sensitivity	LS	V _{IN} = 100dBμV reference, -3dB input	26	31	36	dBμV
Signal-to-noise ratio	S/N	V _{IN} = 100dBμV	63	70		dB
IF count sensitivity	IF-C1	0%mod, SDC = 1	42	50	56	dBμV
Total harmonic distortion	THD	V _{IN} = 100dBμV, MAIN-MOD		0.5	1.5	%
Separation	SEP	V _{IN} = 100dBμV, L output/R output	25	40		dB
Mute attenuation	MUTE	V _{IN} = 100dBμV, L output	55	60		dB
[AM characteristics] : fc = 1000kHz, fm = 1kHz, 30%mod						
Demodulation output	V _O	V _{IN} = 80dBμV	30	50	70	mVrms
Signal-to-noise ratio 1	S/N1	V _{IN} = 23dBμV	15	20		dB
Signal-to-noise ratio 2	S/N2	V _{IN} = 80dBμV	47	53		dB
Total harmonic distortion	THD	V _{IN} = 80dBμV		0.5	1.5	%
IF count sensitivity	IF-C	0%mod	20	27	34	dBμV

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LV23100V

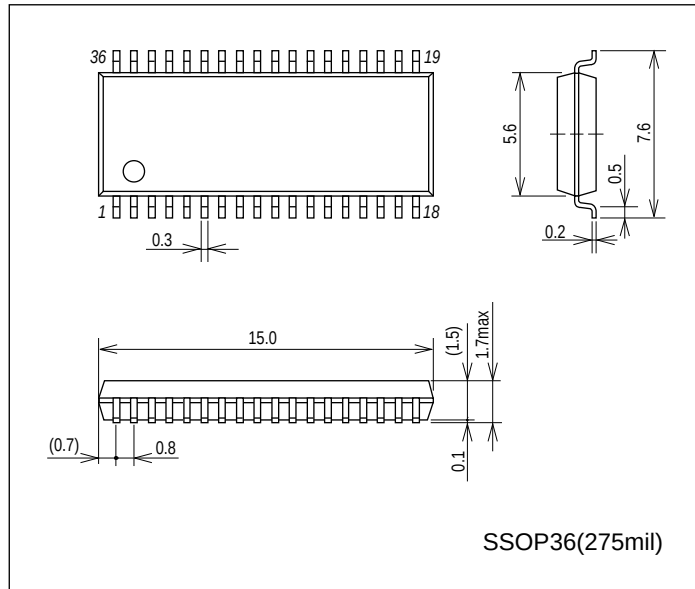
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	VHIS	CE, CL, DI		0.1VDD		V
Output high level voltage	VOH	PD ; IO = -1mA	VDD-1.0			V
Output low level voltage	VOL1	PD ; IO = 1mA			1.0	V
	VOL2	BO1, BO2 ; IO = 1mA			0.25	V
		BO1, BO2 ; IO = 5mA			1.25	V
	VOL3	DO ; IO = 1mA			0.25	V
	VOL4	AOUT ; IO = 1mA, AIN = 2.0V			0.5	V
Input high level current	IIH1	CE, CL, DI ; VI = 6.0V			5.0	μA
	IIH2	XIN ; VI = VDD	0.16		0.9	μA
	IIH3	AIN ; VI = 6.0V			200	nA
Input low level current	IIL1	CE, CL, DI ; VI = 0V			5.0	μA
	IIL2	XIN ; VI = 0V	0.16		0.9	μA
	IIL3	AIN ; VI = 0V			200	nA
Output off-leak current	IOFF1	BO1, AOUT, BO2 ; VO = 10V			5.0	μA
	IOFF2	DO ; VO = 6.0V			5.0	μA
"H" level 3-state off-leak current	IOFFH	PD ; VO = 6.0V		0.01	200	nA
"L" level 3-state off-leak current	IOFFL	PD ; VO = 0V		0.01	200	NA

Package Dimensions

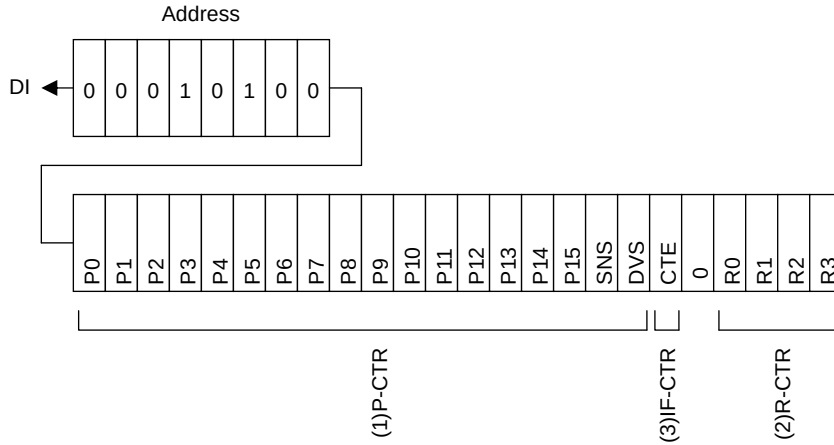
unit : mm (typ)

3247A

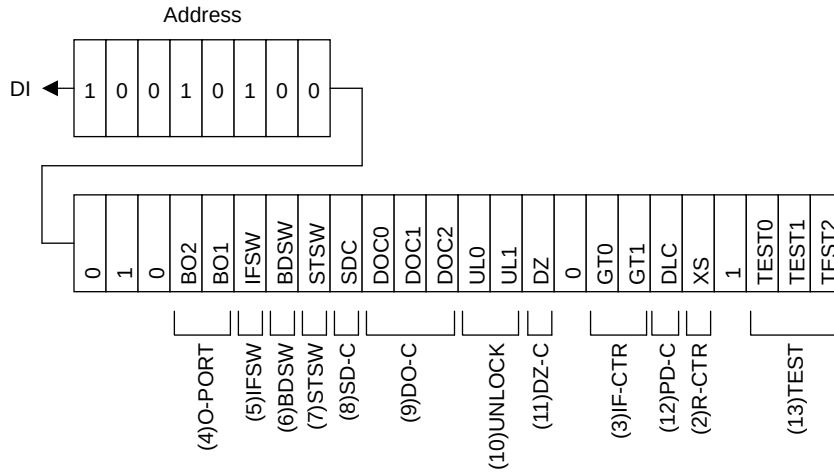


Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



Description of DI control Data

No.	Control block data	Description	Related data																																				
(1)	DO pin Control data DOC0 DOC1 DOC2	- Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : don't care) <table><tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number (N)</th><th>actual dividing number</th></tr><tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr><tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr><tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr></table> * P0 to P3 invalid when LSB : P4 - To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : don't care) <table><tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr><tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr><tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr><tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr></table>	DVS	SNS	LSB	set dividing number (N)	actual dividing number	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	0	1	AMIN	2 to 40MHz	0	0	AMIN	0.5 to 10MHz	
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No.	Control block data	Description	Related data																																																																																					
(2)	Reference divider data R0 to R3 XS	- Reference frequency (fref) selection data <table><tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr></table> * PLL INHIBIT - The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance. - XS must be zero.	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC STOP	1	1	1	1	PLL INHIBIT	
R3	R2	R1	R0	Reference frequency																																																																																				
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1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data CTE GT0, GT1	- IF counter counting start data CTE = 1 : Counting start = 0 : Counting start - Determines the counting time of universal counter <table><tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr><tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr><tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr><tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr><tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr></table>	GT1	GT0	Counting time	Wait time	0	0	4ms	3 to 4ms	0	1	8ms	3 to 4ms	1	0	16ms	3 to 4ms	1	1	32ms	3 to 4ms																																																																		
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1	1	32ms	3 to 4ms																																																																																					
(4)	Output port data $\overline{\text{BO1}}$, $\overline{\text{BO2}}$	Data to determine output of output ports $\overline{\text{BO1}}$ and $\overline{\text{BO2}}$ "Data" = 0 : OPEN 1 : Low																																																																																						
(5)	MUTE control data IFSW	Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0 : at receiving 1 : MUTE																																																																																						
(6)	FM/AM BAND selection control data BDSW	Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0 : AM 1 : FM																																																																																						
(7)	Forced monaural control data STSW	Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0 : MONO 1 : STEREO																																																																																						
(8)	SD sensitivity control data SDC	Data to determine the output of output port SDC, controlling the FM-SD sensitivity (at IF input). <table><tr><th>SDC</th><th>FM-SD sensitivity</th></tr><tr><td>0</td><td>38dBμV</td></tr><tr><td>1</td><td>48dBμV</td></tr></table>	SDC	FM-SD sensitivity	0	38dB μ V	1	48dB μ V																																																																																
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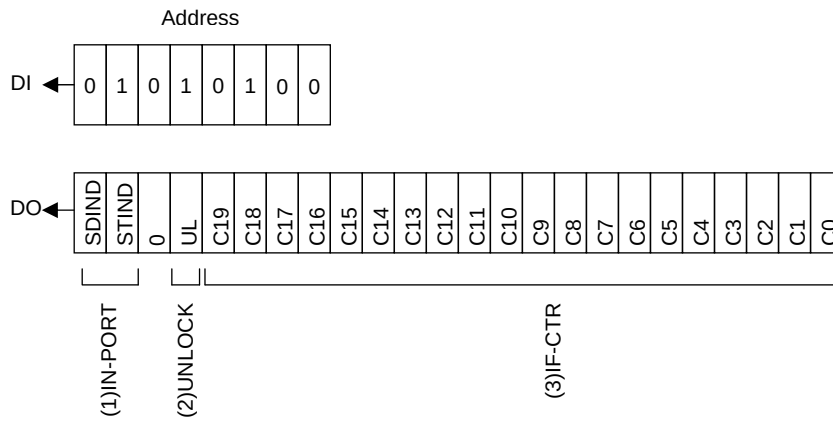
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No.	Control block data	Description	Related data																																				
(9)	DO pin control data DOC0 DOC1 DOC2	• Data to determine the output of the DO pin. <table><tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>end-UC (See the item with asterisk below)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Low when stereo</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Low when SDON</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr></table> • The open condition is selected at power ON/reset. * IF counter counting end check DO pin ① Counting start ② Counting end ③ CE : HI ① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically. ② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made. ③ DO pin opens when serial data is entered/output (CE pin : Hi) Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).	DOC2	DOC1	DOC0	DO pin condition	0	0	0	Open	0	0	1	Low when unlock is detected.	0	1	0	end-UC (See the item with asterisk below)	0	1	1	Open	1	0	0	Open	1	0	1	Low when stereo	1	1	0	Low when SDON	1	1	1	Open	UL0, UL1 CTE
DOC2	DOC1	DOC0	DO pin condition																																				
0	0	0	Open																																				
0	0	1	Low when unlock is detected.																																				
0	1	0	end-UC (See the item with asterisk below)																																				
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1	0	0	Open																																				
1	0	1	Low when stereo																																				
1	1	0	Low when SDON																																				
1	1	1	Open																																				
(10)	Unlock detection data UL0, UL1	• Phase error (ϕE) detection width selection data to judge if PLL is locked. • Phase error exceeding the detection width is judged that PLL is locked (* : don't care) <table><tr><th>UL1</th><th>UL0</th><th>ϕE Detection width</th><th>Detection output</th></tr><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr><tr><td>1</td><td>*</td><td>$\pm 6.67\mu s$</td><td>ϕE extended by 1 to 2 ms</td></tr></table> * DO pin is LOW. Serial data output : UL = 0.	UL1	UL0	ϕE Detection width	Detection output	0	0	Stop	Open	0	1	0	Direct output of ϕE	1	*	$\pm 6.67\mu s$	ϕE extended by 1 to 2 ms	DOC0 DOC1 DOC2																				
UL1	UL0	ϕE Detection width	Detection output																																				
0	0	Stop	Open																																				
0	1	0	Direct output of ϕE																																				
1	*	$\pm 6.67\mu s$	ϕE extended by 1 to 2 ms																																				
(11)	Phase comparator control data DZ	• Data to control the dead zone of phase comparator <table><tr><th>DZ</th><th>Charge pump output</th></tr><tr><td>0</td><td>DZA</td></tr><tr><td>1</td><td>DZB</td></tr></table> Dead zone width : DZA<DZB	DZ	Charge pump output	0	DZA	1	DZB																															
DZ	Charge pump output																																						
0	DZA																																						
1	DZB																																						
(12)	Charge pump control data DLC	• Data to enforce control of charge pump output <table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></table> In case of dead lock because of VCO oscillation stop when the VCO control voltage (V_{tune}) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V_{CC}. (Dead lock clear circuit)	DLC	Charge pump output	0	Normal	1	Forced to LOW																															
DLC	Charge pump output																																						
0	Normal																																						
1	Forced to LOW																																						
(13)	LSI test data TEST0 to 2	• LSI test data TEST0 TEST1 TEST2 All to be set to "0" All set to zero at power ON/reset																																					

DO control data (serial data output) composition

(1) OUT mode



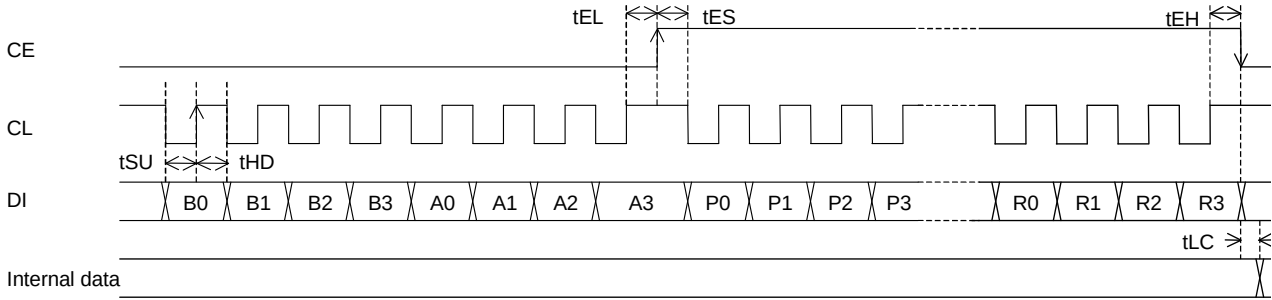
Description of DO output data

No.	Control block data	Description	Related data
(1)	SD and Stereo indicators control data STIND, SDIND	Data latching SD and stereo indicator conditions. Latching made in the data output (OUT) mode. SDIND←SD indicator condition 0 : SD ON, 1 : SD OFF STIND←Stereo indicator condition 0 : ST ON, 1 : ST OFF	
(2)	PLL unlock data UL	Data latching the content of unlock detection circuit UL←0 : At unlock 1 : At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	Data latching the content of IF counter (20-bit binary counter) C19←MSB of binary counter C0 ←MSB of binary counter	CTE GT0 GT1

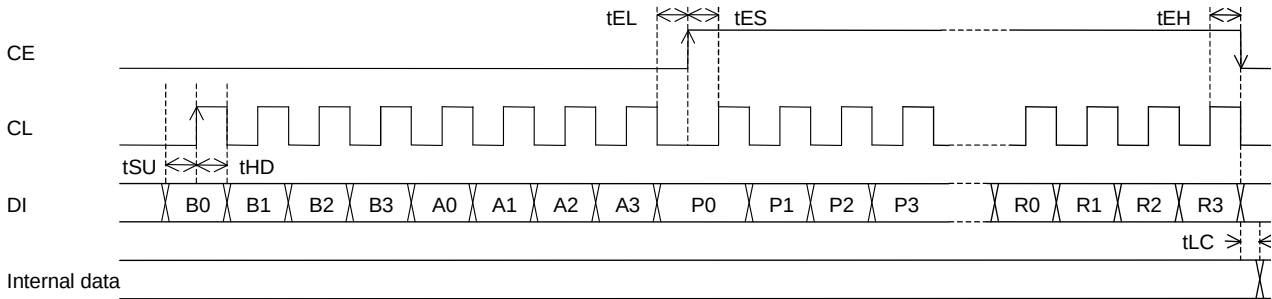
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Serial data input (IN1/IN2) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75\mu s$ $t_{LC} < 0.75\mu s$

CL : Normally Hi

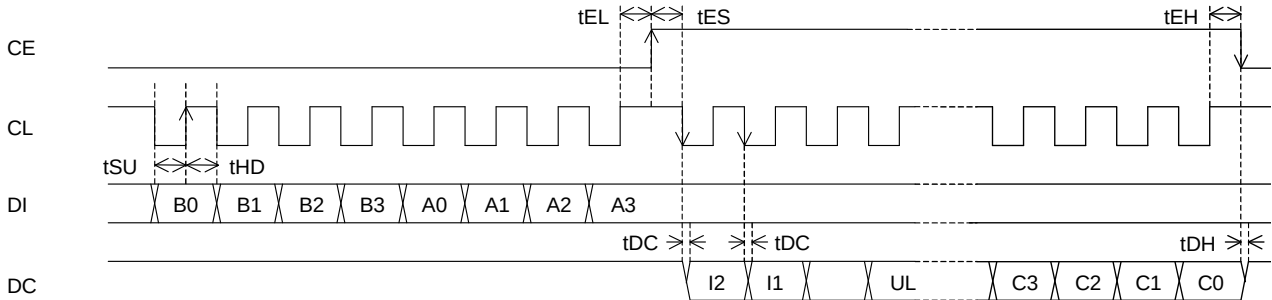


CL : Normally Low

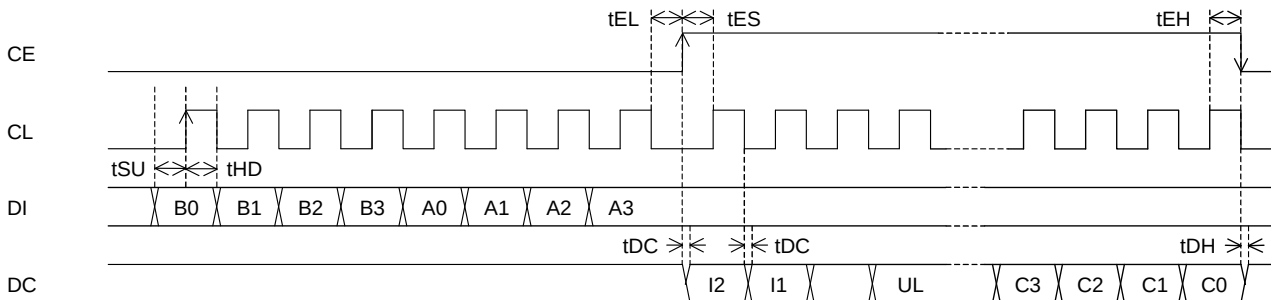


Serial data output (OUT) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75\mu s$ t_{DC} , $t_{DH} < 0.35\mu s$

CL : Normally Hi

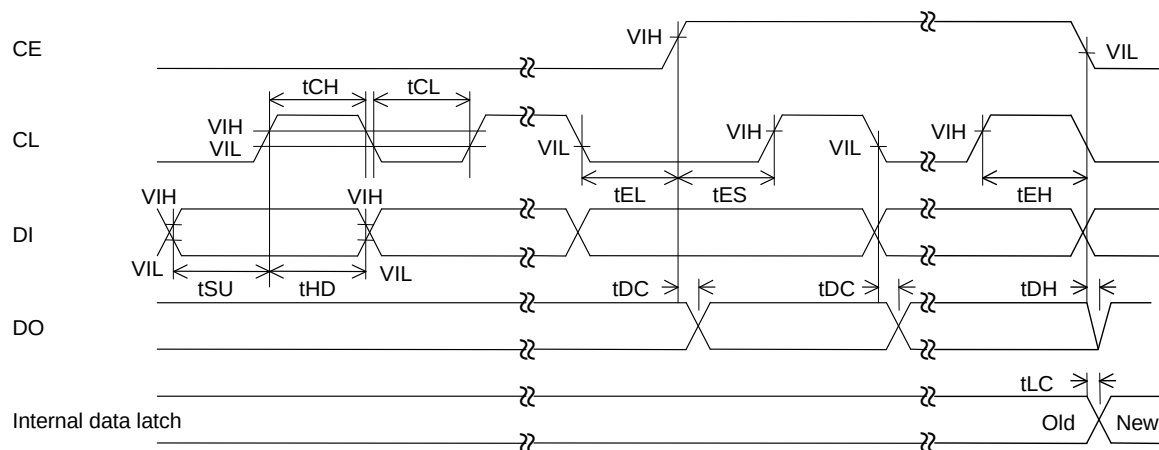


CL : Normally Hi

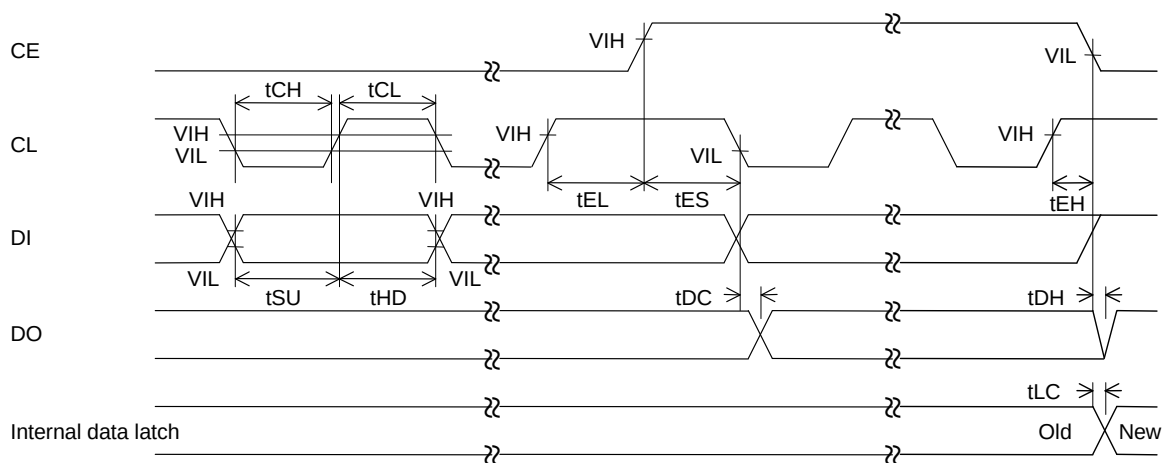


(Note) DO pin is an Nch open drain pin, so that the data varying time (t_{DC} and t_{DH}) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



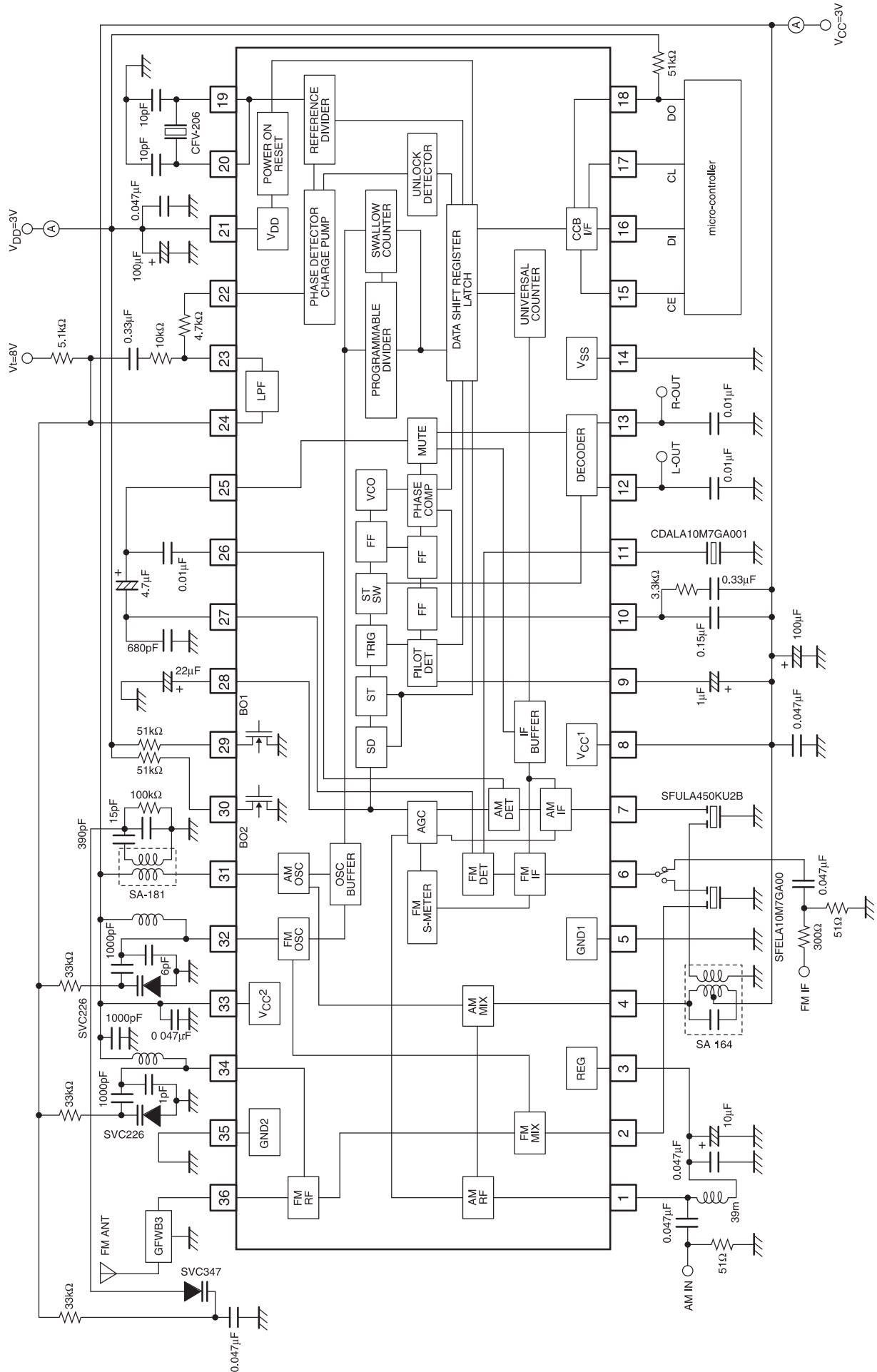
<< When CL stops at the "L" level >>



<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	tEH	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					

Test Circuit



LV23100V

Coil specifications (bottom view)

• FM-BPF : GFWB3 (Soshin) 76MHz to 108MHz		
• FM-RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T		
• FM-OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T		
• FM-IF Filter : SFELA10M7GA00 (Murata)		
• FM-Discriminator : CDALA10M7GA121 (Murata)		
• AM-OSC : SA-181 (Sumida)		
	6-4	37T
	3-1	74T
		0.06UEW
		$f_o = 796\text{kHz}$
		$Q_o \geq 80$ $L = 140\mu\text{H}$
• AM-MIX : SA-164 (Sumida)		
	1-2	122T
	4-6	9T
	2-3	62T
		0.06UEW
		$f_o = 450\text{kHz}$, $Q_o \geq 65$ $C = 180\text{pF}$
• AM-IF Filter : SFULA450KU2B (Murata)		
• MW Bar-antenna : C8E-A0105 (Toko)		
	1-2	67T
	3-4	9T
		$f_o = 796\text{kHz}$
		$Q_o = 180\text{min}$
		$L = 260\mu\text{H}$
• Crystal oscillator : CFV-206 (Citizen)		

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