



SANYO Semiconductors

DATA SHEET

LA73026AV — Monolithic Linear IC Double Scart Interface IC

Overview

This LA73026AV is a double scart (PAL/SECAM 21pin) interface IC.

Functions

- AV switches
- Changeable Gain AMP
- 6dB AMP + driver
- FSS output

Specifications

Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|----------------------|------------|-------------|------|
| Maximum supply voltage | V _{CCV} max | 24, 29 pin | 6.0 | V |
| | V _{CCA} max | 14 pin | 13.0 | V |
| Allowable power dissipation | Pd max | Ta ≤ 80°C* | 760 | mW |
| Operating temperature | Topr | | -20 to +80 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* When mounted on a 114.3×76.1×1.6mm³ glass epoxy board.

Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|---------------------|------------|--------------|------|
| Recommending operation voltage | V _{CCV} | 24, 29 pin | 5.0 | V |
| | V _{CCA} | 14 pin | 12.0 | V |
| Operating voltage range | V _{CCV} op | 24, 29 pin | 4.5 to 5.5 | V |
| | V _{CCA} op | 14 pin | 11.5 to 12.5 | V |

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Electrical Characteristics at Ta = 25°C, VCC = ±5.0V, VCCA = 12.0V

| Parameter | Symbol | Conditions | Ratings | | | Unit | |
|---|------------|---|-----------|----------|-------|------|----|
| | | | min | typ | max | | |
| Current dissipation 1 | ICC1 | Pin 24 Flow in current when non-signal | 16.0 | 24.0 | 32.0 | mA | |
| Current dissipation 2 | ICC2 | Pin 29 Flow in current when non-signal | 12.0 | 18.0 | 24.0 | mA | |
| Current dissipation 3 | ICCA | Pin 14 Flow in current when non-signal | 13.0 | 21.0 | 29.0 | mA | |
| FSS output H voltage | VHFSS | Serial control select FSS OUT H VCCA<13.0V | VCCA-1.0 | VCCA-0.5 | VCCA | V | |
| FSS output M voltage | VMFSS | Serial control select FSS OUT M VCCA<13.0V | 5.0 | 6.0 | 7.0 | V | |
| FSS output L voltage | VLSS | Serial control select FSS OUT L VCCA <13.0V | 0 | 0.1 | 0.5 | V | |
| FSS output cut off current | ICUTOFF | Flow out current when Pin 20 connecting to GND. | M | 2.0 | 3.61 | 10.0 | mA |
| | | | H | 2.0 | 3.78 | 10.0 | mA |
| External control terminal H voltage | VEXTH | RL = 1.8kΩ, VCCRL<13V | VCCRL-0.2 | VCCRL | | V | |
| External control terminal L voltage | VEXTL | RL = 1.8kΩ, VCCRL = 5V | 0 | 0.7 | 1.0 | V | |
| | | RL = 10kΩ, VCCRL = 5V | 0 | 0.15 | 1.0 | V | |
| External control terminal drive current | IDR | RL = 1.8kΩ, VCCRL = 5V | 2.2 | 2.4 | 2.78 | mA | |
| | | RL = 10kΩ, VCCRL = 5V | 400 | 485 | 500 | μA | |
| Power Save control H | VPSAVECTLH | Power Save H, control voltage of Pin 8. | 3.0 | | VCCV | V | |
| Power Save control L | VPSAVECTL | Power Save L, control voltage of Pin 8. | 0 | | 1.0 | V | |
| External mute control H | VMUTECTLH | External mute H, control voltage of Pin 9. | 3.0 | | VCCV | V | |
| External mute control L | VMUTECTL | External mute L, control voltage of Pin 9. | 0 | | 1.0 | V | |
| Video switches part | | | | | | | |
| Voltage gain V1 | VG1V | 25, 26pin output, 100% white | 5.6 | 6.1 | 6.6 | dB | |
| Voltage gain V2 | VG2V | 5 pin output G2 D6-L, 100% white | -0.4 | 0.1 | 0.6 | dB | |
| Voltage gain V3 | VG3V | 5 pin output G2 D6-H, 100% white | 5.6 | 6.1 | 6.6 | dB | |
| Frequency characteristics | VF | f = 100kHz/7MHz | -0.5 | -0.0 | 0.5 | dB | |
| DG differential gain | DG | VIN = 1Vp-p | -1.0 | 0.0 | 1.0 | % | |
| DP differential phase | DP | VIN = 1Vp-p | -1.5 | 0.0 | 1.5 | deg | |
| Output voltage | VOU | Pin 25, 26 DC voltage when non-signal. | | 1.15 | 2.0 | V | |
| Audio switches part | | | | | | | |
| Voltage gain 1A | VG1A | Serial control select 0dB. | -0.3 | 0.2 | 0.7 | dB | |
| Voltage gain 2A | VG2A | Serial control select 2dB. | 1.7 | 2.2 | 2.7 | dB | |
| Voltage gain 3A | VG3A | Serial control select 4dB. | 2.7 | 4.2 | 4.7 | dB | |
| Voltage gain 4A | VG4A | Serial control select 6dB. | 5.7 | 6.2 | 6.7 | dB | |
| Voltage gain 5A | VG5A | Serial control select 12dB. | 11.7 | 12.2 | 12.7 | dB | |
| Maximum output level | VOMAX | Output level at the time of f = 1kHz, THD = 2% | 2 | 3.0 | | Vrms | |
| Total harmonic distortion | THD | VOU = 2Vrms, f = 1kHz, AMP 0dB | | 0.007 | 0.015 | % | |
| Output noise voltage | VOISE | Rg = 1kΩ, JIS-A FILTER | | -100 | -90 | dBm | |
| Cross talk between channel | VCTKA | VIN = 1Vrms, f = 1kHz | | -90 | -75 | dB | |
| Mute attenuation | VMUTEA | VIN = 1Vrms, f = 1kHz | | -90 | -75 | dB | |
| Input impedance | ZIN | | 40 | 50 | 60 | kΩ | |
| Output off set voltage | VOFSET | Off set voltage at the time of changeover SW. | -20 | 0 | 20 | mV | |

*VCCRL:see Test Circuit.

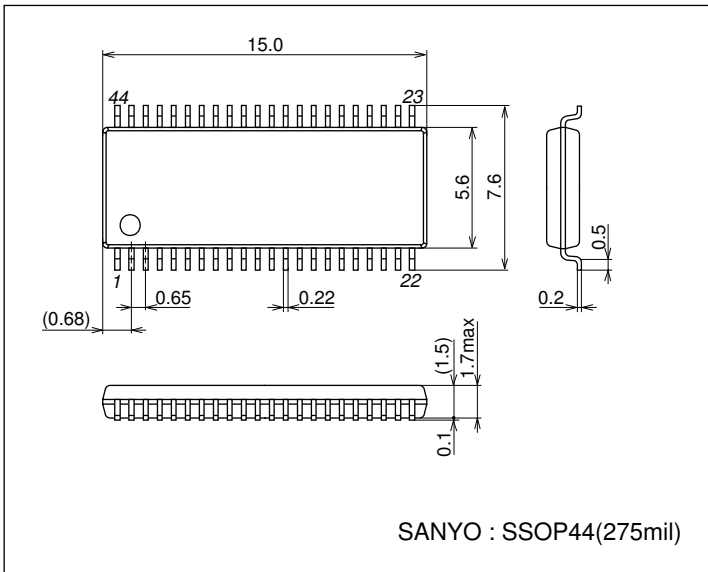
Design guarantee Items

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------|--------|--|---------|-----|-----|------|
| | | | min | typ | max | |
| Mute attenuation | VMUTEV | VIN = 1Vp-p, f = 4.43MHz | | -60 | -50 | dB |
| Cross-talk between channel | VCTKV | VIN = 1Vp-p, f = 4.43MHz Driver output terminated with 75Ω. | | -60 | -50 | dB |

Package Dimensions

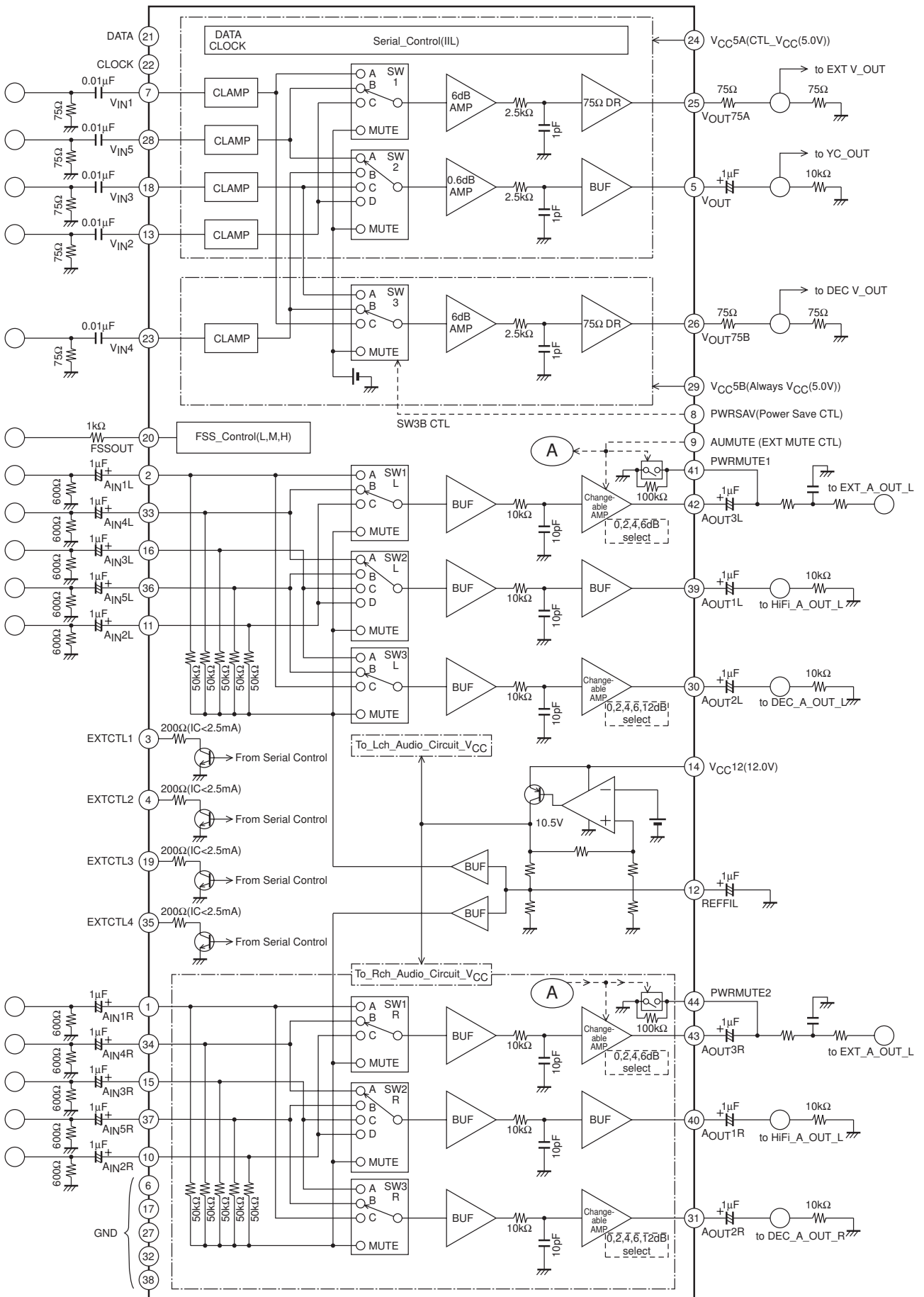
unit : mm (typ)

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Block Diagram



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Pin Function

| Pin No. | Pin name | Function | DC voltage | Equivalent circuit |
|--|--|---|---|--|
| 1 2 10 11 15 16 33 34 36 37 | A _{IN} 1R A _{IN} 1L A _{IN} 2R A _{IN} 2L A _{IN} 3R A _{IN} 3L A _{IN} 4L A _{IN} 4R A _{IN} 5L A _{IN} 5R | Audio input terminal. | 5.58V | |
| 3 4 19 35 | EXTCTL1 EXTCTL2 EXTCTL3 EXTCTL4 | General purpose output. Open collector. | 2.5mA, ON → 0.75V OFF → OPEN | |
| 5 | V _{OUT} | Video output terminal. Push-pull output Low-impedance. | 1.10V | <div style="display: flex; justify-content: space-around; margin-top: 10px;"> <div style="text-align: center;"> <p>Output Pin DC Signal wave form (AmpGain 0dB)</p> </div> <div style="text-align: center;"> <p>Output Pin DC Signal wave form (AmpGain 6dB)</p> </div> </div> |
| 6 17 27 32 38 | GND GND GND GND GND | (EXT-75Ω Driver) (DEC-75Ω Driver) | 0V | |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin name | Function | DC voltage | Equivalent circuit |
|---------------------------|--|--|--|--------------------|
| 7 13 18 23 28 | V _{IN1} V _{IN2} V _{IN3} V _{IN4} V _{IN5} | Video input terminal. Sync-tip clamp input Hi-impedance. | 1.8V | |
| | | Input Signal wave form | Input Pin DC Signal wave form | |
| 8 | PWRS _{AV} | Power save mode select pin. OPEN: L | 0.2V | |
| 9 | AUMUTE | Control terminal for audio mute. OPEN: LOW | 0.05V | |
| 12 | REFFIL | Terminal for Ref_DC ripple removing. | 4.94V | |
| 14 | V _{CC12} | V _{CC} for audio. | | |

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| Pin No. | Pin name | Function | DC voltage | Equivalent circuit |
|----------|------------------------------|---|--|--|
| 20 | FSSOUT | FSS control terminal. Output H, M, L 3 values with serial control. | H: $V_{CC}-0.5V$ M: 6V L: 0V | |
| 21 | DATA | Serial data input terminal. Conformed to I ² C BUS. | | |
| 22 | CLOCK | Serial clock input terminal. Conformed to I ² C BUS. | | |
| 24 | V_{CC5A} | Control V_{CC} for Video. Power save → open | | |
| 25 26 | V_{OUT75A} V_{OUT75B} | Video driver output terminal. Push-pull output Low-impedance. | 1.10V | |
| | | | | <p>Output Pin DC Signal wave form</p> |
| 29 | V_{CC5B} | Always V_{CC} for Video. | | |

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| Pin No. | Pin name | Function | DC voltage | Equivalent circuit |
|----------------------|--------------------------------------|--|------------|--------------------|
| 30 31 42 43 | AOUT2L AOUT2R AOUT3L AOUT3R | Audio output terminal Push-pull output Low-Impedance | 4.91V | |
| 39 40 | AOUT1L AOUT1R | Audio output terminal Push-pull output Low-Impedance | 4.91V | |
| 41 44 | PWRMUTE1 PWRMUTE2 | Output terminal of audio muting | 0V | |

Power Save

LA73024AV has two supplies 5V for Video part and 12V for audio part and FSS output. LA73024AV separates perfectly 5V system from 12V system, so it can be individually movement. For example when in the stand-by mode, if you open 14 pins but 5V supplies 24 and 29 pins, Video part and serial control part work normally. In this case audio part and FSS output don't work normally. And when you pull up 8pin and open 24 pin, IC chooses automatically video sw3-B. Consequently Ext input and Decoder output only move, you can save more power dissipation.

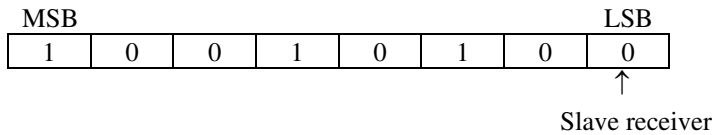
Audio Mute

LA73024AV builds in two mute transistors for reduce audio pop-noise when occur at power on and off. You can control both on serial control and on external parallel control for audio mute.

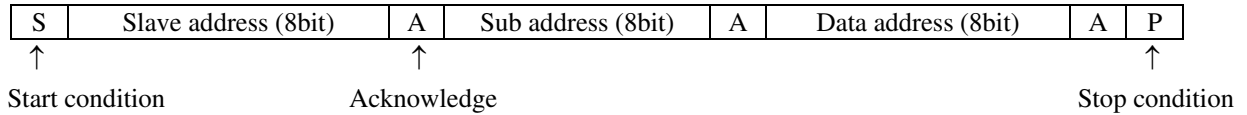
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Serial Control Specification

Slave address



Data format



Sub address and data byte table

| Sub address Hexadecimal | Data byte (Underline is initial setting.) | | | | | | | |
|----------------------------|---|---|---|--|---|---|---|------------------------------------|
| | MSB | | | | | | | LSB |
| | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 |
| 01 (0000 0001) | SW1 00: C <u>01: B</u> 10: A 11: A | | SW2 00: D 01: C 10: B 11: A | | SW3 00: C <u>01: B</u> 10: A 11: * | | FSSOUT 00: HIGH 01: HIGH 10: MID 11: LOW | |
| 02 (0000 0010) | EXT CTL1 <u>0: L</u> 1: H | EXT CTL2 <u>0: L</u> 1: H | AMP GAIN VPS OUT <u>0: 0dB</u> 1: 6dB | AUDIO AMP GAIN1 (DEC OUT) 000: 0dB <u>001: 2dB</u> 010: 4dB 011: 6dB 100: 12dB | | | AUDIO AMP GAIN2 (EXT OUT) 00: 0dB <u>01: 2dB</u> 10: 4dB 11: 6dB | |
| 03 (0000 0011) | MUTE1 VSW1 OUT 0: through <u>1: MUTE</u> | MUTE2 VSW2 OUT 0: through <u>1: MUTE</u> | MUTE3 VSW3 OUT 0: through <u>1: MUTE</u> | MUTE4 ASW1 OUT 0: through <u>1: MUTE</u> | MUTE5 ASW2 OUT 0: through <u>1: MUTE</u> | MUTE6 ASW3 OUT 0: through <u>1: MUTE</u> | EXT CTL3 <u>0: L</u> 1: H | EXT CTL4 <u>0: L</u> 1: H |

Data transfer

I²C-BUS control system is adopted in SW IC and SW IC is controlled by SCL (Serial Clock) and SDA (Serial Data) At first, please set up the START condition*¹ by these two terminals (SCL and SDA). And next, please input the 8bits data which should be synchronized with SCL into SDA terminal. Still more, please give priority to high rank bit at data transfer order (MSB → LSB). The 9th bit is called as ACK (Acknowledge), SW IC sends [0] to the SDA terminal during SCL [1] period. So, please open the port of micro-processor during this period. LA73026AV adopt auto-increment, so you input only first sub-address data (called as Group) and you can transfer data in order. As thus the Data transfer Stop condition*² is finished.

*¹ SDA rise up during SCI is [1]

*² SDA fall down during SCL is [1]

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Transfer data format

The transfer data is composed by START condition, Slave address data^{*3}, and STOP condition.

After setting up the START condition, please transfer the Slave Address (regulated as “10010100” in SW IC). Group and next control data (Please see “Data structure”)

Slave Address is composed by 7bits, and this bit 8th bit^{*4} should be set as [0].

But SW IC is not equipped with such a data out function, please keep this bit as [0].

The both of Group data and control data are composed by 8bits, and the one control action is defined with combination of these two data. And if you want to control 2 or more groups at the same mode, you can realize it by sending some control data together.

The data makes meaning with all bits, so you cannot stop the sending until all data transfer is over. But LA73026AV adopt auto-increment, for example you can stop to transfer STOP condition after group 2 data . If you want to stop transfer action, please transfer the STOP condition without fail.

^{*3} There are 3 control groups.

^{*4} This 8th bit called as R/W bit, and this bit shows the data transmission direction. [0] means send mode (accept mode with SW IC) and [1] means accept mode (send mode with SW IC) fundamentally.

Data structure

| | | | | | | | | | |
|-----------------|---------------|-----|-----|-------|-----|--------------|-----|-----|----------------|
| START condition | Slave Address | R/W | ACK | Group | ACK | Control data | ACK | ... | STOP condition |
|-----------------|---------------|-----|-----|-------|-----|--------------|-----|-----|----------------|

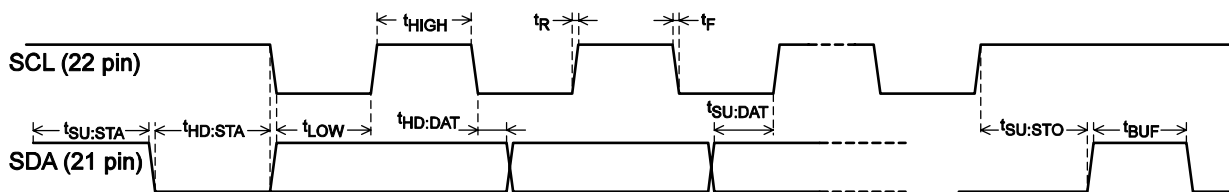
Initialize

SW IC is initialized as the following mode for circuit protection. Please see “Sub address and data byte table” on page 9.

Characteristics of the SDA and SCL 1/0 stages for SW IC

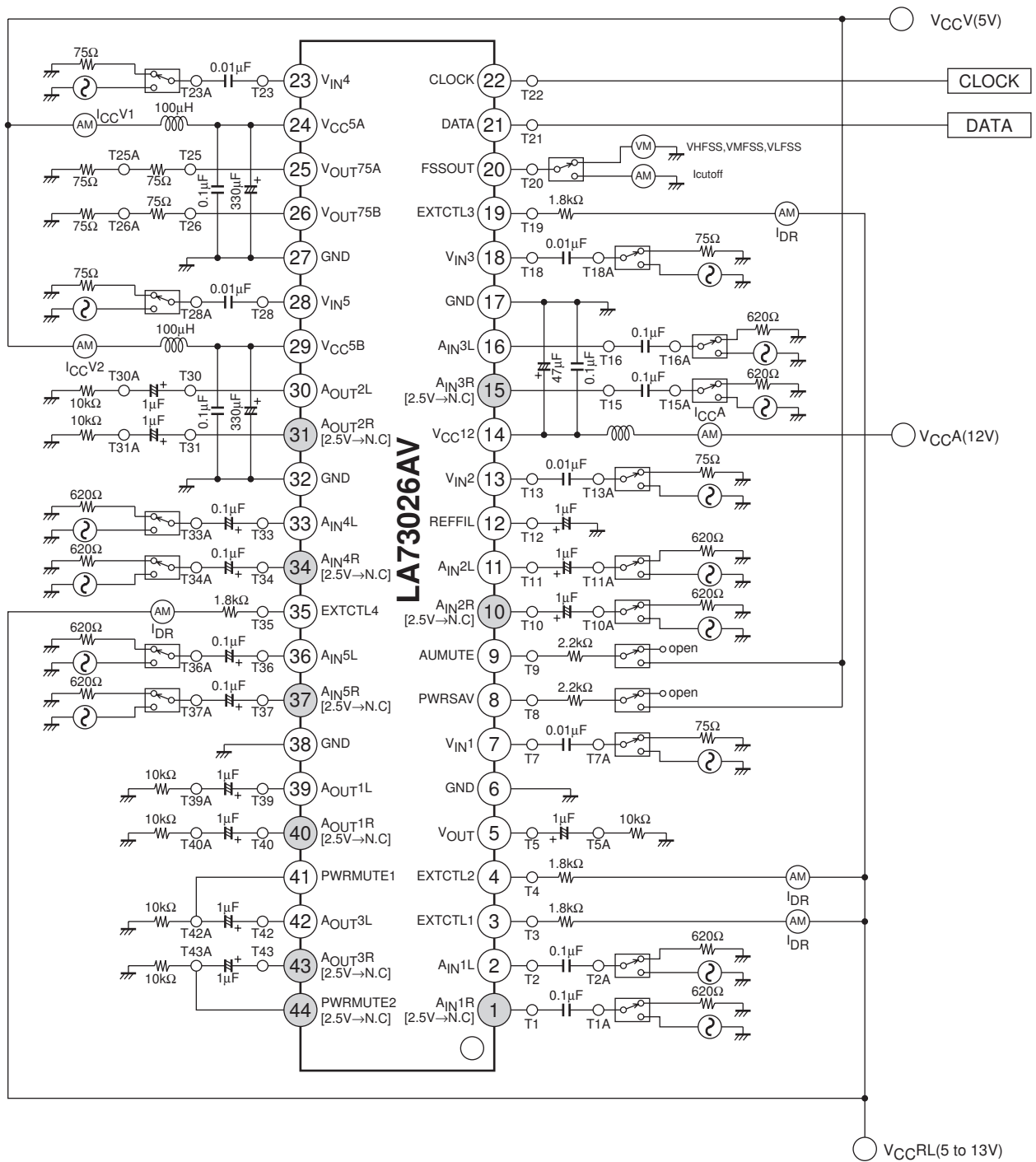
| Parameter | Symbol | Min | Max | Unit |
|---|---------------|-----|-----|---------|
| LOW level input voltage | V_{IL} | 0 | 1.0 | V |
| HIGH level input voltage | V_{IH} | 2.0 | 5.0 | V |
| LOW level output current | I_{OL} | | 3.0 | mA |
| SCL clock frequency | f_{SCL} | | 100 | kHz |
| Set-up time for a repeated START condition | $t_{SU: STA}$ | 4.7 | | μs |
| Hold time START condition. After this period, the first clock pulse is generated. | $t_{HD: STA}$ | 4.0 | | μs |
| LOW period of the SCL clock | t_{LOW} | 4.7 | | μs |
| Rise time of both SDA and SDL signals | t_R | 0 | 1.0 | μs |
| HIGH period of the SCL clock | t_{HIGH} | 4.0 | | μs |
| Fall time of both SDA and SDL signals | t_F | 0 | 1.0 | μs |
| Data hold time | $t_{HD: DAT}$ | 0 | | μs |
| Data set-up time | $t_{SU: DAT}$ | 250 | | ns |
| Set-up time for STOP condition | $t_{SU: STO}$ | 4.0 | | μs |
| BUS free time between a STOP and START condition | t_{BUF} | 4.7 | | μs |

Definition of timing

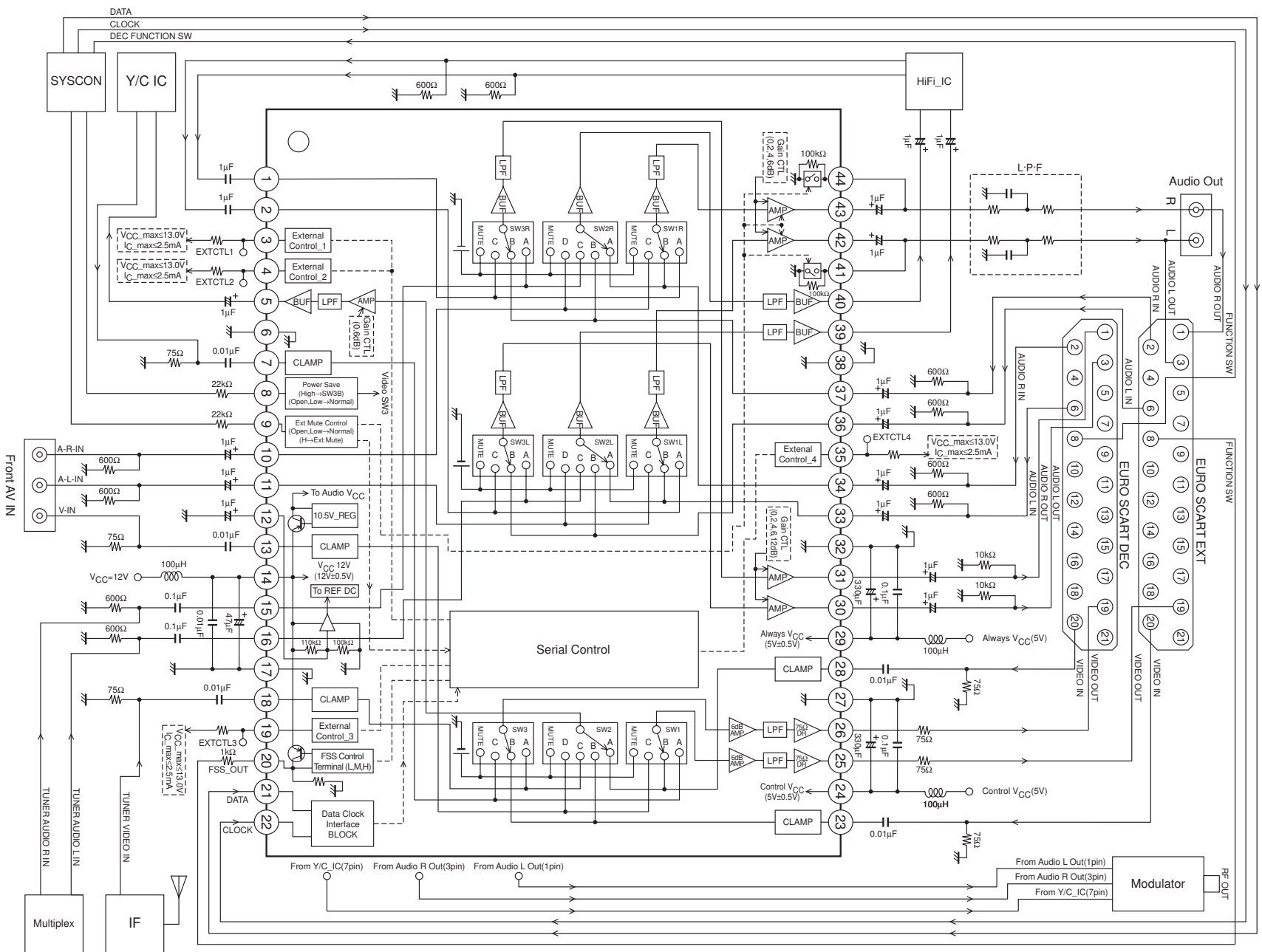


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Test Circuit



Sample Application Circuit



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