Ordering number : ENA0238

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA73024AV — Double Scart Interface IC

Overview

This LA73024AV is a double scart interface IC.

Functions

- AV switches,
- Changeable Gain AMP
- 6dB AMP+driver
- FSS output

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}V max	24, 29 pin	6.0	V
	V_{CC}A max	14 pin	13.0	V
Allowable power dissipation	Pd max	Ta ≤ 80°C*	760	mW
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 114.3×76.1×1.6mm^3 glass epoxy board.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommending operation voltage	V_{CC}V	pins 24 and 29	5.0	V
	V_{CC}A	pin 14	12.0	V
Operating voltage range	V_{CC}V op	pins 24 and 29	4.5 to 5.5	V
	V_{CC}A op	pin 14	11.5 to 12.5	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = ±5.0V, $V_{CC}A$ = 12.0V

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Current dissipation 1	$I_{CC}V1$	Pin 24 Flow in current when non-signal		16.0	24.0	32.0	mA
Current dissipation 2	$I_{CC}V2$	Pin 29 Flow in current when non-signal		12.0	18.0	24.0	mA
Current dissipation 3	$I_{CC}A$	Pin 14 Flow in current when non-signal		17.0	25.0	33.0	mA
FSS output H voltage	V_HFSS	Serial control select FSS OUT H		$V_{CC}A$-1.0	$V_{CC}A$-0.5	$V_{CC}A$	V
FSS output M voltage	V_MFSS	Serial control select FSS OUT M		5.0	6.0	7.0	V
FSS output L voltage	V_LFSS	Serial control select FSS OUT L		0	0.1	0.5	V
FSS output cut off current	I_{CUTOFF}	Flow out current when Pin 20 connecting to GND.	M	2.0	3.61	10.0	mA
			H	2.0	3.78	10.0	mA
External control terminal H voltage	V_{EXTH}	R_L = 1.8kΩ, $V_{CC}3$ < 13V		$V_{CC}3$-0.2	$V_{CC}3$		V
External control terminal L voltage	V_{EXTL}	R_L = 1.8kΩ, $V_{CC}3$ = 5V		0	0.7	1.0	V
		R_L = 10kΩ, $V_{CC}3$ = 5V		0	0.15	1.0	V
External control terminal drive current	I_{DR}	R_L = 1.8kΩ, $V_{CC}3$ = 5V		2.2	2.4	2.78	mA
		R_L = 10kΩ, $V_{CC}3$ = 5V		400	485	500	μA
External mute control H	$V_{MUTECTLH}$	External mute H, control voltage of Pin 9.		4.0		$V_{CC}V$	V
External mute control L	$V_{MUTECTLL}$	External mute L, control voltage of Pin 9.		0		1.0	V
Video switches part							
Voltage gain V1	VG_{1V}	Pins 25 and 26 output, 100% white		5.6	6.1	6.6	dB
Voltage gain V2	VG_{2V}	Pin 5 output G2 D6-L, 100% white		-0.4	0.1	0.6	dB
Voltage gain V3	VG_{3V}	Pin 5 output G2 D6-H,100% white		5.6	6.1	6.6	dB
Frequency characteristics	VF	f = 100kHz/7MHz		-0.5	-0.0	0.5	dB
DG differential gain	DG	V_{IN} = 1Vp-p		-1.0	0.0	1.0	%
DP differential phase	DP	V_{IN} = 1Vp-p		-1.5	0.0	1.5	deg
Output voltage	V_{OUT}	Pins 25 and 26 DC voltage when non-signal.			1.15	2.0	V
Audio switches part							
Voltage gain 1A	V_{G1A}	Serial control select 0dB.		-0.3	0.2	0.7	dB
Voltage gain 2A	V_{G2A}	Serial control select 2dB.		1.7	2.2	2.7	dB
Voltage gain 3A	V_{G3A}	Serial control select 4dB.		2.7	4.2	4.7	dB
Voltage gain 4A	V_{G4A}	Serial control select 6dB.		5.7	6.2	6.7	dB
Voltage gain 5A	V_{G5A}	Serial control select 6dB.		11.7	12.2	12.7	dB
Maximum output level	V_{OMAX}	Output level at the time of f = 1kHz, THD = 2%		2	3.0		Vrms
Total harmonic distortion	THD	V_{IN} = 1Vrms, f = 1kHz, AMP 0dB			0.06	0.20	%
Output noise voltage	V_{ONOISE}	Rg = 1kΩ, JIS-A FILTER			-100	-90	dBm
Cross talk between channel	V_{CTKA}	V_{IN} = 1Vrms, f = 1kHz			-90	-75	dB
Mute attenuation	V_{MUTEA}	V_{IN} = 1Vrms, f = 1kHz			-90	-75	dB
Input impedance	Z_{IN}			40	50	60	kΩ
Output off set voltage	V_{OFSET}	Off set voltage at the time of changeover SW.		-20	0	20	mV

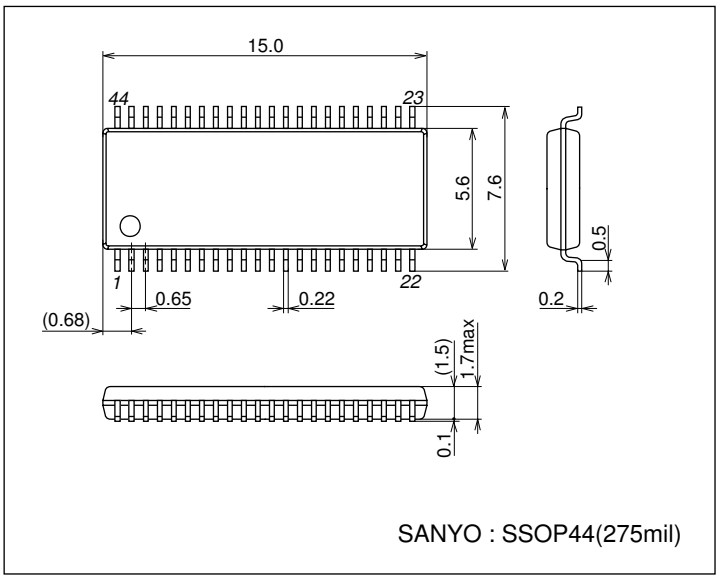
Design guarantee Items

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Mute attenuation	V_{MUTEV}	V_{IN} = 1Vp-p, f = 4.43MHz		-60	-50	dB
Cross-talk between channel	V_{CTKV}	V_{IN} = 1Vp-p, f = 4.43MHz Driver output terminated with 75Ω.		-60	-50	dB

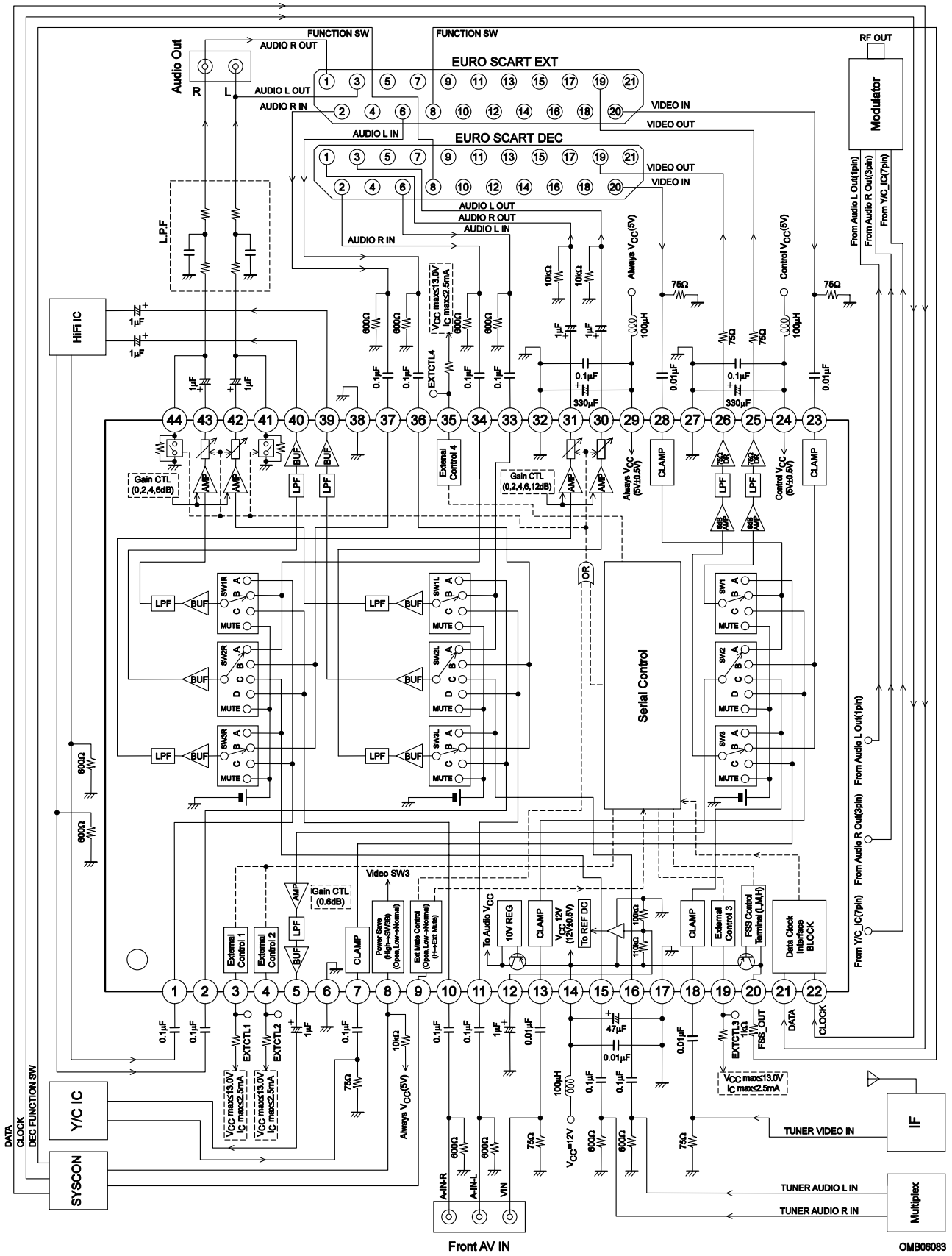
Package Dimensions

unit : mm

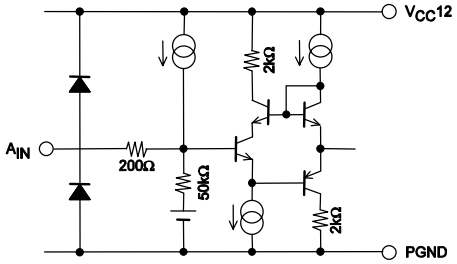
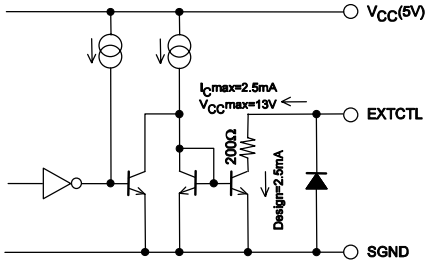
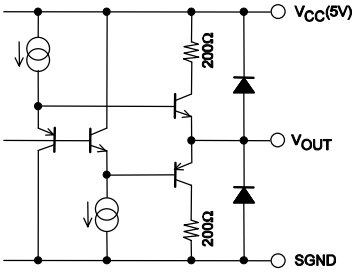
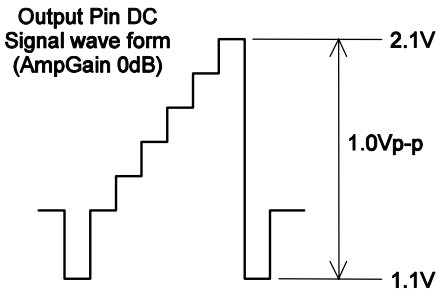
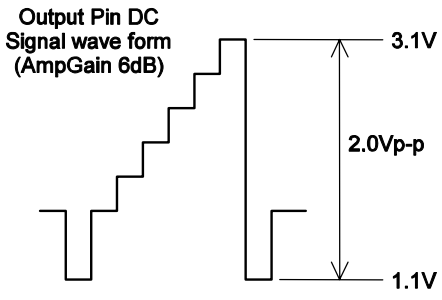
3277



Block Diagram and Sample Application Circuit



Pin Functions

Pin No.	Pin name	Function	DC voltage	Equivalent circuit
1 2 10 11 15 16 33 34 36 37	$A_{IN}1R$ $A_{IN}1L$ $A_{IN}2R$ $A_{IN}2L$ $A_{IN}3R$ $A_{IN}3L$ $A_{IN}4L$ $A_{IN}4R$ $A_{IN}5L$ $A_{IN}5R$	Audio input terminal.	5.58V	
3 4 19 35	EXTCTL1 EXTCTL2 EXTCTL3 EXTCTL4	General purpose output. Open collector.	2.5mA, ON → 0.75V OFF → OPEN	
5	V_{OUT}	Video output terminal. Push-pull output Low-impedance.	1.10V	
		 		
6 17 27 32 38	GND GND GND GND GND	(EXT-75Ω Driver) (DEC-75Ω Deiver)	0V	

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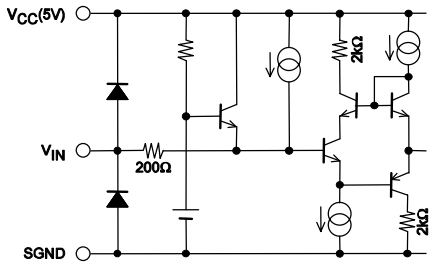
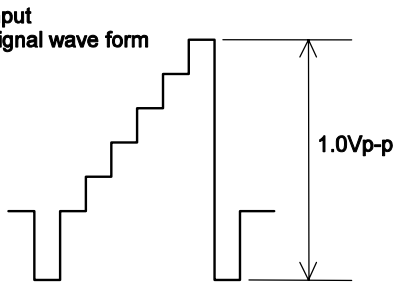
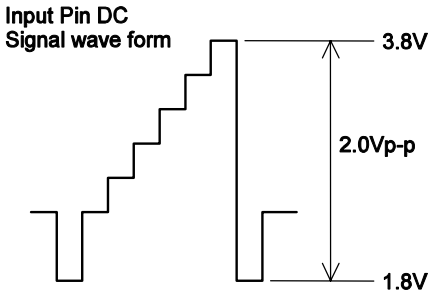
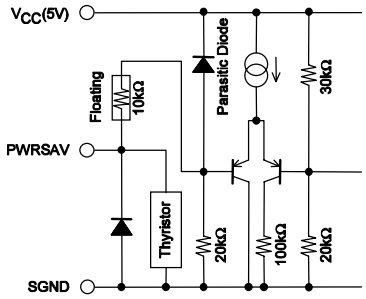
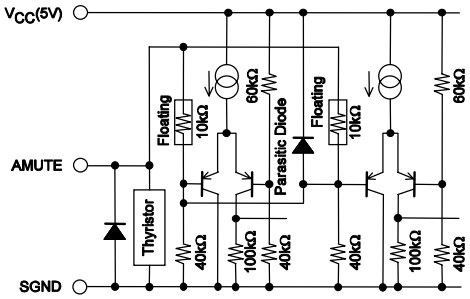
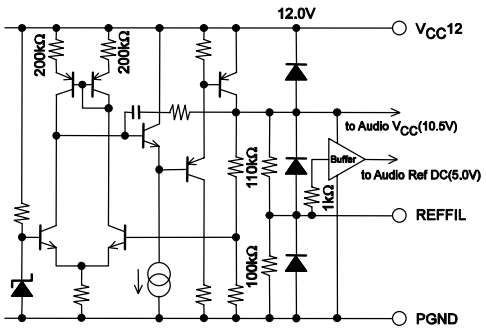
Pin No.	Pin name	Function	DC voltage	Equivalent circuit
7 13 18 23 28	$V_{IN}1$ $V_{IN}2$ $V_{IN}3$ $V_{IN}4$ $V_{IN}5$	Video input terminal. Sync-tip clamp input Hi-impedance.	1.8V	
				
8	PWRSAV	Power save mode select pin. OPEN: L	0.2V	
9	AUMUTE	Control terminal for audio mute. OPEN: LOW	0.05V	
12	REFFIL	Terminal for Ref_DC ripple removing.	4.94V	
14	$V_{CC}12$	V_{CC} for audio.		

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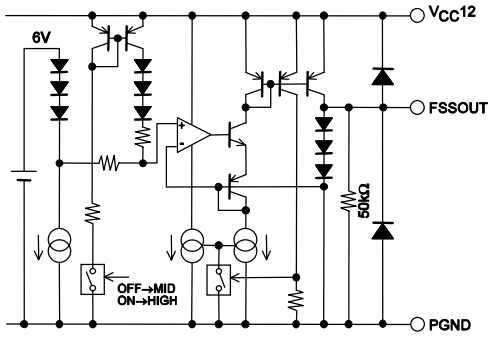
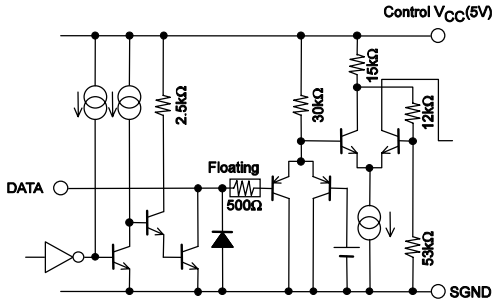
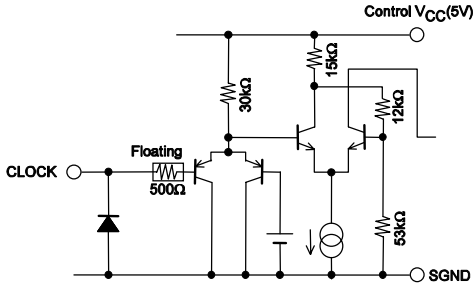
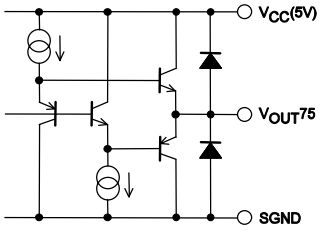
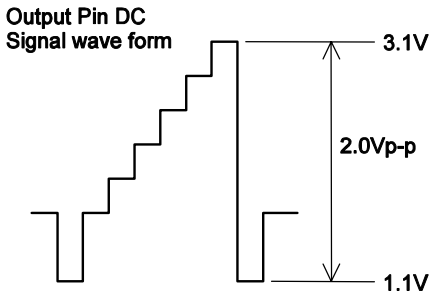
Pin No.	Pin name	Function	DC voltage	Equivalent circuit
20	FSSOUT	FSS control terminal. Output H, M, L 3 values with serial control.	H: V_{CC}-0.5V M: 6V L: 0V	
21	DATA	Serial data input terminal. Conformed to I^2C BUS.		
22	CLOCK	Serial clock input terminal. Conformed to I^2C BUS.		
24	V_{CC}5A	Control V_{CC} for Video. Power save → open		
25 26	V_{OUT}75A V_{OUT}75B	Video driver output terminal. Push-pull output Low-impedance.	1.10V	
				
29	V_{CC}5B	Always V_{CC} for Video.		

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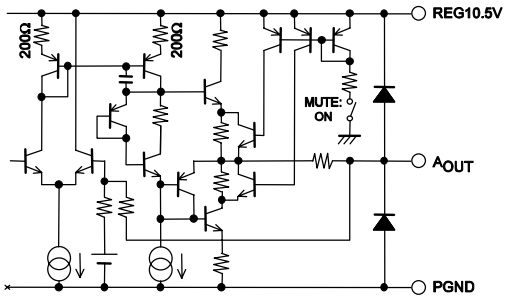
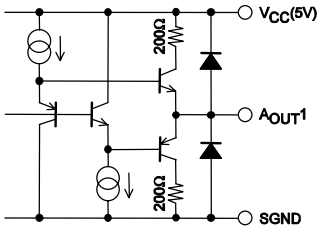
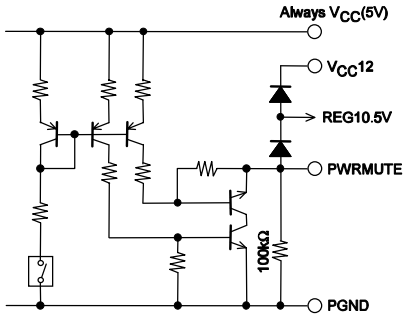
Pin No.	Pin name	Function	DC voltage	Equivalent circuit
30 31 42 43	$A_{OUT}2L$ $A_{OUT}2R$ $A_{OUT}3L$ $A_{OUT}3R$	Audio output terminal Push-pull output Low-Impedance	4.91V	
39 40	$A_{OUT}1L$ $A_{OUT}1R$	Audio output terminal Push-pull output Low-Impedance	4.91V	
41 44	PWRMUTE1 PWRMUTE2	Output terminal of audio muting	0V	

Power Save

LA73024AV has two supplies 5V for Video part and 12V for audio part and FSS output. LA73024AV separates perfectly 5V system from 12V system, so it can be individually movement. For example when in the stand-by mode, if you open 14 pins but 5V supplies 24 and 29 pins, Video part and serial control part work normally. In this case audio part and FSS output don't work normally. And when you pull up 8pin and open 24 pin , IC chooses automatically video sw3-B.Consequently Ext input and Decoder output only move , you can save more power dissipation .

Audio Mute

LA73024AV builds in two mute transistors for reduce audio pop-noise when occur at power on and off. You can control both on serial control and on external parallel control for audio mute.

Serial Control Specification

Slave address

MSB							LSB
1	0	0	1	0	0	0	0

↑

Slave receiver

Data format

S	Slave address (8bit)	A	Sub address (8bit)	A	Data address (8bit)	A	P

↑ Start condition ↑ Acknowledge ↑ Stop condition

Sub address and data byte table

Sub address Hexadecimal	Data byte (Underline is initial setting.)							
	D8	D7	D6	D5	D4	D3	D2	D1
01 (0000 0001)	SW1 00: C 01: B 10: A 11: A		SW2 00: D 01: C 10: B 11: A		SW3 00: C 01: B 10: A 11: *		FSSOUT 00: HIGH 01: HIGH 10: MID 11: LOW	
02 (0000 0010)	EXT CTL1 0: L 1: H	EXT CTL2 0: L 1: H	AMP GAIN VPS OUT 0: 0dB 1: 6dB	AUDIO AMP GAIN1 (DEC OUT) 000: 0dB 001: 2dB 010: 4dB 011: 6dB 100:12dB			AUDIO AMP GAIN2 (EXT OUT) 00: 0dB 01: 2dB 10: 4dB 11: 6dB	
03 (0000 0011)	MUTE1 VSW1 OUT 0: through 1: MUTE	MUTE2 VSW2 OUT 0: through 1: MUTE	MUTE3 VSW3 OUT 0: through 1: MUTE	MUTE4 ASW1 OUT 0: through 1: MUTE	MUTE5 ASW2 OUT 0: through 1: MUTE	MUTE6 ASW3 OUT 0: through 1: MUTE	EXT CTL3 0: L 1: H	EXT CTL4 0: L 1: H

Data transfer

I^2C-BUS control system is adopted in SW IC and SW IC is controlled by SCL (Serial Clock) and SDA (Serial Data) At first, please set up the START condition[*1] by these two terminals (SCL and SDA). And next, please input the 8bits data which should be synchronized with SCL into SDA terminal. Still more, please give priority to high rank bit at data transfer order (MSB → LSB). The 9th bit is called as ACK (Acknowledge), SW IC sends [0] to the SDA terminal during SCL [1] period. So, please open the port of micro-processor during this period. LA73024AV adopt auto-increment, so you input only first sub-address data (called as Group) and you can transfer data in order. As thus the Data transfer Stop condition[*2] is finished.

[*1] SDA rise up during SCI is [1]

[*2] SDA fall down during SCL is [1]

Transfer data format

The transfer data is composed by START condition, Slave address data[*3], and STOP condition.
After setting up the START condition, please transfer the Slave Address (regulated as "1001000" in SW IC). Group and next control data (Please see the Fig. 1)
Slave Address is composed by 7bits, and this bit 8th bit[*4] should be set as [0].
But SW IC is not equipped with such a data out function, please keep this bit as [0].
The both of Group data and control data are composed by 8bits, and the one control action is defined with combination of these two data. And if you want to control 2 or more groups at the same mode, you can realize it by sending some control data together.
The data makes meaning with all bits, so you cannot stop the sending until all data transfer is over. But LA73024AV adopt auto-increment, for example you can stop to transfer STOP condition after group 2 data . If you want to stop transfer action, please transfer the STOP condition without fail.

[*3] There are 3 control groups.

[*4] This 8th bit called as R/W bit, and this bit shows the data transmission direction. [0] means send mode (accept mode with SW IC) and [1] means accept mode (send mode with SW IC) fundamentally.

Data structure

START condition	Slave Address	R/W	ACK	Group	ACK	Control data	ACK	⋯	STOP condition

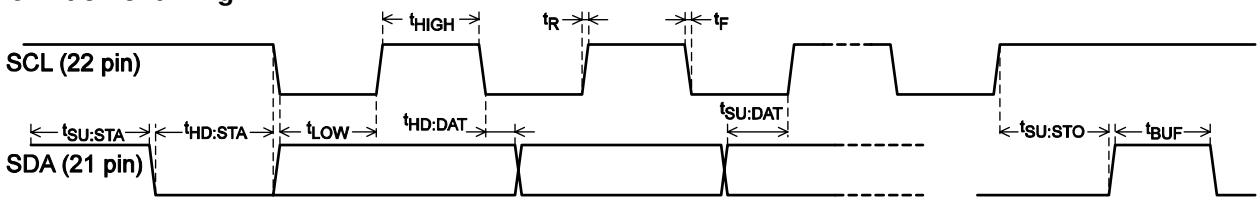
Initialize

SW IC is initialized as the following mode for circuit protection. Please see "Sub address and data byte table" on page 9.

Characteristics of the SDA and SCL 1/0 stages for SW IC

Parameter	Symbol	min	max	unit
LOW level input voltage	V_{IL}	0	1.5	V
HIGH level input voltage	V_{IH}	3.5	5.0	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}		100	kHz
Set-up time for a repeated START condition	$t_{SU: STA}$	4.7		µs
Hold time START condition. After this period, the first clock pulse is generated.	$t_{HD: STA}$	4.0		µs
LOW period of the SCL clock	t_{LOW}	4.7		µs
Rise time of both SDA and SDL signals	t_R	0	1.0	µs
HIGH period of the SCL clock	t_{HIGH}	4.0		µs
Fall time of both SDA and SDL signals	t_F	0	1.0	µs
Data hold time	$t_{HD: DAT}$	0		µs
Data set-up time	$t_{SU: DAT}$	250		ns
Set-up time for STOP condition	$t_{SU: STO}$	4.0		µs
BUS free time between a STOP and START condition	t_{BUF}	4.7		µs

Definition of timing



Test Circuit