Ordering number : ENA0569A

SANYO Semiconductors
DATA SHEET

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LC74736PT — CMOS IC On-Screen Display Controller

Overview

The LC74736PT is an on-screen display CMOS IC that displays characters and patterns on a TV screen under the control of a microcontroller.
For QVGA display, the LC74736PT supports the use of both a 16 × 16 dot character font and a 16 × 16 dot graphic font with 16 colors.
For WVGA display, the LC74736PT supports the use of both a 24 × 32 dot character font and a 24 × 32 dot graphic font with 16 colors.
The LC74736PT can also implement extremely varied displays by the use of an external ROM.
The LC74736PT supports both QVGA (480×234) and WVGA (800×480).

Features

(1) Screen structure
Main: 2 screens (1 screen for WVGA display)
30 characters×15 lines (up to 450 characters) on a QVGA panel
33 characters×15 lines (up to 495 characters) on a WVGA panel
(Up to 34 characters×18 lines)
Wallpaper display screen:
QVGA mode: maximum Permanent repetition of a 4×4 (horizontal×vertical) character pattern
WVGA mode: maximum Permanent repetition of a 2×2 (horizontal×vertical) character pattern

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(2) Character structure
QVGA mode: About 9MHz
16 dots (horizontal) ×16 dots (vertical): Character display
16 dots (horizontal) ×16 dots (vertical): Graphic glyph display
WVGA mode: About 33.2MHz
24 dots (horizontal) ×32 dots (vertical): Character display
24 dots (horizontal) ×32 dots (vertical): Graphic glyph display
Character display clock:
LC oscillator (about 10MHz)
External clock signal input (up to 40MHz)
Built-in PLL (VCO) (7 to 40MHz)

(3) Number of characters
QVGA mode
Up to 16384 characters when an external 16-bit 16M ROM is used.
WVGA mode
Up to 4096 characters when an external 16-bit 16M ROM is used.
No internal ROM
Internal character RAM QVGA: 4 characters, WVGA: 1 character

(4) Character sizes: Four horizontal sizes (1×, 2×, 3×, and 4×)
Four vertical sizes (1×, 2×, 3×, and 4×)
(The character size is specified in line units.)

(5) Display start positions: 1024 positions in the horizontal direction and 512 positions in the vertical direction.
Setting units: Horizontal: 1 dot (in screen units)
Vertical: 1 dot (in screen units)

(6) Display functions
- Blinking specification (in character units)
  Period: 1/64, 1/32, and 1/16 of the vertical sync signal (in screen units)
  Duty: Fixed at 50%
- Box (raised or recessed) display
  Raised/recessed specification (in character units)
  Left: Off/on specification (in character units)
  Right: Off/on specification (in character units)
  Top: Off/on specification (in character units)
  Bottom: Off/on specification (in character units)
- Border specification (in line units): Only valid with glyphs from the character font.

(7) Color specification
Character
- Character color (in character units): 1 of 16 colors can be specified.
- Character background color (in character units): 1 of 16 colors can be specified.
- Border color (in line units): 1 of 16 colors can be specified.

Graphic
- 16 types can be specified by ROM data

Graphic 2
- 16 types can be specified by ROM data
  1 color type can be changed.

Graphic 3
- 16 types can be specified by ROM data
  1 color table type can be changed.
- Box (raised or recessed) color (line units): 1 of 16 colors can be specified.
- Background color (screen units): 1 of 16 colors can be specified.

(8) Color table (palette)
- Sixteen colors can be selected from a set of 4096 colors (One of which is specified to be transparent.)
- Number of color tables: 4. This allows up to 64 colors to be displayed at the same time.

(9) Wallpaper screen (Graphics glyphs only)
Wallpaper display: Repeated display under the main screen
(up to 4 characters horizontally by 4 characters vertically).
Sprite character display: Displayed above the main screen
(up to 4 characters horizontally by 4 characters vertically).

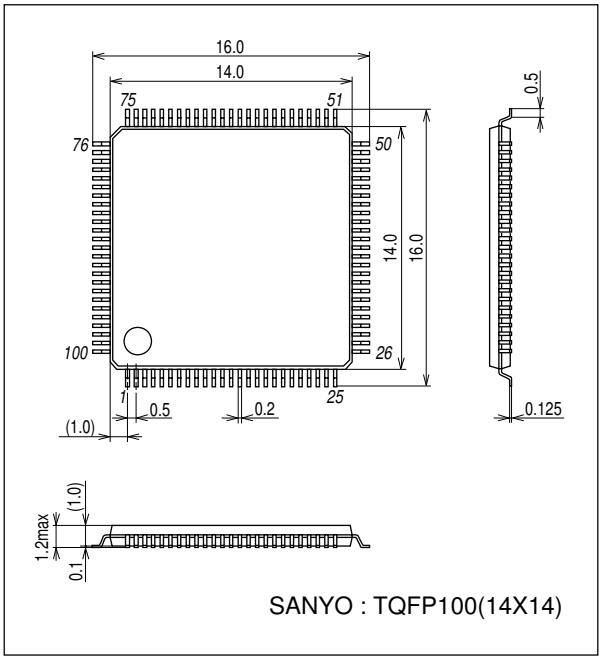
(10) Line spacing control
0-15 scan lines (in line units)

(11) Output
Analog RGB output(to 20MHz)
Digital RGB output (4 bits per color)
BLK (OSD display period signal)

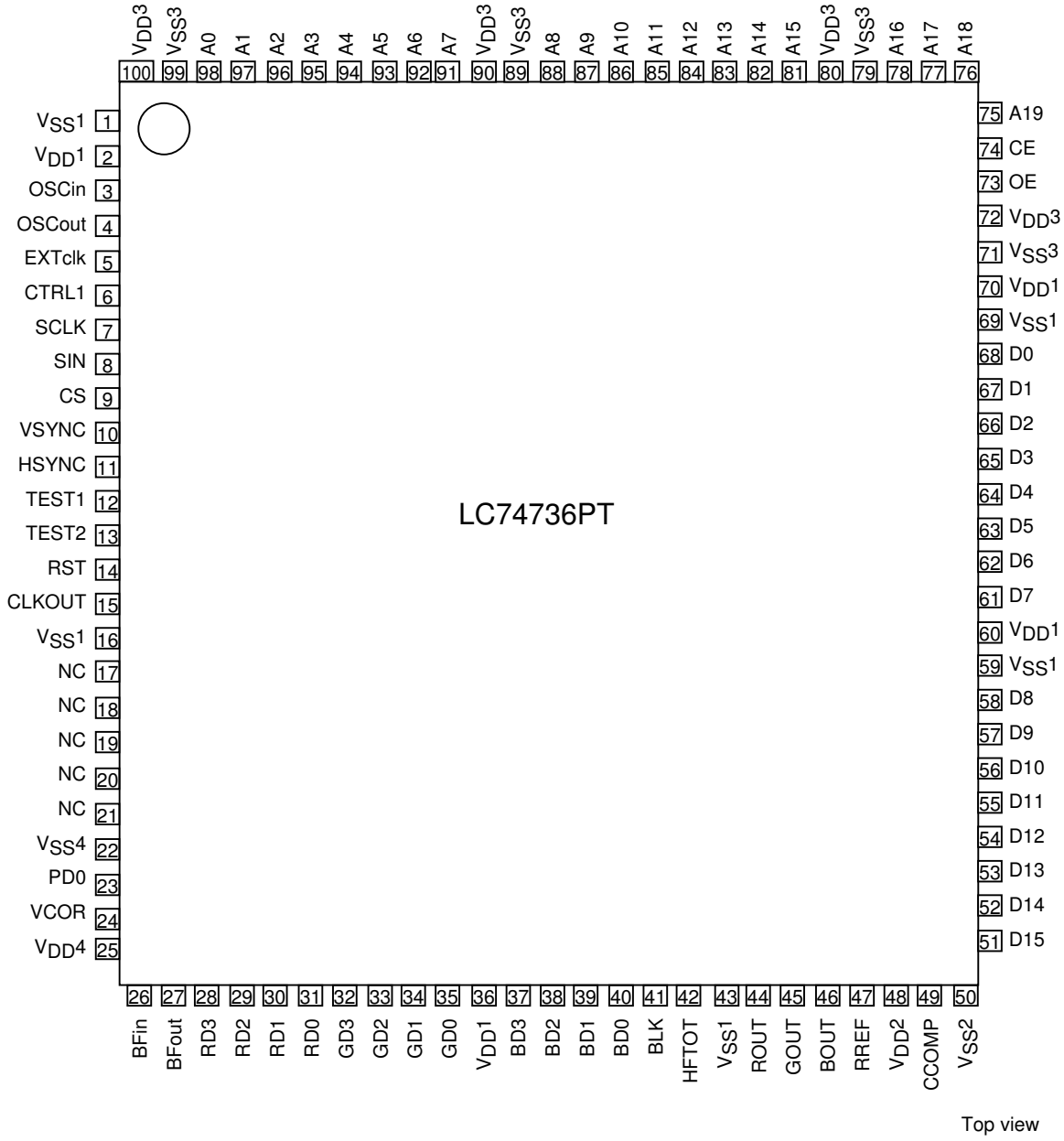
Package: TQFP100
Voltage: 3.3V

Package Dimensions

unit : mm (typ)
3274



Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Type	Functional description
1	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
2	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V
3	OSCin	LC oscillator	Connect to the character output dot clock generator oscillator coil and capacitor.
4	OSCout		
5	EXTclk	External clock signal input	Receives an external clock signal. Capacitor coupling, 50% duty cycle, 0.5Vp-p or higher
6	CTRL1	OSCin oscillator input control	Switches between external clock input mode and LC oscillator mode. Low: LC oscillator, high: external clock input MORE+ OR control with MORE+ command
7	SCLK	Clock input	Clock input for the serial data input system MORE+ (This input has hysteresis characteristics.)
8	SIN	Data input	Serial data input MORE+ (This input has hysteresis characteristics.)
9	$\overline{CS}$	Enable input	Enable input for the serial data input system. Serial data input is enabled when this pin is set low. MORE+ (This input has hysteresis characteristics.)
10	VSYNC	Vertical sync signal input	Vertical sync signal input MORE+ (This input has hysteresis characteristics.)
11	HSYNC	Horizontal sync signal input	Horizontal sync signal input MORE+ (This input has hysteresis characteristics.)
12	TEST1	Test mode control 1	Test mode control 1 Low: normal operation, high: test mode MORE+
13	TEST2	Test mode control 2	Test mode control 2 Low: normal operation, high: test mode (scan mode) MORE+
14	$\overline{RST}$	Reset input	System reset input MORE+ (This input has hysteresis characteristics.)
15	CLKOUT	Clock output	Clock output
16	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
17	NC		
18	NC		
19	NC		
20	NC		
21	NC		
22	$V_{SS}4$	Ground	Connect a ground tro this pin. (PLL system power supply)
23	PD0	PLL charge pump output PLL VCO control voltage input	Charge pump output Connect a LPF (lug lead filter) to this pin. Voltage input for internal VCO control
24	VCOR	VCO variable range adjustment	Used to adjust variable voltage range of internal VCO. Connect a resistor to this pin.
25	$V_{DD}4$	Power supply (+3.3V)	PLL system power supply: +3.3V
26	BFin	Amplifier input	Oscillation input for external VCO
27	BFout	Amplifier output	Oscillation output for external VCO
28	RD3	Rout output: bit 3	Rout output This is a 4-bit digital output with values from 0000 to 1111.
29	RD2	Rout output: bit 2	
30	RD1	Rout output: bit 1	
31	RD0	Rout output: bit 0	
32	GD3	Gout output: bit 3	Gout output This is a 4-bit digital output with values from 0000 to 1111.
33	GD2	Gout output: bit 2	
34	GD1	Gout output: bit 1	
35	GD0	Gout output: bit 0	
36	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V

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Pin No.	Symbol	Type	Functional description
37	BD3	Bout output: bit 3	Bout output This is a 4-bit digital output with values from 0000 to 1111.
38	BD2	Bout output: bit 2	
39	BD1	Bout output: bit 1	
40	BD0	Bout output: bit 0	
41	BLK	Blanking signal output	This signal indicates the OSD display period.
42	HFTOT	Halftone control signal output	OSD halftone period control signal Synthesized in the next stage IC.
43	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
44	Rout	Rout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
45	Gout	Gout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
46	Bout	Bout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
47	RREF	Reference resistor connection	Connect a reference register to this pin.
48	$V_{DD}2$	Power supply (+3.3V)	D/A converter power supply: +3.3V
49	CCOMP	Phase correction capacitor connection	Capacitor connection: 1.5µF
50	$V_{SS}2$	Ground	Connect a ground to this pin. (D/A converter ground)
51	D15	Data input 15	ROM data input 15. MORE+ [MSB]
52	D14	Data input 14	ROM data input 14. MORE+
53	D13	Data input 13	ROM data input 13. MORE+
54	D12	Data input 12	ROM data input 12. MORE+
55	D11	Data input 11	ROM data input 11. MORE+ [MSB]
56	D10	Data input 10	ROM data input 10. MORE+
57	D9	Data input 9	ROM data input 9. MORE+
58	D8	Data input 8	ROM data input 8. MORE+
59	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
60	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V
61	D7	Data input 7	ROM data input 7. MORE+
62	D6	Data input 6	ROM data input 6. MORE+
63	D5	Data input 5	ROM data input 5. MORE+
64	D4	Data input 4	ROM data input 4. MORE+
65	D3	Data input 3	ROM data input 3. MORE+
66	D2	Data input 2	ROM data input 2. MORE+
67	D1	Data input 1	ROM data input 1. MORE+
68	D0	Data input 0	ROM data input 0. MORE+ [LSB][LSB]
69	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
70	$V_{DD}1$	Power supply (+3.3V)	Power supply: (+3.3V: Digital system)
71	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
72	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
73	$\overline{OE}$	Output enable	ROM output enable output. This is an active low output.
74	$\overline{CE}$	Chip enable	ROM chip enable output. This is an active low output.
75	A19	Address output 19	ROM address output 19
76	A18	Address output 18	ROM address output 18
77	A17	Address output 17	ROM address output 17
78	A16	Address output 16	ROM address output 16
79	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
80	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
81	A15	Address output 15	ROM address output 15
82	A14	Address output 14	ROM address output 14
83	A13	Address output 13	ROM address output 13
84	A12	Address output 12	ROM address output 12
85	A11	Address output 11	ROM address output 11

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Pin No.	Symbol	Type	Functional description
86	A10	Address output 10	ROM address output 10
87	A9	Address output 9	ROM address output 9
88	A8	Address output 8	ROM address output 8
89	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
90	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
91	A7	Address output 7	ROM address output 7
92	A6	Address output 6	ROM address output 6
93	A5	Address output 5	ROM address output 5
94	A4	Address output 4	ROM address output 4
95	A3	Address output 3	ROM address output 3
96	A2	Address output 2	ROM address output 2
97	A1	Address output 1	ROM address output 1
98	A0	Address output 0	ROM address output 0
99	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
100	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$,$V_{DD}2$, and $V_{DD}4$	V_{SS}-0.3 to V_{SS}+4.6	V
	$V_{DD}3$	$V_{DD}3$	V_{SS}-0.3 to V_{SS}+6.0	V
Input voltage	V_{IN}	All input pins	V_{SS}-0.3 to $V_{DD}1$+0.3	V
Output voltage	$V_{OUT}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, HFTOT outputs	V_{SS}-0.3 to $V_{DD}1$+0.3	V
	$V_{OUT}2$	A0 to 19, $\overline{CE}$, $\overline{OE}$ outputs	V_{SS}-0.3 to $V_{DD}3$+0.3	V
Maximum power dissipation	Pd max		275	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$, 2, and $V_{DD}4$	3.0	3.3	3.6	V
	$V_{DD}3$	$V_{DD}3$	3.0	3.3	5.5	V
Input high-level voltage	$V_{IH}1$	CTRL1, TEST1, TEST2	0.7$V_{DD}1$		5.5	V
	$V_{IH}2$	SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	0.8$V_{DD}1$		5.5	V
	$V_{IH}3$	D0 to D15	0.7$V_{DD}1$		5.5	V
Input low-level voltage	$V_{IL}1$	CTRL1, TEST1, TEST2	V_{SS}-0.3		0.3$V_{DD}1$	V
	$V_{IL}2$	SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	V_{SS}-0.3		0.2$V_{DD}1$	V
	$V_{IH}3$	D0 to D11	V_{SS}-0.3		0.3$V_{DD}1$	V
Oscillator frequency (LC)	FOSC1	OSCin and OSCout oscillator pins (LC oscillator)		10		MHz
External clock input	FOSC2	OSCin, $V_{DD}1$ = 3.3V		33	40	MHz
	$V_{IN}1$	$V_{DD}1$ = 3.3V CTRL1 = high	0.5		3.3	Vp-p
Oscillator frequency (VCO)	FOSC3	VCO oscillator (internal)	7		40	MHz
D/A converter (4-bit, 3 ch) When maximum output voltage = 0.7V	Vrefda	Reference voltage		1.1		V
	Rfda	Output load resistance ROUT, GOUT, BOUT	120		225	Ω
	Rref	Reference load resistance, RREF		1100		Ω

Electrical Characteristics at Ta = -40 to +85°C, V_{DD} = 3.3V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Output high-level voltage	$V_{OH}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, and HFTOT outputs	$V_{DD}1$ = 3.0V $I_{OH}1$ = -8mA	$V_{DD}1$ -0.8			V
	$V_{OH}2$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 3.0V $I_{OH}2$ = -8mA	$V_{DD}3$ -0.8			V
	VOH3	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 4.5V $I_{OH}3$ = -8mA	$V_{DD}3$ -0.8			V
Output low-level voltage	$V_{OL}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, and HFTOT outputs	$V_{DD}1$ = 3.0V $I_{OL}1$ = 8mA			0.4	V
	$V_{OL}2$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 3.0V $I_{OL}2$ = 8mA			0.4	V
	$V_{OL}3$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 4.5V $I_{OL}3$ = 8mA			0.4	V
Input current	$I_{IH}1$	CTRL1, TEST1, TEST2 SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	V_{IN} = $V_{DD}1$			10	µA
	$I_{IH}2$	D0 to D15	V_{IN} = $V_{DD}3$			10	µA
	$I_{IL}1$	CTRL1, TEST1, TEST2 SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC	V_{IN} = V_{SS}	-10			µA
	$I_{IL}2$	D0 to D15	V_{IN} = V_{SS}	-10			µA
Operating current drain	$I_{DD}1$	$V_{DD}1$	All outputs open OSCin: 20MHz			25	mA
	$I_{DD}2$	$V_{DD}2$	D/A on			22	mA
	$I_{DD}3$	$V_{DD}3$				10	mA
	$I_{DD}4$	$V_{DD}4$	VCO on			22	mA
D/A converter	CLK	Clock frequency				20	MHz
	V max	Maximum output voltage	$V_{DD}2$ = 3.3V	0.25		1.5	V
	V min0	Minimum output voltage	$V_{DD}2$ = 3.3V		0		V

Timing Characteristics

OSD Write (See figure 1.) at Ta = -40 to +85°C, $V_{DD}1$ = 3.3V ± 0.3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_w(sclk)	SCLK	200			ns
	t_w(cs)	$\overline{CS}$ (The period $\overline{CS}$ is high)	1			µs
Data setup time	t_{su}(cs)	$\overline{CS}$	200			ns
	t_{su}(sin)	SIN	200			ns
Data hold time	t_h(cs)	$\overline{CS}$	2			µs
	t_h(sin)	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	RAM data write time	1			µs

Supplementary Materials

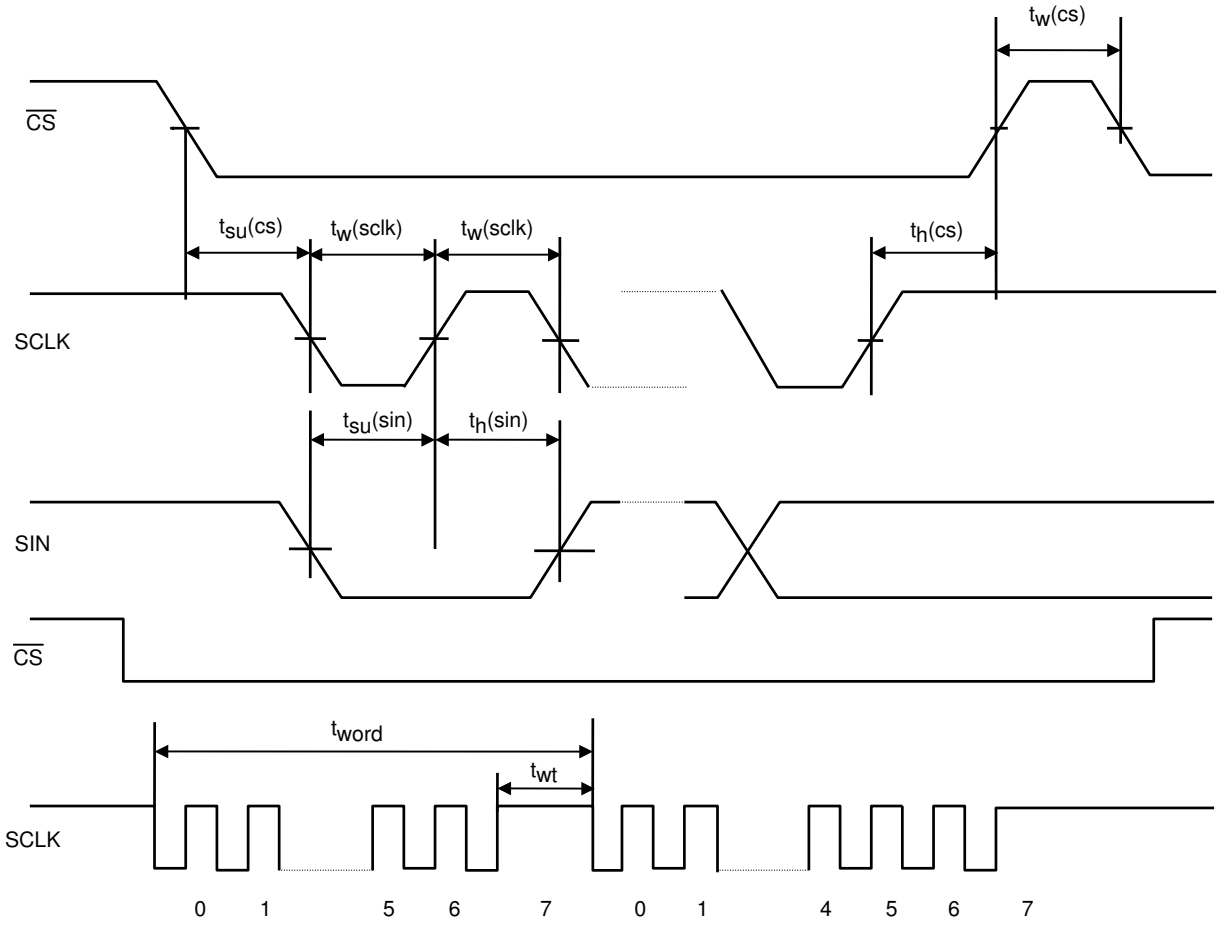
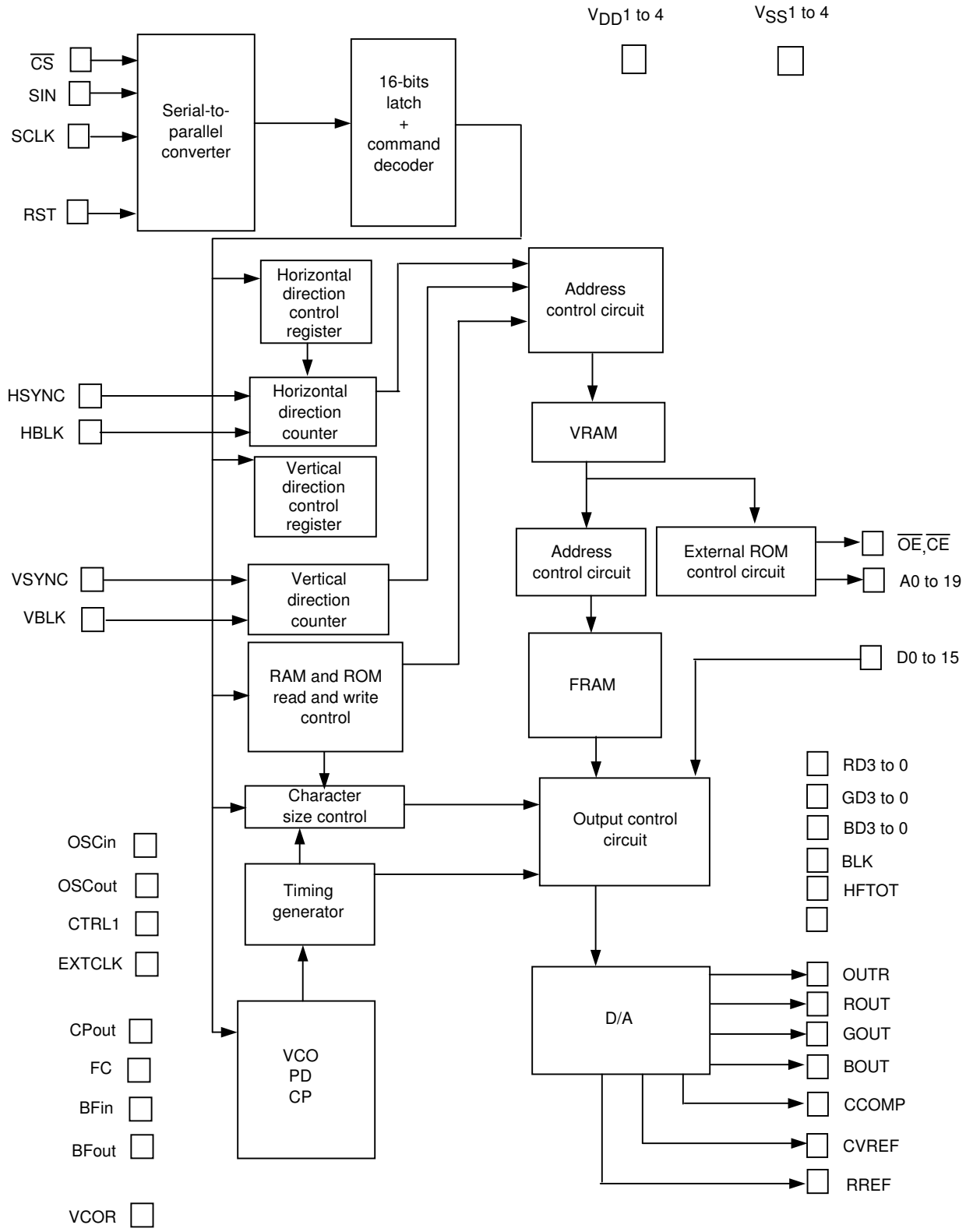


Figure 1 OSD Serial Data Input Timing

System Block Diagram



Display Control Commands

The display control commands have serial input format that consists of 8-bit units transmitted LSB first. A commands consists of a command identification code in the first byte and data in the second and following bytes. Both a first byte and a second byte (16 bits) must be transmitted for each command. Commands 10, 11, 12, 6C1, and 701 set the IC to continuous write mode. (Continuous write mode is cleared by setting the CS pin high.)

Display Control Command Table

Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND00 (Write address) Main 1: V	1	0	0	0	0	0	0	0	0	0	0	V14	V13	V12	V11	V10
COMMAND01 (Write address) Main 1: H	1	0	0	0	0	0	1	0	0	0	H15	H14	H13	H12	H11	H10
COMMAND02 (Write address) Main 2: V	1	0	0	0	0	1	0	0	0	0	0	V24	V23	V22	V21	V20
COMMAND03 (Write address) Main 2: H	1	0	0	0	0	1	1	0	0	0	H25	H24	H23	H22	H21	H20
COMMAND04 (Write address) Sub	1	0	0	0	1	0	0	0	SV1	SV0	0	0	0	0	SH1	SH0
COMMAND10 (Character write) Main 1	1	0	0	1	0	0	RM2	RM1[1]	HF1	HF0	at	BXS	BXL	BXR	BXU	BXD
								[2]	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND11 (Character write) Main 2	1	0	0	1	0	1	RM2	RM1[1]	HF1	HF0	at	BXS	BXL	BXR	BXU	BXD
								[2]	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND12 (Character write) Sub	1	0	0	1	1	0	RM2	RM1[1]	0	0	0	0	0	0	0	0
								[2]	0	0	0	0	0	0	0	0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND20 (System control)	1	0	1	0	0	0	0	0	TST MD2	TST MD1	SYS RST	FRM ERS	CT ERS	SRM ERS	MRM ER2	MRM ERS1
COMMAND21 (Display control)	1	0	1	0	0	0	0	1	BK 12	BK 02	BK 11	BK 01	DSP BG	DSP GS	DSP GM2	DSP GM1
COMMAND22 (I/O polarity control 1)	1	0	1	0	0	0	1	0	0	BLOP	BLO 2	BLO 1	BLO 0	CKP	VIP	HIP
COMMAND23 (Screen background color)	1	0	1	0	0	0	1	1	DPM HC1	DPM HC0	BGC T1	BGC T0	BGC 3	BGC 2	BGC 1	BGC 0
COMMAND24 (I/O polarity control 2)	1	0	1	0	0	1	0	0	DPM MD	DPM VC	DA SEL	SBG SL	GD 2	GD 1	GD 0	CKOP

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND25 (Output control 1)	1	0	1	0	0	1	0	1	CEHSL	TOKSL	VIPSL	LCSSP2	OTM1	OTM0	LCSSTP	LCSOFF
COMMAND26 (Output control 2)	1	0	1	0	0	1	1	0	HFOFF	TBLOFF	KBL2	BL1	BL0	OTM2	ROTOFF	DOTOFF
COMMAND27 (Output control 3)	1	0	1	0	0	1	1	1	0	HFT2	HFT1	HFT0	TOKCB4	TOKCB3	TOKCB2	TOKCB1
COMMAND28 (Output control 4)	1	0	1	0	1	0	0	0	HPG9	HPS9	HPM29	HPM19	VPG8	VPS8	VPM28	VPM18
COMMAND29 (Output control 5)	1	0	1	0	1	0	0	1	0	SVH1	SVH0	SHH1	SHH0	0	0	MLCH
COMMAND2A (Display area control 1)	1	0	1	0	1	0	1	0	0	HINDIN	HID1	HID0	VID1	VID0	0	0
COMMAND30 (Vertical display start position: main 1)	1	0	1	1	0	0	0	0	VPM17	VPM16	VPM15	VPM14	VPM1	VPM12	VPM11	VPM10
COMMAND31 (Horizontal display start position: main 1)	1	0	1	1	0	0	1	HPM18	HPM17	HPM16	HPM15	HPM14	HPM13	HPM12	HPM11	HPM10
COMMAND32 (Vertical display start position: main 2)	1	0	1	1	0	1	0	0	VPM27	VPM26	VPM25	VPM24	VPM23	VPM22	VPM21	VPM20
COMMAND33 (Horizontal display start position: main 2)	1	0	1	1	0	1	1	HPM28	HPM27	HPM26	HPM25	HPM24	HPM23	HPM22	HPM21	HPM20
COMMAND34 (Vertical display start positions: sub)	1	0	1	1	1	0	0	0	VPS7	VPS6	VPS5	VPS4	VPS3	VPS2	VPS1	VPS0
COMMAND35 (Horizontal display start position: sub)	1	0	1	1	1	0	1	HPS8	HPS7	HPS6	HPS5	HPS4	HPS3	HPS2	HPS1	HPS0
COMMAND36 (Vertical display start positions: screen)	1	0	1	1	1	1	0	0	VPG7	VPG6	VPG5	VPG4	VPG3	VPG2	VPG1	VPG0
COMMAND37 (Horizontal display start position: screen)	1	0	1	1	1	1	1	HPG8	HPG7	HPG6	HPG5	HPG4	HPG3	HPG2	HPG1	HPG0

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND40 (Character size control)	1	1	0	0	0	0	0	0	0	0	0	0	SZV1	SZV0	SZH1	SZH0
COMMAND41 main 1 (Character size control: line setting U)	1	1	0	0	0	0	0	1	LSZ 7	LSZ 6	LSZ 5	LSZ 4	LSZ 3	LSZ 2	LSZ 1	LSZ 0
COMMAND42 main 1 (Character size control: line setting D)	1	1	0	0	0	0	1	0	LSZ 15	LSZ 14	LSZ 13	LSZ 12	LSZ 11	LSZ 10	LSZ 9	LSZ 8
COMMAND43 main 1 (Character size control: line setting D2)	1	1	0	0	0	0	1	1	0	0	0	0	0	0	LSZ 17	LSZ 16
COMMAND44 main 2 (Character size control: line setting U)	1	1	0	0	0	1	0	0	LSZ 7	LSZ 6	LSZ 5	LSZ 4	LSZ 3	LSZ 2	LSZ 1	LSZ 0
COMMAND45 main 2 (Character size control: line setting D)	1	1	0	0	0	1	0	1	LSZ 15	LSZ 14	LSZ 13	LSZ 12	LSZ 11	LSZ 10	LSZ 9	LSZ 8
COMMAND46 main 2 (Character size control: line setting D2)	1	1	0	0	0	1	1	0	0	0	0	0	0	0	LSZ 17	LSZ 16
COMMAND50 (BOX control U)	1	1	0	1	0	0	0	0	BXL W1	BXL W0	BXU CT1	BXU CT0	BXU C3	BXU C2	BXU C1	BXU C0
COMMAND51 (BOX control D)	1	1	0	1	0	0	0	1	BXR W1	BXR W0	BXD CT1	BXD CT0	BXD C3	BXD C2	BXD C1	BXD C0
COMMAND52 main 1 (BOX control: line setting U)	1	1	0	1	0	0	1	0	LBX 7	LBX 6	LBX 5	LBX 4	LBX 3	LBX 2	LBX 1	LBX 0
COMMAND53 main 1 (BOX control: line setting D)	1	1	0	1	0	0	1	1	LBX 15	LBX 14	LBX 13	LBX 12	LBX 11	LBX 10	LBX 9	LBX 8
COMMAND54 main 1 (BOX control: line setting D2)	1	1	0	1	0	1	0	0	0	0	0	0	0	0	LBX 17	LBX 16
COMMAND55 main 2 (BOX control: line setting U)	1	1	0	1	0	1	0	1	LBX 7	LBX 6	LBX 5	LBX 4	LBX 3	LBX 2	LBX 1	LBX 0
COMMAND56 main 2 (BOX control: line setting D)	1	1	0	1	0	1	1	0	LBX 15	LBX 14	LBX 13	LBX 12	LBX 11	LBX 10	LBX 9	LBX 8
COMMAND57 main 2 (BOX control: line setting D2)	1	1	0	1	0	1	1	1	0	0	0	0	0	0	LBX 17	LBX 16

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND58 (Line spacing control 1)	1	1	0	1	1	0	0	0	0	GYBCK	GS1	GS0	GY3	GY2	GY1	GY0
COMMAND59 (Line spacing control 2)	1	1	0	1	1	0	0	1	BXDW	BXUW	GYHSL	BXHSL	FCHSL	BXC3	BXC2	BXC1
COMMAND5A main 1 (Line spacing control: line setting U)	1	1	0	1	1	0	1	0	LGY7	LGY6	LGY5	LGY4	LGY3	LGY2	LGY1	LGY0
COMMAND5B main 1 (Line spacing control: line setting U)	1	1	0	1	1	0	1	1	LGY15	LGY14	LGY13	LGY12	LGY11	LGY10	LGY9	LGY8
COMMAND5C main 1 (Line spacing control: line setting D2)	1	1	0	1	1	1	0	0	0	0	0	0	0	0	LGY17	LGY16
COMMAND5D main 2 (Line spacing control: line setting U)	1	1	0	1	1	1	0	1	LGY7	LGY6	LGY5	LGY4	LGY3	LGY2	LGY1	LGY0
COMMAND5E main 2 (Line spacing control: line setting D)	1	1	0	1	1	1	1	0	LGY15	LGY14	LGY13	LGY12	LGY11	LGY10	LGY9	LGY8
COMMAND5F main 2 (Line spacing control: line setting D2)	1	1	0	1	1	1	1	1	0	0	0	0	0	0	LGY17	LGY16
COMMAND60 (Border control)	1	1	1	0	0	0	0	0	BLK	BLK	EGCT1	EGCT0	EGC3	EGC2	EGC1	EGC0
COMMAND61 main 1 (Border control: line setting U)	1	1	1	0	0	0	0	1	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
COMMAND62 main 1 (Border control: line setting D)	1	1	1	0	0	0	1	0	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
COMMAND63 main 1 (Border control: line setting D2)	1	1	1	0	0	0	1	1	0	0	0	0	0	0	LFC17	LFC16
COMMAND64 main 2 (Border control: line setting U)	1	1	1	0	0	1	0	0	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
COMMAND65 main 2 (Border control: line setting D)	1	1	1	0	0	1	0	1	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
COMMAND66 main 2 (Border control: line setting D2)	1	1	1	0	0	1	1	0	0	0	0	0	0	0	LFC17	LFC16
COMMAND67 (PLL control 1)	1	1	1	0	0	1	1	1	EVOOFF	LCOFF	ECKOFF	VCOOFF	VCS1	VCS0	CKSL1	CKSL0
COMMAND68 (PLL control 2)	1	1	1	0	1	0	0	0	0	0	0	DIV12	DIV11	DIV10	DIV9	DIV8
COMMAND69 (PLL control 3)	1	1	1	0	1	0	0	1	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
COMMAND6A (PLL control 5)	1	1	1	0	1	0	1	0	0	HDSL	DZ1	DZ0	HRSL	DID2	DID1	DID0
COMMAND6C0 (Write address) Color table	1	1	1	0	1	1	0	0	0	0	CTN1	CTN0	CTA3	CTA2	CTA1	CTA0
COMMAND6C1 (Data write) Color table	1	1	1	0	1	1	1	RM3[1][2]	0TG3	0TG2	HFTTG1	TOKTG0	TB3TR3	TB2TR2	TB1TR1	TB0TR0

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND700 (character ram1) writeaddress	1	1	1	1	0	0	0	0	FAD 1	FAD 0	FRN 1	FRN 0	FVA 3	FVA 2	FVA 1	FVA 0
COMMAND701 (character ram2) write	1	1	1	1	0	0	1	RM3[1] [2]	D15 D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0
COMMAND710 (WVGA ROM)	1	1	1	1	0	1	0	0	0	0	CKO S1	CKO S0	WFC MD	WRA M2	WRA M1	WRA M0
COMMAND711 (PLL control 6)	1	1	1	1	0	1	0	1	RSTB	0	VCRS	VCRS 1	CP 0	0 X2	CP I11	CP I0
COMMAND712 (PLL control 7)	1	1	1	1	0	1	1	0	0	STB CP	RES CP	SCP CP	DIV ECP	GAN 2	GAN 1	GAN 0

1 COMMAND00 (Main screen 1: horizontal write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 1 memory horizontal write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 0	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	V14 [MSB]	0	Main screen 1 memory line address (0 to 11, hexadecimal) 15 lines: 0E (hexadecimal) 18 lines: 11 (hexadecimal)	COM24-2: Line number specification
		1		
3	V13	0		
		1		
2	V12	0		
		1		
1	V11	0		
		1		
0	V10 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

2 COMMAND01 (Main screen 1: vertical write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 1 memory vertical write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 1	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	H15 [MSB]	0	Main screen 1 memory character position address (0 to 21, hexadecimal) 30 characters: 1D (hexadecimal) 33 characters: 20 (hexadecimal) 34 characters: 21 (hexadecimal)	COM23-2: Character number specification
		1		
4	H14	0		
		1		
3	H13	0		
		1		
2	H12	0		
		1		
1	H11	0		
		1		
0	H10 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

3 COMMAND02 (Main screen 2: horizontal write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 2 memory horizontal write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 2	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	V24 [MSB]	0	Main screen 2 memory line address (0 to 0E, hexadecimal) 15 lines: 0E (hexadecimal) 18 lines: 11 (hexadecimal)	COM24-2: Line number specification
		1		
3	V23	0		
		1		
2	V22	0		
		1		
1	V21	0		
		1		
0	V20 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

4 COMMAND03 (Main screen 2: vertical write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 2 memory vertical write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 3	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	H25 [MSB]	0	Main screen 2 memory character position address (0 to 21, hexadecimal) 30 characters: 1D (hexadecimal) 33 characters: 20 (hexadecimal) 34 characters: 21 (hexadecimal)	COM23-3: Character number specification
		1		
4	H24	0		
		1		
3	H23	0		
		1		
2	H22	0		
		1		
1	H21	0		
		1		
0	H20 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

5 COMMAND04 (Subscreen write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Subscreen write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	1	Sub-identification code: 4	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	SV1	0	Subscreen memory line address 0 to 3 (hexadecimal) 4 lines (maximum)	COM29-2: Line number specification
		1		
6	SV0	0		
		1		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	SH1	0	Subscreen memory character position address 0 to 3 (hexadecimal) 4 characters (maximum)	COM29-2: Character number specification
		1		
0	SH0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

6 COMMAND10 (Main screen 1 display character data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 1 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	0		
5	-	0		
4	-	1		
3	-	0	Sub-identification code: 0	
2	-	0		
1	RM2	0	RM2 RM1 Mode 0 0 [1][2][3][4][5] End 0 1 [1][2][3][4][5] Continuous 1 0 [3][4][5] Continuous 1 1 [2][3][4][5] Continuous	Continuous write mode selection
		1		
0	RM1	0		
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	HFT1	0	HFT1 HFT0 0 0 None 0 1 Character only 1 0 Character background only 1 1 Character+Character background	Halftone specification Graphic is processed as a character. COM59-2
		1		
6	HFT0	0		
		1		
5	at	0	Blinking off	Blinking specification
		1	Blinking on	
4	BXS	0	Raised	Box specification: raised/recessed
		1	Recessed	
3	BXL	0	None	Box specification: left side
		1	Box displayed	
2	BXR	0	None	Box specification: right side
		1	Box displayed	
1	BXU	0	None	Box specification: upper
		1	Box displayed	
0	BXD	0	None	Box specification: down
		1	Box displayed	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	CB3 [MSB]	0	Character background color specification 0000 to 1111, or 0 to F (hexadecimal)	Character background color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
6	CB2	0		
		1		
5	CB1	0		
		1		
4	CB0 [LSB]	0		
		1		
3	CC3 [MSB]	0	Character color specification 0000 to 1111, or 0 to F (hexadecimal)	Character color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
2	CC2	0		
		1		
1	CC1	0		
		1		
0	CC0 [LSB]	0		
		1		

(4) Second byte-[3]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	CTB1	0	CTB1 CTB0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Color table selection
		1		
5	CTB0	0		
		1		
4	I/E	0	Character RAM (internal)	ROM selection
		1	External ROM	
3	M/G1	0	MG1 MG0 0 0 Character 0 1 Graphic 1(CB, CC invalid) 1 0 Graphic 2 CTB address shown with CB → Chantged to CTB address shown with CC 1 1 Graphic 3 CTBNo of address shown with CB → Changed to CTBNo shown with CC1, CC0	Character/graphic specification
		1		
2	M/G0	0		
		1		
		1		
1	ROM1	0	ROM1 ROM0 0 0 ROM area number 1 0 1 ROM area number 2 1 0 ROM area number 3 1 1 ROM area number 4	ROM area selection
		1		
0	ROM0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

(5) Second byte-[4]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	C13 [MSB]	0		Character code specification
		1		
4	C12	0		
		1		
3	C11	0		
		1		
2	C10	0		
		1		
1	C9	0		
		1		
0	C8	0		
		1		

(6) Second byte-[5]

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code External ROM: 16384 characters 0000 to 3FFF (hexadecimal) 0 to 16383 Character RAM (internal): QVGA mode: 0 to 3, hexadecimal, 4 characters WVGA mode: 0 hexadecimal, 1 character * Transparent character specification I/E = 0 (Internal character RAM) M/G10 = 00 (Character) Code = FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

7 COMMAND11 (Main screen 2 display character data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 1 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	0		
5	-	0		
4	-	1		
3	-	0	Sub-identification code: 1	
2	-	0		
1	RM2	0	RM2 RM1 Mode 0 0 [1][2][3][4][5] End 0 1 [1][2][3][4][5] Continuous 1 0 [3][4][5] Continuous 1 1 [2][3][4][5] Continuous	Continuous write mode selection
		1		
0	RM1	0		
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	HFT1	0	HFT1 HFT0 0 0 None 0 1 Character only 1 0 Character background only 1 1 Character+Character background	Halftone specification Graphic is processed as a character. COM59-2
		1		
6	HFT0	0		
		1		
5	at	0	Blinking off	Blinking specification
		1	Blinking on	
4	BXS	0	Raised	Box specification: raised/recessed
		1	Recessed	
3	BXL	0	None	Box specification: left side
		1	Box displayed	
2	BXR	0	None	Box specification: right side
		1	Box displayed	
1	BXU	0	None	Box specification: upper
		1	Box displayed	
0	BXD	0	None	Box specification: down
		1	Box displayed	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	CB3 [MSB]	0	Character background color specification 0000 to 1111, or 0 to F (hexadecimal)	Character background color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
6	CB2	0		
		1		
5	CB1	0		
		1		
4	CB0 [LSB]	0		
		1		
3	CC3 [MSB]	0	Character color specification 0000 to 1111, or 0 to F (hexadecimal)	Character color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
2	CC2	0		
		1		
1	CC1	0		
		1		
0	CC0 [LSB]	0		
		1		

(4) Second byte-[3]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	CTB1	0	CTB1 CTB0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Color table selection
		1		
5	CTB0	0		
		1		
4	I/E	0	Character RAM (internal)	ROM selection
		1	External ROM	
3	M/G1	0	MG1 MG0 0 0 Character 0 1 Graphic 1 (CB, CC invalid) 1 0 Graphic 2 CTB address shown with CB → Changed to CTB address shown with CC. 1 1 Graphic 3 CTBNo of address shown with CB. → Changed to CTBNo shown with CC1, CC0.	Character/graphic specification
		1		
2	M/G0	0		
		1		
		1		
1	ROM1	0	ROM1 ROM0 0 0 ROM area number 1 0 1 ROM area number 2 1 0 ROM area number 3 1 1 ROM area number 4	ROM area selection
		1		
0	ROM0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

(5) Second byte-[4]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	C13 [MSB]	0		Character code specification
		1		
4	C12	0		
		1		
3	C11	0		
		1		
2	C10	0		
		1		
1	C9	0		
		1		
0	C8	0		
		1		

(6) Second byte-[5]

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code External ROM: 16384 characters 0000 to 3FFF (hexadecimal) 0 to 16383 Character RAM (internal): QVGA mode: 0 to 3, hexadecimal, 4 characters WVGA mode: 0 hexadecimal, 1 character * Transparent character specification I/E = 0 (Internal character RAM) M/G10 = 00 (Character) Code = FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

12 COMMAND12 (Subscreen display character data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 1 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	0		
5	-	0		
4	-	1		
3	-	1	Sub-identification code 2	
2	-	0		
1	RM2	0	RM2 RM1 Mode 0 0 [1][2][3][4][5] End 0 1 [1][2][3][4][5] Continuous 1 0 [3][4][5] Continuous 1 1 [2][3][4][5] Continuous	Continuous write mode selection
		1		
0	RM1	0		
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	-	0		
0	-	0		

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	-	0		
0	-	0		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(4) Second byte-[3]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	CTB1	0	CTB1 CTB0	Color table selection
		1	0 0 Color table number 1	
5	CTB0	0	0 1 Color table number 2	
		1	1 0 Color table number 3	
			1 1 Color table number 4	
4	I/E	0	Character RAM (internal)	ROM selection
		1	External ROM	
3	M/G1	0	MG1 MG0	Graphic only
		1	0 0 Character (only when transparent character is specified.)	
2	M/G0	0	0 1 Graphic 1 only	
		1		
		1		
1	-	0		
0	-	0		

(5) Second byte-[4]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	C13 [MSB]	0		Character code specification
		1		
4	C12	0		
		1		
3	C11	0		
		1		
2	C10	0		
		1		
1	C9	0		
		1		
0	C8	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

(6) Second byte-[5]

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code External ROM: 16384 characters 0000 to 3FFF (hexadecimal) 0 to 16383 Character RAM (internal): QVGA mode: 0 to 3, hexadecimal, 4 characters WVGA mode: 0 hexadecimal, 1 character * Transparent character specification I/E = 0 (Internal character RAM) M/G10 = 00 (Character) Code = FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

9 COMMAND20 (System control setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code System control settings	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Sub-identification code 0	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	TST MD2	0	Normal operation	Do not use test mode. This bit must always be set to 0.
		1	Test mode 2	
6	TST MD1	0	Normal operation	Do not use test mode. This bit must always be set to 0.
		1	Test mode 1	
5	SYS RST	0		The registers are reset when the $\overline{CS}$ pin is low. The reset state is cleared when the $\overline{CS}$ pin goes high.
		1	Reset all registers (All bits set to 0.)	
4	FRM ERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase FontRAM (Sets all values to 00.)	
3	CT ERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase the color table. (Sets all values to 00.)	
2	SRM ERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase sub-RAM. (Sets all values to 00.) Wallpaper	
1	MRM ER2	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase main RAM. (Sets all values to 00.) Main screen	
0	MRM ER1	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase main RAM. (Sets all values to 00.) Main screen	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

10 COMMAND21 (Display control setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Display control	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 1 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BK12	0	BK12 BK02 Blinking period	Blinking period main 2 Specified for screen units.
		1	0 0 1/16	
6	BK02	0	0 1 1/32	
		1	1 0 1/64	
5	BK11	0	BK11 BK01 Blinking period	Blinking period main 1 Specified for screen units.
		1	0 0 1/16	
4	BK01	0	0 1 1/32	
		1	1 0 1/64	
3	DSP BG	0	Display off	Screen background color
		1	Display on	
2	DSP GS	0	Display off	Subscreen (wallpaper)
		1	Display on	
1	DSP GM2	0	Display off	Main screen 2
		1	Display on	
0	DSP GM1	0	Display off	Main screen 1
		1	Display on	

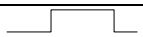
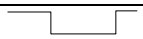
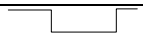
*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

11 COMMAND22 (I/O polarity control 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code I/O polarity control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 2 identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	BLOP	0	BLK output: positive polarity 	BLK output polarity selection
		1	BLK output: negative polarity 	
5	BLO2	0	BLO210 BLK output 0 0 0 Normal character.+charcter background+graphic 0 0 1 Character only 0 1 0 Character background only 0 1 1 Graphic only 1 0 0 Character+character background only 1 0 1 Character+graphic only 1 1 0 Character background+graphic only	BLK output control Character, character background, and graphic output control. Border specification is enabled when character background output is selected.
4	BLO1	0		
		1		
3	BLO0	0		
		1		
2	CKP	0	Clock input: positive polarity	Clock input polarity selection
		1	Clock input: negative polarity	
1	VIP	0	VSYNC input: negative polarity 	VSYNC input polarity selection
		1	VSYNC input: positive polarity 	
0	HIP	0	HSYNC input: negative polarity 	HSYNC input polarity selection
		1	HSYNC input: positive polarity 	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

12 COMMAND23 (Screen background color setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Screen background color	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 3 identification code	
2	-	0		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	DPM HC1	0	HC1 0 Characters 0 0 30 characters (1D, hexadecimal) 0 1 33 characters (20, hexadecimal) 1 0 34 characters (21, hexadecimal)	Main screen display area specification Horizontal direction
		1		
6	DPM HC0	0		
		1		
5	BGC T1	0	T1 T0 Color table setting 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Screen background color Color table setting
		1		
4	BGC T0	0		
		1		
3	BGC3	0	Screen background color 0000 to 1111 0 to F (hexadecimal)	Screen background color setting 1 of 16 colors may be selected.
		1		
2	BGC2	0		
		1		
1	BGC1	0		
		1		
0	BGC0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

13 COMMAND24 (I/O polarity control 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code I/O polarity control 2	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 4 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	DPM MD	0	QVGA mode (16×16 dots)	Display mode selection
		1	WVGA mode (24×32 dots)	
6	DPM VC	0	15 lines	Mmain screen display area specification Vertical
		1	18 lines	
5	D/A SEL	0	D/A on	D/A converter use/no-use selection
		1	D/A off	
4	SBG SL	0	Repeated display (wallpaper)	Subscreen display selection COM29-2: Display area specification
		1	Cursor display (sprite display) QVGA: Horizontal 4 characters×Vertical 4 lines (maximum) WVGA: Horizontal 2 characters×Vertical 2 lines (maximum)	
3	GD2	0	GD2 1 0 Screen display [upper⇔lower] 0 0 0 Main 1, Main 2, Wallpaper 0 0 1 Main 2, Main 1, Wallpaper 0 1 0 Wallpaper, Main 1, Main 2 0 1 1 Wallpaper, Main 2, Main 1 1 0 0 Main 1, Wallpaper, Main 2 1 0 1 Main 2, Wallpaper, Main 1	Screen display order selection
		1		
2	GD1	0		
		1		
1	GD0	0		
		1		
0	CKOP	0	Clock output: positive polarity	Clock output polarity selection
		1	Clock output: negative polarity	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

14 COMMAND25 (Output control 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 5 identification code	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	CEHSL	0	Normal operation	$\overline{CE}$ pin
		1	$\overline{CE}$ pin held fixed at the high level	
6	TOKSL	0	Normal mode	Transparent mode specification Specifis effective color table with COMN27-2.
		1	Transmissive mode The color specified at address 0 in color table No. 1 is displayed in the transmissive state.	
5	VIPSL	0	Falling edge detection	Selects the detection polarity for the VSYNC signal.
		1	Rising edge detection	
4	LCS OF2	0	LC oscillator: Normal operation (H sync)	LC oscillator STOP control When external clock is input.
		1	LC oscillator: STOP state (OFF) RSTLC also	
3	OTMD1	0	OTMD1 OTMD0 Output 0 0 Normal 0 1 Disabled 1 0 Disabled 1 1 High-impedance state	A0 to A19, CE, OE output selection
		1		
2	OTMD0	0		
		1		
1	LCS STP	0	LC oscillator: Normal operation (H sync.)	LC oscillator STOP control Enabled when display is off
		1	LC oscillator: Always STOP state	
0	LCS OFF	0	LC oscillator: Normal operation (H sync.)	LC oscillator STOP control When external clock is input.
		1	LC oscillator: STOP state (OFF) LCSTOP only	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

15 COMMAND26 (Output control 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 6 identification code	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HFT OFF	0	HFTOT output on	HFTOT output setting
		1	HFTOT output off=low	
6	BLK OFF	0	BLK output on	BLK output setting
		1	BLK output off=low	
5	BLD2	0	BLD2 1 0 BLK output delay 0 0 0 ±0 (analog) 0 0 1 +1 0 1 0 +2 0 1 1 -1 (digital) 1 0 0 -2	BLK output delay
		1		
4	BLD1	0		
		1		
3	BLD0	0		
		1		
2	OTM2	0	Output off=Low	CLKout output output control
		1	Normal output	
1	ROT OFF	0	External ROM address, OE, CE output on	External ROM address output setting
		1	External ROM address, OE, CE output off=low	
0	DOT OFF	0	Digital RGB output on	Digital RGB output setting
		1	Digital RGB output off=low	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

16 COMMAND27 (Output control 3 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	0	Extended command 7 identification code	
2	-	1		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	HFT OD2	0	HFTOD2 1 0 0 0 0 ±0 (analog) 0 0 1 +1 0 1 0 +2 0 1 1 -1 (digital) 1 0 0 -2	HFTOT output delay
5	HFT OD1	0		
		1		
4	HFT OD0	0		
		1		
3	TOK CB4	0	Address 0000: Normal color	Transparent color specification or specifiable color table No. 4 COM25-2 Enabled by setting TOKSL to 1.
		1	Address 0000: Transparent color	
2	TOK CB3	0	Address 0000: Normal color	Transparent color specification or specifiable color table No. 3 COM25-2 Enabled by setting TOKSL to 1.
		1	Address 0000: Transparent color	
1	TOK CB2	0	Address 0000: Norrmal color	Transparent color specification or specifiable color table No. 2 COM25-2 Enabled by setting TOKSL to 1.
		1	Address 0000: Transparent color	
0	TOK CB1	0	Address 0000: Normal color	Transparent color specification or specifiable color table No. 1 COM25-2 Enabled by setting TOKSL to 1.
		1	Address 0000: Transparent color	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

17 COMMAND28 (Output control 4 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	1	Extended command 8 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPG 9	0	Screen background color H position msb 0	H position screen background color msb
		1	Screen background color H position msb 1	
6	HPS 9	0	Subscreen H position msb 0	H position subscreen msb
		1	Subscreen H position msb 1	
5	HPM2 29	0	Main screen 2 H position msb 0	H position main screen 2 msb
		1	Main screen 2 H position msb 1	
4	HPM1 19	0	Main screen 1 H position msb 0	H position main screen 1 msb
		1	Main screen 1 H position msb 1	
3	VPG 8	0	Screen background V position msb 0	V position screen background color msb
		1	Screen background V position msb 1	
2	VPS 8	0	Subscreen V position msb 0	V position subscreen msb
		1	Subscreen V position msb 1	
1	VPM2 28	0	Main screen 2 V position msb 0	V position main screen 2 msb
		1	Main screen 2 V position msb 1	
0	VPM1 18	0	Main screen 1 V position msb 0	V position main screen 1 msb
		1	Main screen 1 V position msb 1	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

18 COMMAND29 (Output control 5 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	1	Extended command 9 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	SVH1	0	SVH1 SVH0 Display area QVGA WVGA 0 0 1 line - 0 1 2 line - 1 0 3 line 1 line 1 1 4 line 2 line	Subscreen vertical direction display range selection QVGA: 4 lines (maximum) WVGA: 2 lines (maximum)
		1		
5	SVH0	0		
		1		
4	SHH1	0	SHH1 SHH0 Display area QVGA WVGA 0 0 1 character - 0 1 2 characters - 1 0 3 characters 1 character 1 1 4 characters 2 characters	Subscreen horizontal direction display range selection QVGA: 4 characters (maximum) WVGA: 2 characters (maximum)
		1		
3	SHH0	0		
		1		
2	-	0		
1	-	0		
0	ML CHG	0	LSB first	3-wire control transfer direction selection
		1	MSB first	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

18 COMMAND2A (Display area control 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 2 identification code Output control 1	
6	-	0		
5	-	1		
4	-	0		
3	-	1	Extended command A identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	HIN DIN	0	Normal (LC oscillator control route)	HSYNC input selection Direct taking-in specification (1) must be used in modes other than LC oscillator.
		1	Direct taking in	
5	HI D1	0	HID1 HID0 delay 0 0 ±0 (initial) 0 1 +1 1 0 +2 1 1 +3	HSYNC taking in Enabled when HINDIN is set to 1.
		1		
4	HI D0	0		
		1		
3	VI D1	0	VID1 VID0 delay 0 0 ±0 (initial) 0 1 +1 1 0 +2 1 1 +3	VSYNC taking in
		1		
2	VI D0	0		
		1		
1	-	0		
0	-	0		

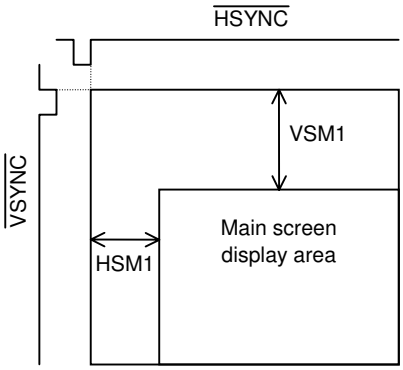
*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

25 COMMAND30 (Main screen 1: vertical display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Main screen 1 vertical display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	0	Extended command 0 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPM17	0	The vertical display start position, VSM 1, is given by: $VSM1=1H\times(\sum_{n=0}^{8}2^{n}VPM1n)$  	Main screen 1 The vertical display start position is specified by the 9 bits VPM18 to VPM10. The weight of the LSB is 1H. This setting applies in screen units.
		1		
6	VPM16	0		
		1		
5	VPM15	0		
		1		
4	VPM14	0		
		1		
3	VPM13	0		
		1		
2	VPM12	0		
		1		
1	VPM11	0		
		1		
0	VPM10 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

26 COMMAND31 (Main screen 1: horizontal display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Main screen: horizontal display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	0	Extended command 1 identification code	
2	-	0		
1	-	1		
0	HPM18	0		
		1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPM17	0	The horizontal display start position, HSM1, is given by:	Main screen 1 The horizontal display start position is specified by the 10 bits HPM19 to HPM10. The weight of the LSB is 1TC. This setting applies in screen units.
		1	$HSM1=1Tc\times(\sum_{n=0}^{9}2^{n}HPM1n)+\alpha$	
6	HPM16	0		
		1	α=45Tc(QVGA) 41Tc(WVGA)	
5	HPM15	0	Tc: The input clock frequency in operating mode.	
		1		
4	HPM14	0	Setting disable range	
		1	QVGA WVGA	
3	HPM13	0	Sub H 0 character 00HEX 00HEX	
		1	Sub H 1 character 00 to 05HEX 00 to 15HEX (00 to 0CHEX)	
2	HPM12	0	Sub H 2 characters 00 to 0DHEX 00 to 2CHEX (00 to 1CHEX)	
		1		
1	HPM11	0	Sub H 3 characters 00 to 15HEX	
		1	Sub H 4 characters 00 to 1DHEX	
0	HPM10 (LSB)	0	The values in parentheses apply when ROM access No. 2 and No. 3 are set.	
		1		

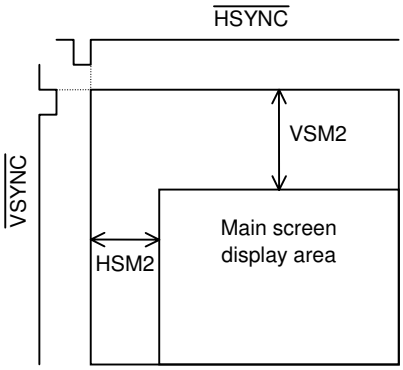
*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

27 COMMAND32 (Main screen 2: vertical display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Main screen 2 vertical display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	0	Extended command 2 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPM27	0	The vertical display start position, VSM2, is given by: $VSM2=1H\times(\sum_{n=0}^{8}2^{n}VPM2n)$  	Main screen 2 The vertical display start position is specified by the 9 bits VPM28 to VPM20. The weight of the LSB is 1H. This setting applies in screen units.
		1		
6	VPM26	0		
		1		
5	VPM25	0		
		1		
4	VPM24	0		
		1		
3	VPM23	0		
		1		
2	VPM22	0		
		1		
1	VPM21	0		
		1		
0	VPM20 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

28 COMMAND33 (Main screen 2: horizontal display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Main screen: horizontal display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	0	Extended command 3 identification code	
2	-	1		
1	-	1		
0	HPM28	0		
		1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPM27	0	The horizontal display start position, HSM2, is given by: $HSM2=1Tc\times(\sum_{n=0}^{9}2^{n}HPM2n)+\alpha$ α=45Tc(QVGA) 41Tc(WVGA) Tc: The input clock frequency in operating mode. Setting disable range QVGA WVGA Sub H 0 character 00HEX 00HEX Sub H 1 character 00 to 05HEX 00 to 15HEX (00 to 0CHEX) Sub H 2 characters 00 to 0DHEX 00 to 2CHEX (00 to 1CHEX) Sub H 3 characters 00 to 15HEX Sub H 4 characters 00 to 1DHEX The values in parentheses apply when ROM access No. 2 and No. 3 are set.	Main screen 2 The horizontal display start position is specified by the 10 bits HPM29 to HPM20. The weight of the LSB is 1TC. This setting applies in screen units.
		1		
6	HPM26	0		
		1		
5	HPM25	0		
		1		
4	HPM24	0		
		1		
3	HPM23	0		
		1		
2	HPM22	0		
		1		
1	HPM21	0		
		1		
0	HPM20 (LSB)	0		
		1		

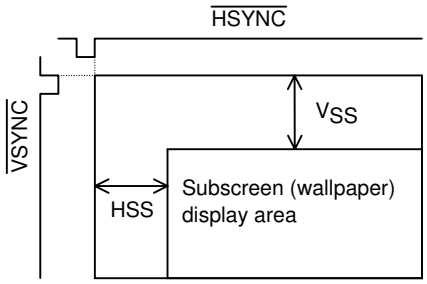
*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

29 COMMAND34 (Subscreen: vertical display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Subscreen: vertical display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	1	Extended command 4 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPS7	0	The vertical display start position, V_{SS}, is given by: $V_{SS}=1H\times(\sum_{n=0}^{8}2^{n}VPSn)$  	Subscreen (wallpaper) The vertical display start position is specified by the 9 bits VPS8 to VPS0. The weight of the LSB is 1H. This setting applies in screen units.
		1		
6	VPS6	0		
		1		
5	VPS5	0		
		1		
4	VPS4	0		
		1		
3	VPS3	0		
		1		
2	VPS2	0		
		1		
1	VPS1	0		
		1		
0	VPS0 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

30 COMMAND35 (Subscreen: horizontal display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Subscreen: horizontal display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	1	Extended command 5 identification code	
2	-	0		
1	-	1		
0	HPS8	0		
		1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPS7	0	The horizontal display start position, HSS, is given by: $HSS=1Tc\times(\sum_{n=0}^{9}2^{n}HPSn)+\alpha$ $\alpha=15Tc$ Tc: The input clock frequency in operating mode. Setting disable range QVGA WVGA Sub H 1 character 00 to 13HEX 00 to 22HEX (00 to 1AHEX) Sub H 2 characters 00 to 1BHEX 00 to 3AHEX (00 to 2AHEX) Sub H 3 characters 00 to 23HEX Sub H 4 characters 00 to 2BHEX The values in parentheses apply when ROM access No. 2 and No. 3 are set.	Subscreen (wallpaper) The horizontal display start position is specified by the 9 bits HPS9 to HPS0. The weight of the LSB is 1TC. This setting applies in screen units.
		1		
6	HPS6	0		
		1		
5	HPS5	0		
		1		
4	HPS4	0		
		1		
3	HPS3	0		
		1		
2	HPS2	0		
		1		
1	HPS1	0		
		1		
0	HPS0 (LSB)	0		
		1		

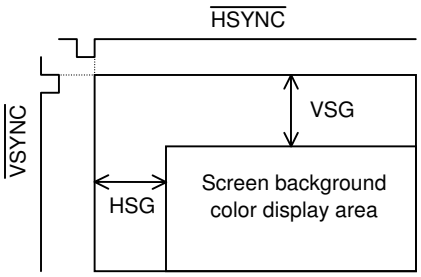
*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

31 COMMAND36 (Screen background color: vertical display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Screen background color: vertical display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	1	Extended command 6 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPG7	0	The vertical display start position, VSG, is given by: $VSG=1H\times(\sum_{n=0}^{8}2^{n}VPGn)$  	Screen background color The vertical display start position is specified by the 8 bits VPG8 to VPG0. The weight of the LSB is 1H. This setting applies in screen units.
		1		
6	VPG6	0		
		1		
5	VPG5	0		
		1		
4	VPG4	0		
		1		
3	VPG3	0		
		1		
2	VPG2	0		
		1		
1	VPG1	0		
		1		
0	VPG0 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

32 COMMAND37 (Screen background color: horizontal display start position setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 3 identification code Screen background color: horizontal display start position setting	
6	-	0		
5	-	1		
4	-	1		
3	-	1	Extended command 7 identification code	
2	-	1		
1	-	1		
0	HPG8	0		
		1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPG7	0	The horizontal display start position, HSG, is given by: $HSG=1Tc\times(\sum_{n=0}^{9}2^{n}HPGn)$ Tc: The input clock frequency in operating mode.	Screen background color The horizontal display start position is specified by the 10 bits HPG9 to HPG0. The weight of the LSB is 1TC. This setting applies in screen units.
		1		
6	HPG6	0		
		1		
5	HPG5	0		
		1		
4	HPG4	0		
		1		
3	HPG3	0		
		1		
2	HPG2	0		
		1		
1	HPG1	0		
		1		
0	HPG0 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

33 COMMAND40 (Character size control setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size control settings	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 0 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	SZV1	0	SZV1 SZV0 Character size 0 0 1× 0 1 2× 1 0 3× 1 1 4×	Specifies the character size in the vertical direction. This setting applies in line units.
		1		
2	SZV0	0		
		1		
1	SZH1	0	SZH1 SZH0 Character size 0 0 1× 0 1 2× 1 0 3× 1 1 4×	Specifies the character size in the horizontal direction. This setting applies in line units.
		1		
0	SZH0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

34 COMMAND41 (Character size line U control main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line U control main 1	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 1 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ7	0	Do not set for line 8.	Character size line setting control Upper lines
		1	Set for line 8.	
6	LSZ6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LSZ5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LSZ4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LSZ3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LSZ2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LSZ1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LSZ0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

35 COMMAND42 (Character size line D control main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line D control main 1	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 2 identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ15	0	Do not set for line 16.	Character size line setting control Lower lines
		1	Set for line 16.	
6	LSZ14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LSZ13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LSZ12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LSZ11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LSZ10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LSZ9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LSZ8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

36 COMMAND43 (Character size line D2 control main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line D2 control main 1	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 3 identification code	
2	-	0		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LSZ17	0	Do not set for line 18.	Character size line setting control Lower lines 2
		1	Set for line 18.	
0	LSZ16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

37 COMMAND44 (Character size line U control main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line U control main 2	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 4 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ7	0	Do not set for line 8.	Character size line setting control Upper lines
		1	Set for line 8.	
6	LSZ6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LSZ5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LSZ4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LSZ3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LSZ2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LSZ1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LSZ0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

38 COMMAND45 (Character size line D control main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line D control main 2	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 5 identification code	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ15	0	Do not set for line 16.	Character size line setting control Lower lines
		1	Set for line 16.	
6	LSZ14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LSZ13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LSZ12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LSZ11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LSZ10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LSZ9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LSZ8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

39 COMMAND46 (Character size line D control main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 4 identification code Character size line D control main 2	
6	-	1		
5	-	0		
4	-	0		
3	-	0	Extended command 6 identification code	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LSZ17	0	Do not set for line 18.	Character size line setting control Lower lines 2
		1	Set for line 18.	
0	LSZ16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

46 COMMAND50 (Box control: U setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control U settings	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 0 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BXL W1	0	W1 W0 0 0 1 dot 0 1 2 dots 1 0 3 dots 1 1 4 dots	Box display: left side Dot width. This setting applies in line units. It does not depend on the character size.
		1		
6	BXL W0	0		
		1		
5	BXU CT1	0	BXUCT1 0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Box display: upper side Color table specification This setting applies in line units.
		1		
4	BXU CT0	0		
		1		
3	BXU C3	0	Box display: upper side color specification 0000 to 1111 0 to F (hexadecimal)	Box display: upper side Color specification This setting applies in line units.
		1		
2	BXU C2	0		
		1		
1	BXU C1	0		
		1		
0	BXU C0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

47 COMMAND51 (Box control: D setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control D settings	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 1 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BXR W1	0	W1 W0	Box display: right side Dot width. This setting applies in line units. It does not depend on the character size.
		1	0 0 1 dot 0 1 2 dots 1 0 3 dots 1 1 4 dots	
6	BXR W0	0		
		1		
5	BXD CT1	0	BXDCT1 0	Box display: lower side Color table specification This setting applies in line units.
		1	0 0 Color table number 1 0 1 Color table number 1 1 0 Color table number 3 1 1 Color table number 4	
4	BXD CT0	0		
		1		
3	BXD C3	0	Box display: lower side color specification 0000 to 1111 0 to F (hexadecimal)	Box display: lower side Color specification This setting applies in line units.
		1		
2	BXD C2	0		
		1		
1	BXD C1	0		
		1		
0	BXD C0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

48 COMMAND52 (Box control: U line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control U line main 1 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 2 identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX7	0	Do not set for line 8.	Box control line setting control Upper lines
		1	Set for line 8.	
6	LBX6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LBX5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LBX4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LBX3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LBX2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LBX1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LBX0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

49 COMMAND53 (Box control: D line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control D line main 1 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 3 identification code	
2	-	0		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX15	0	Do not set for line 16.	Box control line setting control Lower lines
		1	Set for line 16.	
6	LBX14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LBX13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LBX12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LBX11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LBX10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LBX9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LBX8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

50 COMMAND54 (Box control: D2 line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control D2 line main 1 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 4 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LBX17	0	Do not set for line 18.	Box control line setting control Lower lines
		1	Set for line 18.	
0	LBX16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

51 COMMAND55 (Box control: U line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control U line main 2 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 5 identification code	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX7	0	Do not set for line 8.	Box control line setting control Upper lines
		1	Set for line 8.	
6	LBX6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LBX5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LBX4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LBX3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LBX2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LBX1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LBX0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

52 COMMAND56 (Box control: D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control D line main 2 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 6 identification code	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX15	0	Do not set for line 16.	Box control line setting control Lower lines
		1	Set for line 16.	
6	LBX14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LBX13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LBX12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LBX11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LBX10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LBX9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LBX8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

53 COMMAND57 (Box control: D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Box control D2 line main 2 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	0	Extended command 7 identification code	
2	-	1		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LBX17	0	Do not set for line 18.	Box control line setting control Lower lines 2
		1	Set for line 18.	
0	LBX16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

54 COMMAND58 (Line spacing control 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Line spacing control 1 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command 8 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	0	0		
6	GYB CK	0	Line spacing basic clock: 1V	Line spacing basic unit (clock) setting
		1	Line spacing basic clock: Depending on the character size	
5	GS1	0	GS1 GS0 Character Graphic 0 0 Transparent Transparent 0 1 Transparent ±1 (char. bkg color) Transparent ±1 (CB specified color) 1 0 Char. bkg. color CB specified color 1 1 Transparent (Border enabled) Transparent	Line spacing mode setting This setting applies in line units
		1		
4	GS0	0		
		1		
3	GY3	0	GY3 2 1 0 Line spacing (×H) 0 0 0 0 0 0 0 0 1 -1 (upper) +1 (lower) 0 0 1 0 -1 +2 0 0 1 1 -1 +3 0 1 0 0 -1 +4 0 1 0 1 -1 +5 0 1 1 0 -1 +6 0 1 1 1 -1 +7 1 0 0 0 -1 +8 1 0 0 1 -1 +9 1 0 1 0 -1 +10 1 0 1 1 -1 +11 1 1 0 0 -1 +12 1 1 0 1 -1 +13 1 1 1 0 -1 +14 1 1 1 1 -1 +15	Line spacing dot number setting This setting applies in line units of 1H
		1		
2	GY2	0		
		1		
1	GY1	0		
		1		
0	GY0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

55 COMMAND59 (Line spacing control 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Line spacing control 2 setting	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command 9 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BXW D	0	Box display: lower side is 1 dot	Box display Lower side. This setting applies in line units. Depending on the character size
		1	Box display: lower side is 2 dots	
6	BXW U	0	Box display: upper side is 1 dot	Box display Upper side. This setting applies in line units. Depending on the character size
		1	Box display: upper side is 2 dots (Invalid when line spacing is specified.)	
5	GYHSL	0	Normal display	Line spacing area when halftone is specified This setting applies in line units. Transparent is supported except for 00.
		1	Line spacing area: halftone	
4	BXHSL	0	Normal display	Box area when halftone is specified This setting applies in line units
		1	Box area: halftone	
3	FCHSL	0	Depending on the character	Border area when halftone is specified This setting applies in line units
		1	Depending on the character background	
2	BXC3	0	Displayed in upper part of character lower line spacing	Box upper and lower display control 2 Valid when line spacing is specified. This setting applies in line units
		1	Displayed in lower part of character lower line spacing	
1	BXC2	0	Inside the character range (V1&V16 dots)	Box upper and lower display control 1 This setting applies in line units
		1	Outside the character range (line spacing area): Valid only when line spacing is specified.	
0	BXC1	0	Inside the character range	Box left and ight display control This setting applies in line units
		1	Outside the character range	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

56 COMMAND5A (Line spacing control: U line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting U main 1	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command A identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LGY7	0	Do not set for line 8.	Control the line spacing control line setting Upper lines
		1	Set for line 8.	
6	LGY6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LGY5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LGY4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LGY3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LGY2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LGY1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LGY0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

57 COMMAND5B (Line spacing control: D line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting D main 1	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command B identification code	
2	-	0		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LGY15	0	Do not set for line 16.	Control the line spacing control line setting Lower lines
		1	Set for line 16.	
6	LGY14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LGY13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LGY12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LGY11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LGY10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LGY9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LGY8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

58 COMMAND5C (Line spacing control: D line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting D main 1	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command C identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LGY17	0	Do not set for line 18.	Control the line spacing control line setting Lower lines 2
		1	Set for line 18.	
0	LGY16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

59 COMMAND5D (Line spacing control: U line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting U main 2	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command D identification code	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LGY7	0	Do not set for line 8.	Control the line spacing control line setting Upper lines
		1	Set for line 8.	
6	LGY6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LGY5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LGY4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LGY3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LGY2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LGY1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LGY0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

60 COMMAND5E (Line spacing control: D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting D main 2.	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command E identification code	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LGY15	0	Do not set for line 16.	Control the line spacing control line setting Lower lines
		1	Set for line 16.	
6	LGY14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LGY13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LGY12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LGY11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LGY10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LGY9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LGY8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

61 COMMAND5F (Line spacing control: D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 5 identification code Control the line spacing control line setting D main 2.	
6	-	1		
5	-	0		
4	-	1		
3	-	1	Extended command F identification code	
2	-	1		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LGY17	0	Do not set for line 18.	Control the line spacing control line setting Lower lines
		1	Set for line 18.	
0	LGY16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

62 COMMAND60 (Border control setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code	
6	-	1	Border control setting	
5	-	1		
4	-	0		
3	-	0	Extended command 0 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BLK1	0	BLK1 BLK0 Border mode specification	Border mode specification
		1	0 0 Normal display	This setting applies in line units.
6	BLK0	0	0 1 Border	
		1	1 0 Shadow 1 (lower side)	
			1 1 Shadow 2 (lower and right sides)	
5	EG CT1	0	EGCT1 0	Border display
		1	0 0 Color table number 1	Color table specification
4	EG CT0	0	0 1 Color table number 2	This setting applies in line units.
		1	1 0 Color table number 3	
			1 1 Color table number 4	
3	EG C3	0	Border display: color specification	Border display
		1	0000 to 1111	color specification
2	EG C2	0	0 to F (hexadecimal)	This setting applies in line units.
		1		
1	EG C1	0		
		1		
0	EG C0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

63 COMMAND61 (Border control U line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting U main 1 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 1 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC7	0	Do not set for line 8.	Border control line settings control main 1 Upper lines
		1	Set for line 8.	
6	LFC6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LFC5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LFC4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LFC3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LFC2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LFC1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LFC0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

64 COMMAND62 (Border control D line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting D main 1 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 2 identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC15	0	Do not set for line 16.	Border control line settings control main 1 Lower lines
		1	Set for line 16.	
6	LFC14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LFC13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LFC12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LFC11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LFC10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LFC9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LFC8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

65 COMMAND63 (Border control D line main 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting D main 1 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 3 identification code	
2	-	0		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LFC17	0	Do not set for line 18.	Border control line settings control main 1 Lower lines
		1	Set for line 18.	
0	LFC16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

66 COMMAND64 (Border control U line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting U main 2 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 4 identification code	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC7	0	Do not set for line 8.	Border control line settings control main 2 Upper lines
		1	Set for line 8.	
6	LFC6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LFC5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LFC4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LFC3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LFC2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LFC1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LFC0	0	Do not set for line 1.	
		1	Set for line 1.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

67 COMMAND65 (Border control D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting D main 2 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 5 identification code	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC15	0	Do not set for line 16.	Border control line settings control main 2 Lower lines
		1	Set for line 16.	
6	LFC14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LFC13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LFC12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LFC11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LFC10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LFC9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LFC8	0	Do not set for line 9.	
		1	Set for line 9.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

68 COMMAND66 (Border control D line main 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Border line setting D main 2 control	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 6 identification code	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	LFC17	0	Do not set for line 18.	Border control line settings control main 2 Lower lines
		1	Set for line 18.	
0	LFC16	0	Do not set for line 17.	
		1	Set for line 17.	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

69 COMMAND67 (PLL control 1 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code PLL control 1	
6	-	1		
5	-	1		
4	-	0		
3	-	0	Extended command 7 identification code	
2	-	1		
1	-	1		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	EVO OFF	0	External VCO on	Oscillator-related control Initial LC oscillation
		1	External VCO off	
6	LC OFF	0	LC oscillator on	
		1	LC oscillatior off	
5	ECK OFF	0	External clock on	
		1	External clock off	
4	VCO OFF	0	VCO oscillator on	
		1	VCO oscillator off	
3	VCO SL1	0	VCOSL1 0 0 0 Internal VCO 1/1 0 1 Internal VCO 1/2 1 0 Internal VCO 1/4 1 1 External VCO	VCO selection Clock selection required CKSL = 10
		1		
2	VCO SL0	0		
		1		
1	CKSL 1	0	CKSL1 0 0 0 LC 0 1 External clock 1 0 Internal VCO (PLL) or external VCO	Clock selection
		1		
0	CKSL 0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

70 COMMAND68 (PLL control 2 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code PLL control 2	
6	-	1		
5	-	1		
4	-	0		
3	-	1	Extended command 8 identification code	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	DIV 12	0		PLL-circuit frequency division ratio setting
		1		
3	DIV 11	0		
		1		
2	DIV 10	0		
		1		
1	DIV 9	0		
		1		
		1		
0	DIV 8	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

71 COMMAND69 (PLL control 3 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code PLL control 3	
6	-	1		
5	-	1		
4	-	0		
3	-	1	Extended command 9 identification code	
2	-	0		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	DIV 7	0	$N2=\sum_{n=0}^{12} 2^n DIVn$ N2: 48 to 8196 30 to 1FFF (hexadecimal) FVCO = fH×N2 VCO oscillation frequency Horizontal frequency input	PLL-circuit frequency division ratio setting Initial values: 27BHEX fH = 15.734kHz FVCO = 10MHz
		1		
6	DIV 6	0		
		1		
5	DIV 5	0		
		1		
4	DIV 4	0		
		1		
3	DIV 3	0		
		1		
2	DIV 2	0		
		1		
1	DIV 1	0		
		1		
0	DIV 0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

72 COMMAND6A (PLL control 5 setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code PLL control 5	
6	-	1		
5	-	1		
4	-	0		
3	-	1	Extended command A identification code	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	HD SEL	0	HD (AFC)	H sync signal switch at AFC Enabled when Com67-2 CKSL is set to 10.
		1	HIN (input)	
5	DZ1	0	DZ1 DZ0 0 0 DZA 0.0ns 0 1 DZB 0.5ns 1 0 DZC 2.5ns	Dead zone specification
		1		
4	DZ0	0		
		1		
3	HREF SL	0	HREF (sync)	HREF selection
		1	HREF (directly)	
2	DID 2	0	DID2 1 0 Frequency division ratio (N1) 0 0 0 1/1 0 0 1 1/2 0 1 0 1/3 0 1 1 1/4 1 0 0 1/6 FDOT = FVCO×N1 Dot clock VCO oscillation frequency	Dot clock frequency division ratio specification
		1		
1	DID 1	0		
		1		
0	DID 0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

73 COMMAND6C0 (Color table write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Color table write address setting	
6	-	1		
5	-	1		
4	-	0		
3	-	1	Sub-identifier code CO	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-			
6	-			
5	CTN1	0	CTN1 CTN0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Color table selection
		1		
4	CTN0	0		
		1		
3	CTA3 (MSB)	0	Color table address 0 to 15 0 to F (hexadecimal) 16 values	Address of the color tables
		1		
2	CTA2	0		
		1		
1	CTA1	0		
		1		
0	CTA0 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

74 COMMAND6C1 (Color table data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 6 identification code Color table write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	1		
5	-	1		
4	-	0		
3	-	1	Sub-identifier code C1	
2	-	1		
1	-	1		
0	RM3	0	RM3 Mode 0 [1][2] End 1 [1][2] Continuous	Continuous write mode selection
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	HFT	0	Halftone: off	
		1	Halftone: on (HFTOT output is high.)	
4	TOK	0	Color	
		1	Transparent (BLK output: low)	
3	TB3	0	Color table B output 0000 to 1111 0 to F (hexadecimal)	Color table setting B
		1		
2	TB2	0		
		1		
1	TB1	0		
		1		
0	TB0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	TG3	0	Color table G output 0000 to 1111 0 to F (hexadecimal)	Color table setting G
		1		
6	TG2	0		
		1		
5	TG1	0		
		1		
4	TG0	0		
		1		
3	TR3	0	Color table R output 0000 to 1111 0 to F (hexadecimal)	Color table setting R
		1		
2	TR2	0		
		1		
1	TR1	0		
		1		
0	TR0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

When transparent is selected, the BLK output is set to the low level. (Transparent state)
The RGB outputs are values from the color table.
The transparent specification is best for color table 1, address 0000.
Since the data is set to all zeros by a RAM clear operation,
the RGB output will be 000 (black) and the BLK output will be 1.
Transparent is specified by setting the TOK bit to 1. (The BLK output will go to the low level.)

75 COMMAND700 (Character RAM write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 7 identification code Character RAM write address setting	
6	-	1		
5	-	1		
4	-	1		
3	-	0	Sub-identifier code 000	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	FAD1	0	QVGA mode Character RAM address 0 to 3 0 to 3 (hexadecimal) WVGA mode PNo. 0 to 3 P1 to P4	Character RAM QVGA: address WVGA: PNo.
		1		
6	FAD0	0		
		1		
5	FRN1	0	ROM No.1 to 4 0 to 3 0 to 3 (hexadecimal) No.1 to No.4	Character RAM ROM No.
		1		
4	FRN0	0		
		1		
3	FVA3 (MSB)	0	Character RAM V dot addresses 0 to 15 0 to F (hexadecimal)	Character RAM V dot address
		1		
2	FVA2	0		
		1		
1	FVA1	0		
		1		
0	FVA0 (LSB)	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

76 COMMAND701 (Character RAM data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 7 identification code Character RAM data write address setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	1		
5	-	1		
4	-	1		
3	-	0	Sub-identifier code 001	
2	-	0		
1	-	1		
0	RM3	0	RM3 Mode	Continuous write mode selection
		1	0 [1][2] End 1 [1][2] Continuous	

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	D15	0	Character RAM write data D15 to D0	Character RAM write data
		1		
6	D14	0		
		1		
5	D13	0		
		1		
4	D12	0		
		1		
3	D11	0		
		1		
2	D10	0		
		1		
1	D9	0		
		1		
0	D8	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	D7	0		Character RAM write data
		1		
6	D6	0		
		1		
5	D5	0		
		1		
4	D4	0		
		1		
3	D3	0		
		1		
2	D2	0		
		1		
1	D1	0		
		1		
0	D0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

77 COMMAND710 (WVGA: ROM access setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 7 identification code WVGA ROM access setting	
6	-	1		
5	-	1		
4	-	1		
3	-	0	Sub-identifier code 0100	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7		0		
6		0		
5	CKOS1	0	CKOS1 0 0 0 CLK 0 1 PHASECP(HD1BFQ) 1 0 NCHCP 1 1 PCHCP	CLKout output selection
		1		
4	CKOS0	0		
		1		
3	WFCMD	0	No border	WVGA mode Specifies border display when ROM access mode is set to 011 or 100.
		1	Border (displayed for each upper and lower 1V)	
2	WRAM2	0	When WRAM210 DCLK=33.3MHz • No.1 3CLK = 90ns 000 Main 1 only (Main 2 display off) 001 Main 2 only (Main 1 display off) because box is displayed • No.2 2CLK 60ns Main 1 Main 2 010 Character Character 011 Graphic Character HPM1≤HPM2 * The character has no border. 100 Character Graphic HPM1≥HPM2 * The character has no border. • No.3 1CLK = 30ns 101 Equivalent to QVGA (external ROM only)	WVGA mode ROM access specification
		1		
1	WRAM1	0		
		1		
0	WRAM0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

78 COMMAND711 (PLL setting command 6)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 7 identification code PLL setting command 6	
6	-	1		
5	-	1		
4	-	1		
3	-	0	Sub-identifier code 0101	
2	-	1		
1	-	0		
0	-	1		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	RSETB	0	VCOR: Internal RSETB"H"	VCOR selection
		1	VCOR: External "L"	
6	-	0		
5	VCR S1	0	VCRS1 VCRS0 RSET0 1 2	Internal VCOR value setting Large resistance → low gain
		1	0 0 5.6K 1 1 0	
4	VCR S0	0	0 1 6.6K 1 0 0	
		1	1 0 7.6K 0 0 0	
			1 1 4.6K 1 1 1	
3	CPI X2	0	The following set current ×1	CP current value setting 2
		1	The following set current ×3	
2	-	0		
1	CPI S1	0	CPIS1 CPIS0 CPIS0 1 2	CP current value setting 1
		1	0 0 40μA 0 0 0	
0	CPI S0	0	0 1 44μA 1 0 0	
		1	1 0 52μA 0 1 0	
			1 1 60μA 0 0 1	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

79 COMMAND712 (PLL setting command 7)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 7 identification code Display character data write setting	
6	-	1		
5	-	1		
4	-	1		
3	-	0	Sub-identifier code 0110	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	STYB CP	0	Normal operation: STYB"H"	CP, VCO standby setting
		1	CP, VCO standby: PD0 = "Z"	
5	RESETBCP	0	Normal operation: RESETB"H"	PD reset setting
		1	PD reset: PD0 = "Z"	
4	SCP1 CP	0	CP enable: SCP1"H"	CP control
		1	CP disable	
3	DIV ENB	0	Normal operation: DIVENB"H"	Frequency divider control
		1	Frequency divider reset	
2	GAIN 2	0		VCO adjustment
		1		
1	GAIN 1	0		
		1		
0	GAIN 0	0		
		1		

GAIN			Fmin	Fmax	Gain[MHz]
2	1	0			
0	0	0	7	40	20/V
0	0	1	7	-20%	-22.5%
0	1	0	-20%	40	+2.5%
0	1	1	-20%	-20%	-20%
1	0	0	+20%	+10%	+8.75%
1	0	1	+20%	-10%	-13.75%
1	1	0	7	+10%	+11.25%
1	1	1	7	-10%	+11.25%

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Display Structure

The display screen consists of a 34-character×18-line grid (maximum).

- QVGA mode (16×16 dot characters)
  QVGA panel (480×234) 30-character×15-line
- WVGA mode (24×32 dot characters)
  WVGA panel (800×480) 33-character×15-line

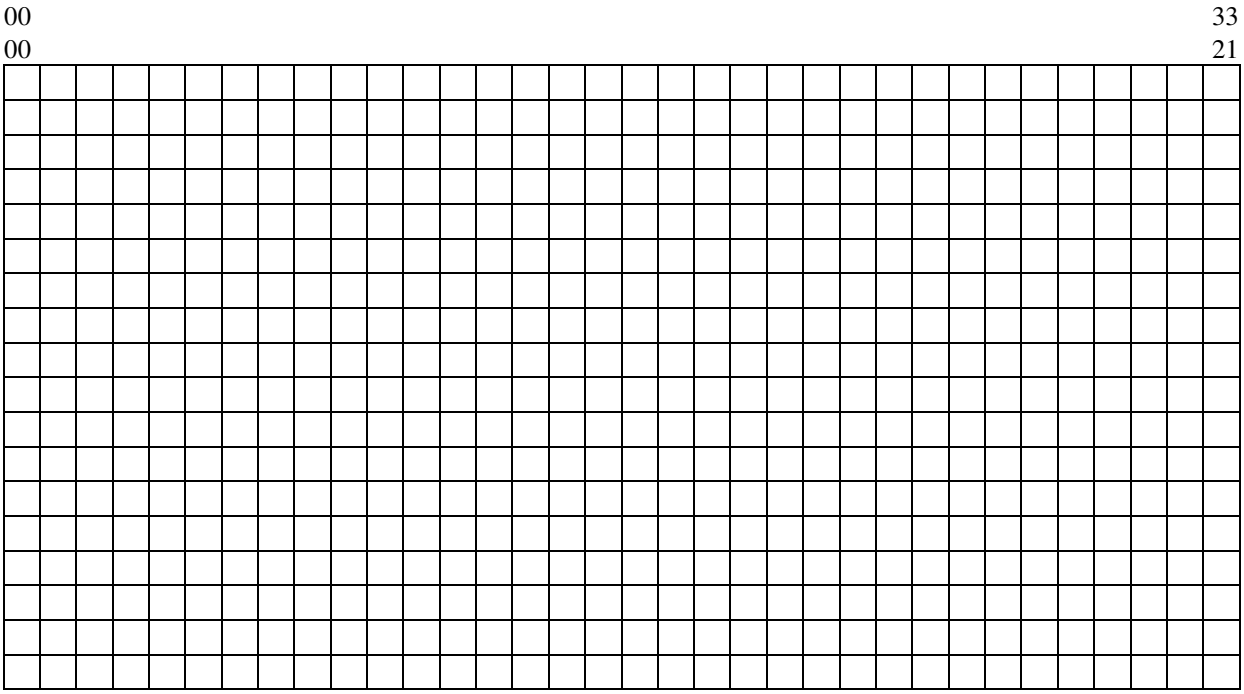
Up to a maximum of 612 characters can be displayed.

If the character size is increased, the number of characters that can be displayed will decrease to be fewer than 612 characters.

Display memory is addressed by specifying a line address (00 to 17 (hexadecimal) and a character position address (00 to 32 (hexadecimal)).

Display memory is addressed by specifying a line address (00 to 11 (hexadecimal) and a character position address (00 to 21 (hexadecimal)).

Display structure (Display memory address): 34 characters×18 lines (maximum)



Operational Description

1. Command transfer method

1.1 Overview

(1) Commands are transferred in 8-bit units, LSB first.
Always send a first byte and a second byte (16 bits).

(2) COMMAND10 (Main screen 1 RAM write)
COMMAND11 (Main screen 2 RAM write)
COMMAND12 (Subscreen write)
COMMNAD6C1 (Color table write)
COMMAND701 (Character RAM write) is locked in continuous write mode when a continuous mode is specified (RM2, 1 RM3). (Continuous mode is cleared by setting the CS pin high.)

1.2 Writing Data to VRAM

(1) Write start address specification
Write start address is set using:
COMMAND00, COMMAND01 (Main screen 1)
COMMAND02, COMMAND03 (Main screen 2)
COMMAND04 (Subscreen)
V4 to V0: Vertical direction; H5 to H0: Horizontal direction

(2) Data write
Continuous write mode differs depending on the write mode specification. (RM1, RM2)
1. Normal (RM2 = 0, RM1 = 0: initial state) *Continuous mode not used*
-- COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-5 command wait state --

2. Write continuous (RM2 = 0, RM1 = 1): Mode 2
COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-5

3. Write continuous (RM2 = 1, RM1 = 0): Mode 3
COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-5 10-2-3 10-2-4 10-2-5

4. Write continuous (RM2 = 1, RM1 = 1): Mode 4
COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-5 10-2-2 10-2-3 10-2-4 10-2-5

*: In modes 2, 3, and 4, the IC remains locked in continuous write mode until the $\overline{CS}$ pin is set high.

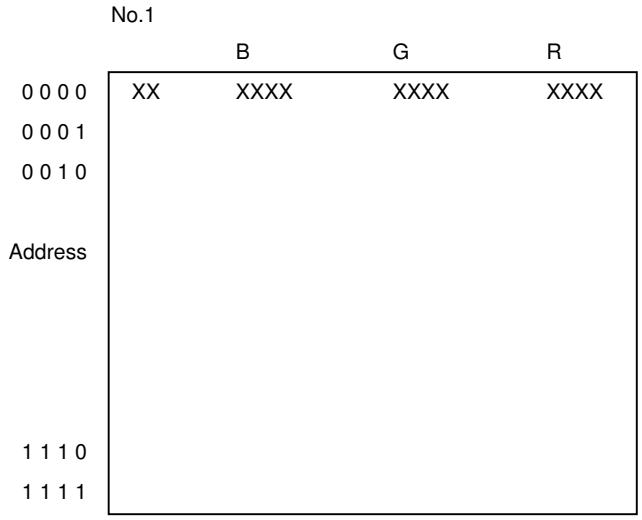
- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

1.3 Color Table write

(1) Write start address specification

Use command 6C0 to set the color table write start address.

CTN1 to CTN0: Color table specification (No.1 to No.4), CTA3 to CTA0: Address specification



(2) Data write

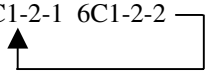
Continuous write mode differs depending on the write mode specification. (RM3)

1. Normal (RM3 = 0: initial state) *Continuous mode not used*

---COM6C1-1 6C1-2-1 6C1-2-2 command wait state ---

2. Write continuous (RM3 = 1) mode

COM6C1-1 6C1-2-1 6C1-2-2



*: In mode 2, the IC remains locked in continuous write mode until the $\overline{CS}$ pin is set high.

- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

1.4 Character RAM write

(1) Write start address specification

Use COMMAND700 to specify the character RAM write start address.

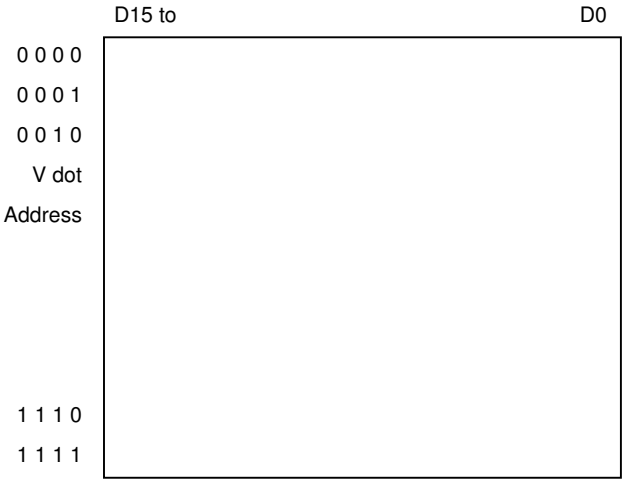
FAD1to FAD0: Character RAM address P-No specification

QVGA: 0 to 3, hexadecimal, (4 characters)

WVGA: 1 character only 0 to 3 (hexadecimal) P1 to P4

FVA3 to FVA0: Character RAM V dot address specificatrion 0 to F (hexadecimal)

FRN1 to FRN0: ROM No. specification 0 to 3 (hexadecimal) No.1 to No.4



(2) Data write

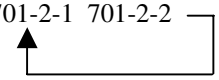
Continuous write mode differs depending on the write mode specification. (RM3)

1. Normal (RM3 = 0: initial state) *Continuous mode not used*

---COM701-1 701-2-1 701-2-2 command wait state ---

2. Write continuous (RM3 = 1) mode

COM701-1 701-2-1 701-2-2



*: In mode 2, the IC remains locked in continuous write mode until the $\overline{CS}$ pin is set high.

- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

2. Display format

2.1 Color Specification Related Items

(1) When a character is specified

Specify color with the character color (character area) and character background color (outside the character area)

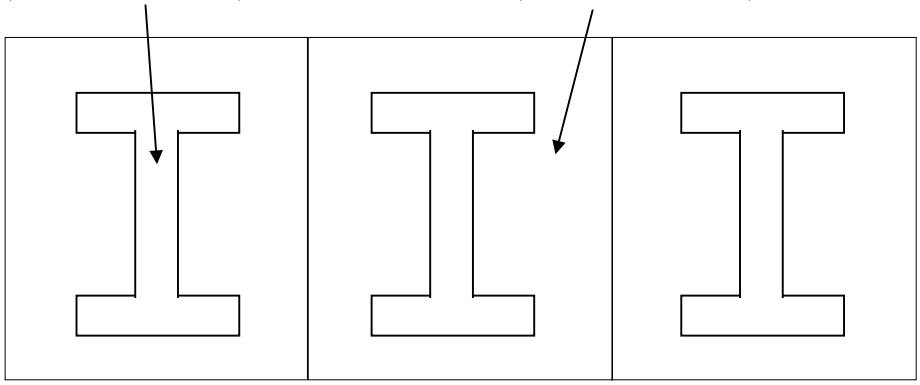
Character color: 1 of 16 colors

Character background color: 1 of 16 colors

Color tables: Table No. 1 to No. 4 specified by CT1 to CT0. (COM10-2-3: VRAM)
1 of 64 types

Character color
Specified by CC0 to CC3: 1of 16 colors
(COM10-2-2: VRAM)

Character background color
Specified by CB0 to CB3: 1 of 16 colors
(COM10-2-2: VRAM)



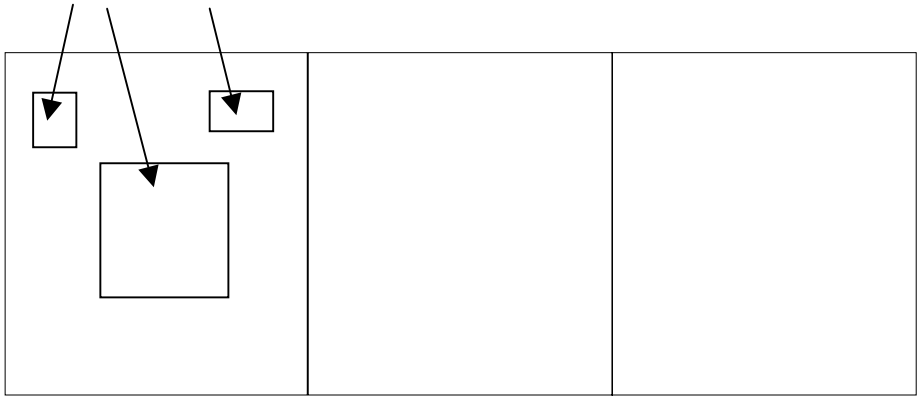
(2) When a graphic 1 is specified

Specify color is in dot units (16×16)

1 of 16 colors (FROM)

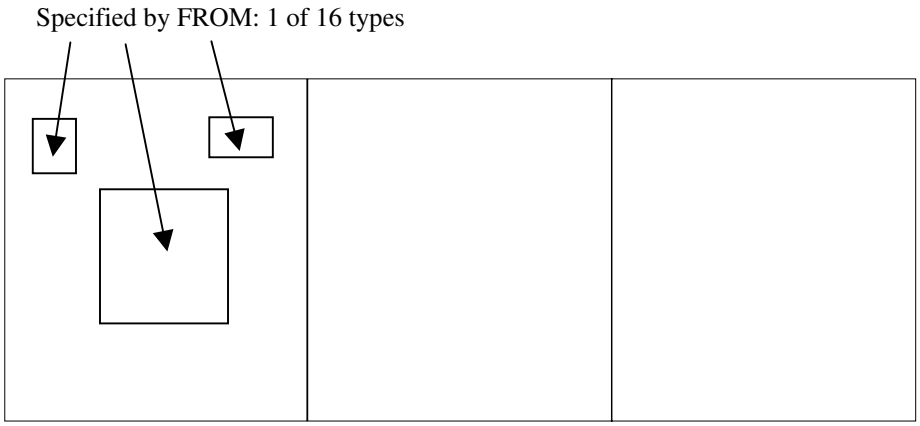
Color tables: Table No. 1 to No. 4 specified by CT1 to CT0. (COM10-2-3: VRAM)
1 of 64 types

Specified by FROM: 1 of 16 types



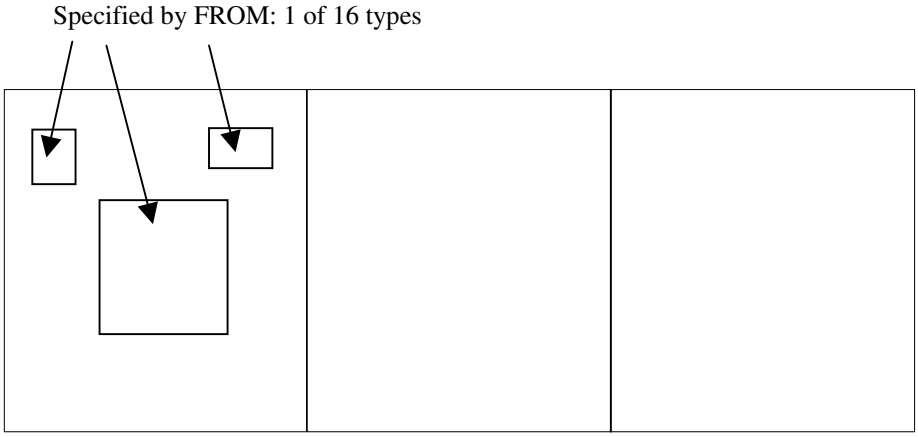
(3) When a graphic 2 is specified
Specify color is in dot units (16×16)
1 of 16 colors (FROM)
Color tables: Table No. 1 to No. 4 specified by CT1 to CT0. (COM10-2-3: VRAM)
1 of 64 types

The CTB address display color shown with CB3 to CB0 is changed to the CTB address display color shown with CC3 to CC0.
One color in the graphic character display can be changed by setting CB and CC.



(4) When a graphic 3 is specified
Specify color is in dot units (16×16)
1 of 16 colors (FROM)
Color tables: Table No. 1 to No. 4 specified by CT1 to CT0. (COM10-2-3: VRAM)
1 of 64 types

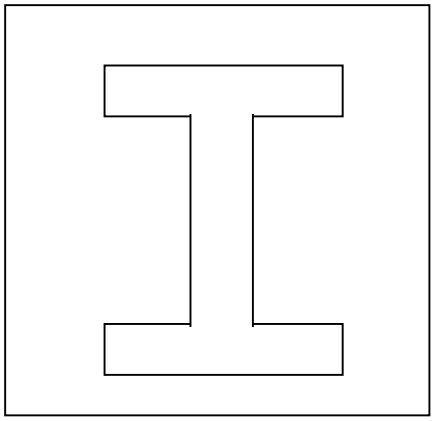
CTB No. in the address shown with CB3 to CB0 is changed to CTB No. shown with CC1 to CC0 and display it.
CTB No. of one color in the graphic character display can be changed by setting CB and CC.



2.2 Display Control Related Items

(1) Blinking: In character units

1. Normal at1 = 0 (COM10-2-1: VRAM)



2. Blinking at1 = 1

Display alternates between normal and transparent with the blinking period. (COM21-2: BK1, BK0)

(2) Border display: Only valid for font specified characters

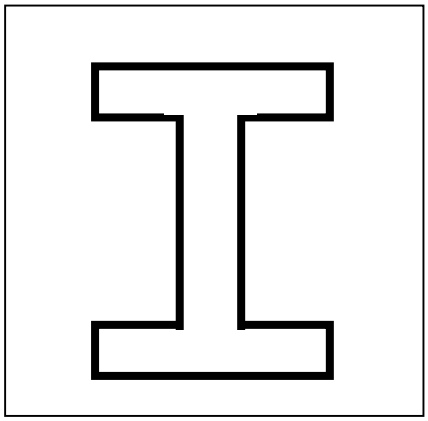
1. Border color: 1 of 16 colors (COM60-2 EGC3 to EGC0)

Color table specification (COM60-2 EGCT1 to EGCT0)

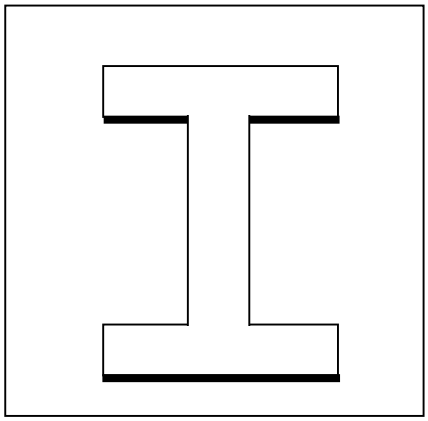
→ 1 of 64 types specified in line units

2. Border mode control (COM60-2 BLK1, BLK0) specified in line units

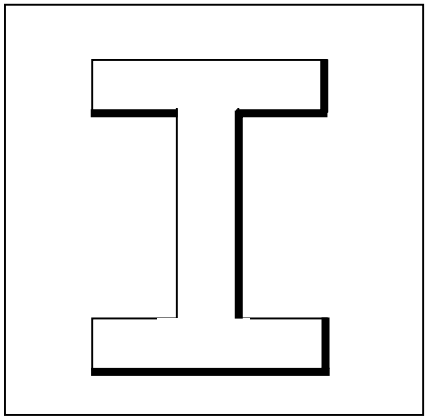
i. Border



ii. Shadow 1: lower

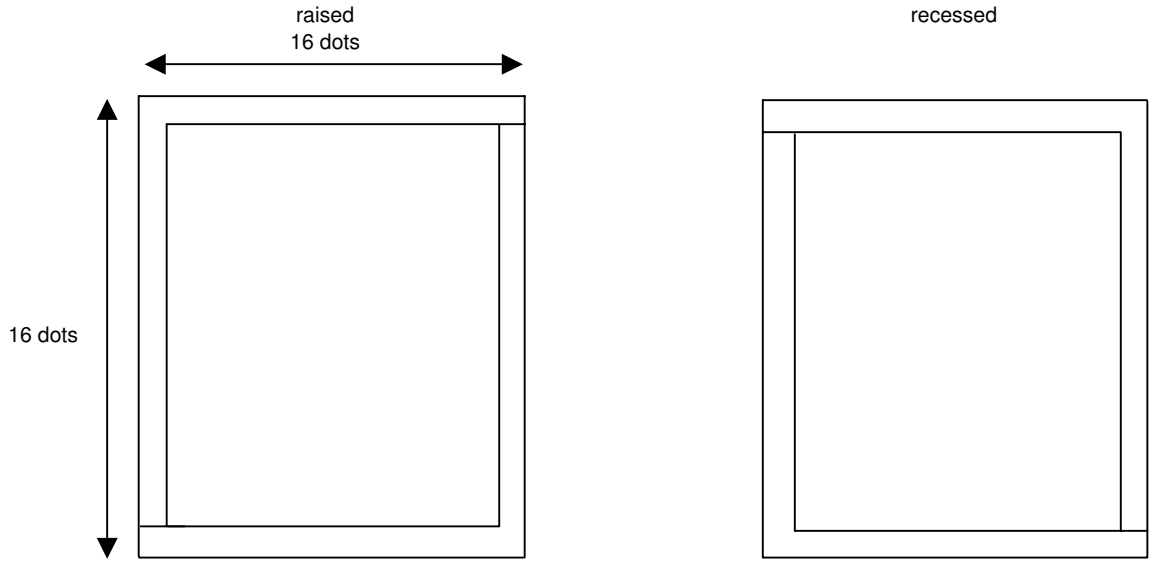


iii. Shadow 2: lower + right



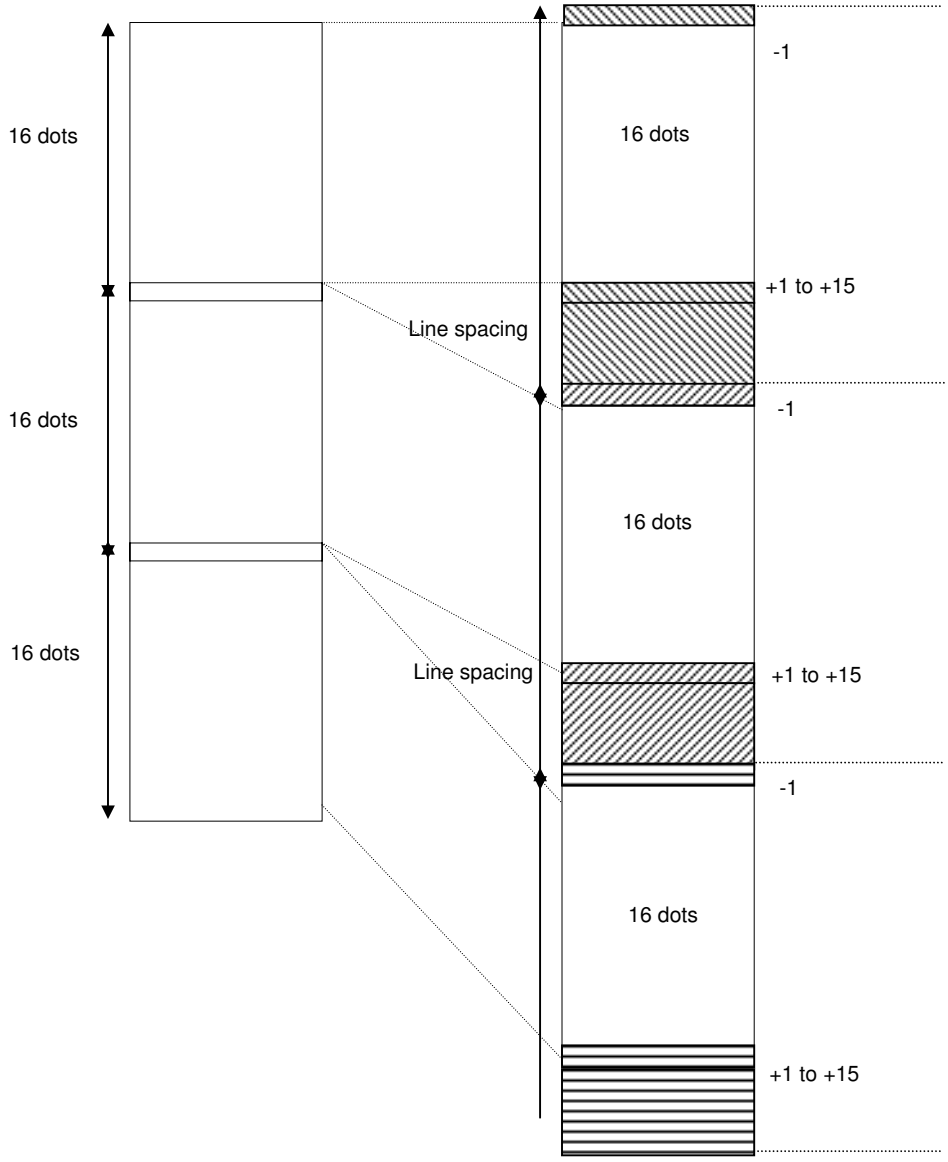
(3) Character size: Specified in line units
The character size is specified as 1x to 4x independently for the vertical and horizontal directions. (COM40-2)

2.3 Box Display (raised/recessed)



(1) Raised/recessed specification: In character units (COM10-2-1 BXS)
(2) Left side-displayed/undisplayed specification: in character units (COM10-2-1 BXL)
(3) Right side-displayed/undisplayed specification: in character units (COM10-2-1 BXR)
(4) Upper side-displayed/undisplayed specification: in character units (COM10-2-1 BXU)
(5) Lower side-displayed/undisplayed specification: in character units (COM10-2-1 BXD)
(6) Color specification: In line units
COM50 (Upper side)
COM51 (Lower side)
BXUC3 to BXDC0: 1 of 16 colors
BXDC3 to BXDC0: 1 of 16 colors
Color table specification
BXUCT1 to BXUCT0
BXDCT1 to BXUCT0
1 of 64 types
Box dot width specification
Each of left, right, upper, and lower can be specified independently.
Left: BXLW1 to BXLW0 1 to 4 dots
Right: BXRW1 to BXRW0 1 to 4 dots
Upper and lower (COM59-2)
Upper BXWU 1 to 2 dots (It depends on the character size.)
Lower BXWD 1 to 2 dots (It depends on the character size.)

2.4 Line spacing control (Command 58-2: GY3, GY2, GY1, GY0)

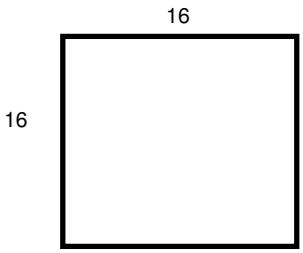


- Line spacing display control
  COM58-2: GS1, GS0

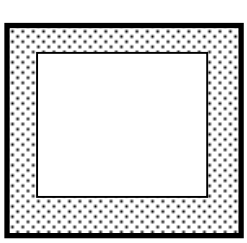
	Character	Graphic
(1)	Transparent	Transparent
(2)	Transparent ±1(character background color)	Transparent ±1(CB specified color)
(3)	Character background color	CB setting color
(4)	Transparent (Border enabled)	Transparent

- Basic line spacing unit
  GYBCK "0": 1V
  "1": It depends on the character size.

- Box display (COM59-2)
  Character display range

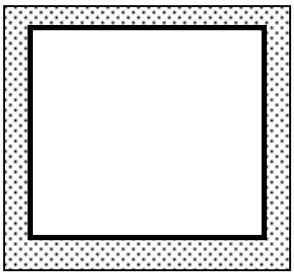


Box display



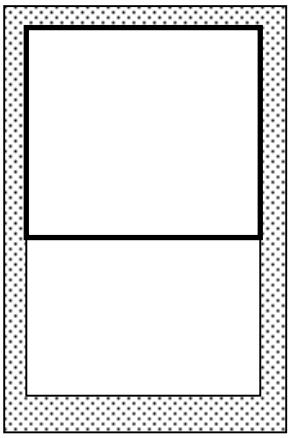
Inside the character

BXC1 = "0"
BXC2 = "0"



Outside the character 1
(Valid only when line spacing is set.)

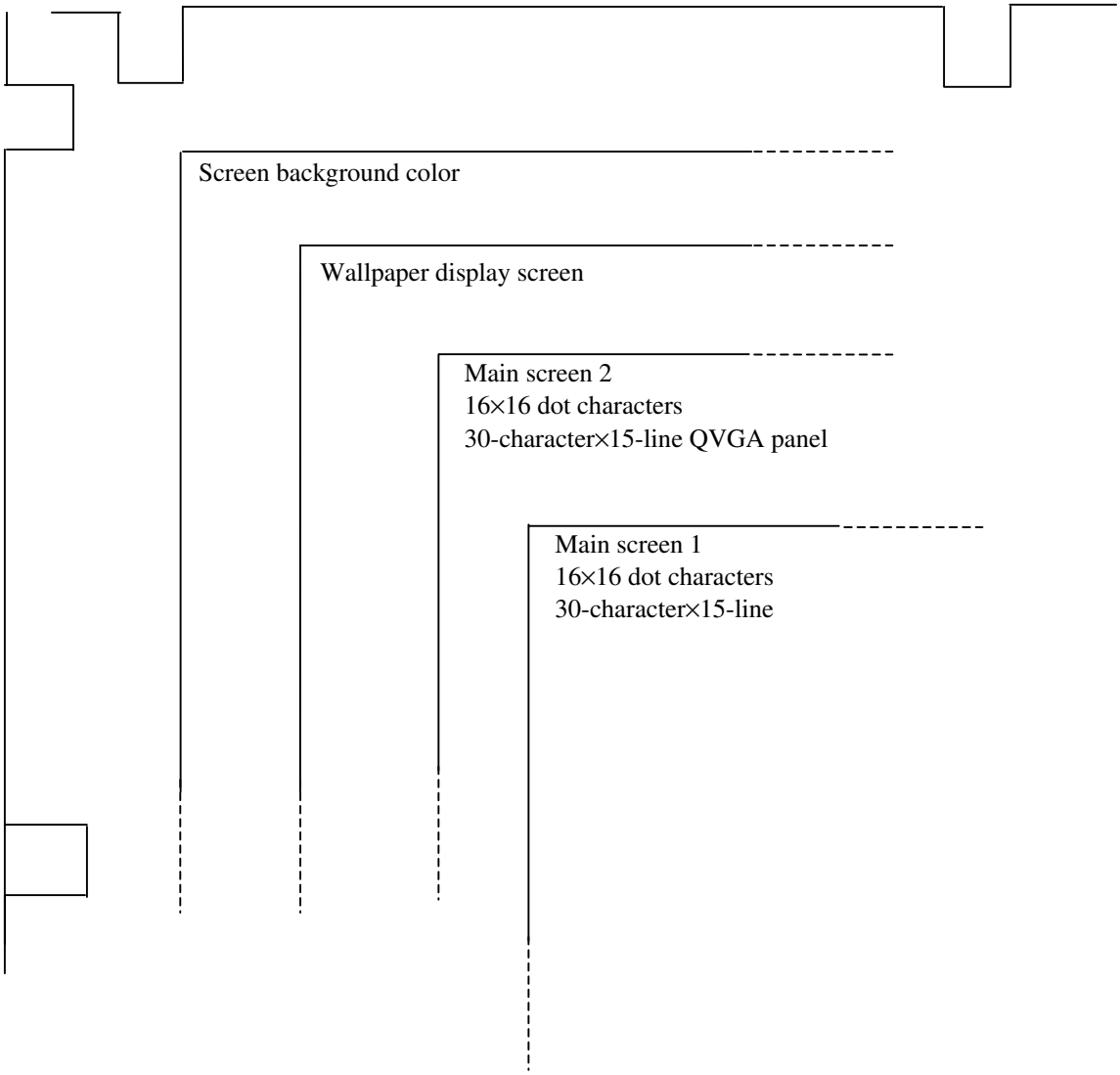
BXC1 = "1"
BXC2 = "1"
BXC3 = "0"



Outside the character 2
(Valid only when line spacing is set.)

BXC1 = "1"
BXC2 = "1"
BXC3 = "1"

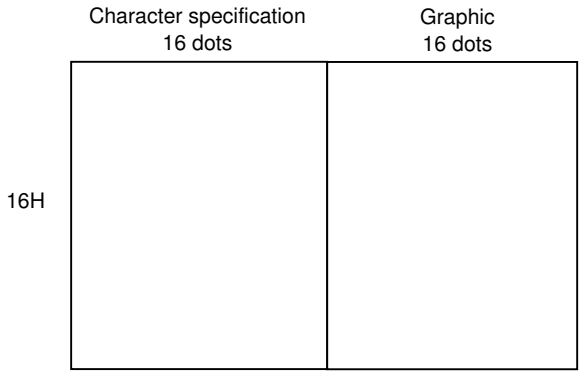
2.5 Screen Structure



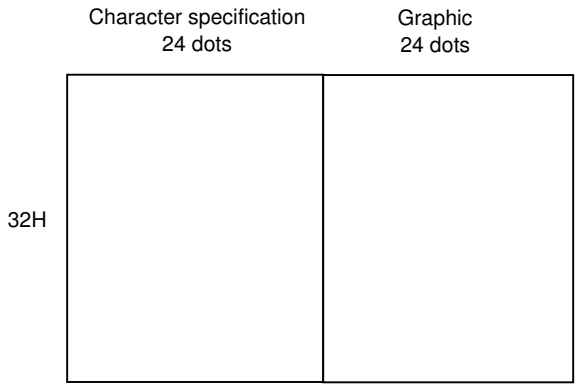
- For each screen: Display on/off (transparent) can be specified independently.
- For each screen: The display start position can be specified independently.
  The wallpaper display screen and the main screen require xxxx clocks before the horizontal start position is reached.

• Display Format

1) QVGA



2) WVGA



• ROM structure

(1) No internal ROM

(2) Internal character RAM QVGA: 4 characters, WVGA: 1 character

1) Character font

QVGA: 16×16-dot structure

WVGA: 24×32-dot structure

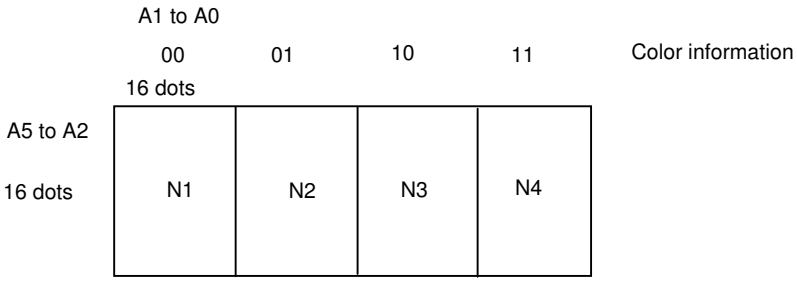
2) Graphics

QVGA: 16×16-dot structure

WVGA: 24×32-dot structure

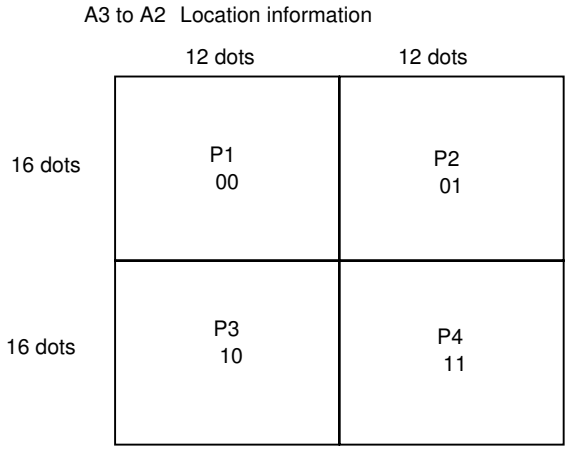
(3) External ROM (QVGA: 16384 characters, WVGA: 4096 characters)
×16 types, 16M
1) Conditions
- QVGA mode
  Access time = 2× dot clock frequency or shorter
  Example: DCLK = 10MHz = 100ns×2 = 200ns or shorter
- WVGA mode
  1) Access time =3× dot clock frequency or shorter, with display limitations
  Example: DCLK = 33MHz = 30ns×3 = 90ns or shorter
  2) Access time =2× dot clock frequency or shorter, with display limitations
  Example: DCLK = 33MHz = 30ns×2 = 60ns or shorter
  3) Access time =1× dot clock frequency or shorter
  Example: DCLK = 33MHz = 30ns×1 = 30ns or shorter

2) ROM map
- QVGA
  - Address
    A19 to A0
  - Data
    D15 to D0
    Used



A19 to A6 (14 bits) = 16384 characters = character codes

- WVGA
  - Address
    A19 to A0
  - Data
    D15 to D12, D11 to D0
    Unused Used



On each of P1 to P4

A19 to A8 (12 bits) = 4096 characters = character codes

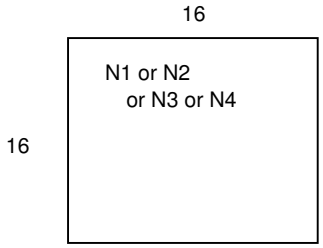
3) Display appearance

- QVGA: 1 character = 16×16 dots

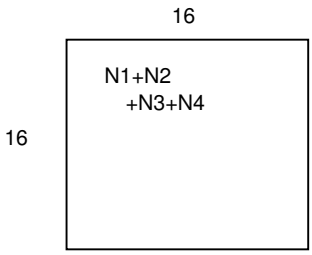
  Character N1 or N2 or N3 or N4, VRAM selectable

  Graphic N1+N2+N3+N4

Character



Graphic



- WVGA: 1 character = 24×32 dots

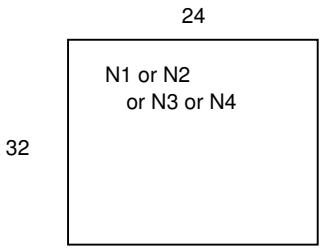
  Character P1+P2+P3+P4 (12×16×4)

  N1 or N2 or N3 or N4, VRAM selectable

  Graphic P1+P2+P3+P4 (12×16×4)

  N1+N2+N3+N4

Character



Graphic