

SANYO Semiconductors

DATA SHEET

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LC88F42A0PA/A0PAU — For Car Audio Systems

For Car Audio Systems 16-bit ETR Microcontroller (ALL FLASH)

Overview

The LC88F42A0PA/A0PAU is 16-bit microcontroller which is ideally suited as a sub controller in car audio applications for the control of "Power" "Operating mode." They are configured around a CPU that operates at a high speed, and incorporate an internal flash ROM (All Flash, onboard programmable) and RAM. This 16-bit microcontroller integrate on a single chip such principal functions as on-chip debugging, 16-bit timer/counter (may be divided into 8-bit timers/counters), synchronous SIO (also used as the I²C bus interface), UART (full duplex), and 16 vector interrupts.

List of ROM and RAM sizes

Type No.	Flash ROM (byte)	RAM (byte)	Package
LC88F42A0PA/A0PAU	64K	4K	SSOP24 (225mil)

Features

- ■Flash ROM (ALL FLASH)
 - Single 3.3V power supply, on-board writeable
 - Block erase in 128/512/1K byte units
- Minimum instruction cycle time (Tcyc)
 - 83.3ns

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Ports

• Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units: 13 (P00 to P07, P10, P13 to P15, P17)

• 5V Tolerant I/O ports : 3 (P11, P12, P16)

Low-pass filter pin
Regulator pins
Reset pins
TEST pins
Crystal oscillator pins
Power pins
1 (LPFO)
1 (VREG)
1 (RESB)
2 (XT1, XT2)
2 (VDD1, VSS1)

\blacksquare SIO: 2 channels (1 channel are also used as I²C bus.)

• SIO0: 8 bit synchronous SIO

Mode0: 8bit communication (selectable 1 to 8 bits)

- 1) LSB first/MSB first mode selectable
- 2) Built-in 8-bit baud rate generator (transfer cycle: 4 to 512 tCYC)
- 3) Wakeup function

Model: Automatic and continuous data transfer function (selectable 9 to 32768 bits)

- 1) LSB first/MSB first mode selectable
- 2) Built-in 8-bit baud rate generator (transfer cycle: 4 to 512 tCYC)
- 3) Interval function (interval time: 0 to 64 tSCK)
- SMIIC0: Single master I²C/8-bit synchronous SIO

Mode 0: Single-master I²C communication (Master/Slave mode)

1) I²C : Standard-mode/Fast-mode support 2) Baud rate source clock : System clock/External clock

Mode 1: Synchronous 8-bit serial I/O (MSB first)

1) Transfer : 2-wire/3-wire

2) Data length : 8 bits (MSB first)

3) Baud rate source clock : System clock/External clock

■UART: 1 channel

1) Data length : 8 bits (LSB first)
2) Stop bits : selectable 1 to 2 bits

3) Parity bits : None/even parity/odd parity

4) Transfer rate : 8 to 4096 cycles

- 5) Baudrate source clock: System clock/XT clock/VCO clock
- 5) Wakeup function
- 6) Full duplex communication

■Timers

- Timer 0: 16-bit timer that supports PWM/toggle outputs
 - 1) 5-bit prescaler
 - 2) 8-bit PWM × 2 mode/8-bit timer + 8-bit PWM mode selectable.
 - 3) Clock source selectable from system clock, XT clock, VCO clock, and internal RC oscillator.
- Timer 1: 16-bit timer with capture registers
 - 1) 5-bit prescaler
 - 2) 16-bit timer/8-bit timer \times 2 selectable
 - 3) Clock source selectable from system clock, XT clock, VCO clock, and internal RC oscillator.
- Timer 2: 16-bit timer with capture registers
 - 1) 4-bit prescaler
 - 2) 16-bit timer/8-bit timer \times 2 selectable
 - 3) Clock source selectable from system clock, XT clock, VCO clock, and external events.
- Timer 8
 - 1) Clock source selectable from XT clock (32.768 kHz) and frequency-divided output of system clock.
 - 2) Interrupts can be generated in 8 timing schemes.
- Clock timer
 - 1) Clock source is XT clock (32.768 kHz).
 - 2) Interrupts can be generated in 4 timing schemes.
 - 3) Built-in temperature compensation circuit.
 - 4) Continues operate when in HOLDX mode.
- ■Day, minute and second counter
 - 1) Count-up of clocks output from Clock timer
 - 2) Configured with day counter, minute counter, and second counter.
 - 3) Continues operation when in HOLDX mode.
- ■Watchdog Timer: 1 channel
 - Clock source is Timer 8.
 - Watch dog timer can operate interrupt or reset.

■Interrupts

- 26 sources, 16 vector addresses
 - 1) Provides three levels of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Source
1	H00080	WDT (1)
2	08004H	Timer 8 (2)/Clock timer (1)
3	08008H	Timer 0 (2)
4	0800CH	INT0 (1)
5	08010H	
6	08014H	INT1 (1)
7	08018H	INT2 (1)/timer 1 (2)/UART2 (3)
8	0801CH	INT3 (1)/timer 2 (3)/SMIIC0 (1)
9	08020H	
10	08024H	
11	08028H	
12	0802CH	
13	08030H	
14	08034H	
15	08038H	SIO0 (2)
16	0803CH	Port 0 (5)

- Interrupt priority: 3 levels selectable.
- If an interrupt occurs, at the same level, small interrupt vector address will be given priority.
- A number enclosed in parentheses denotes the number of sources.
- Subroutine Stack: Entire maximum RAM space (The stack is allocated in RAM.)
 - Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
 - Subroutine calls that do not automatically save PSW: 4 bytes
- High-speed Multiplication/division instructions
 - 16 bits \times 16 bits
 - 16 bits ÷ 16 bits
 - 32 bits ÷ 16 bits

■Oscillation circuits

RC oscillator circuit (internal)
 XT oscillator circuit
 VCO oscillator circuit (internal)
 For system clock
 For system clock

■System clock divider function

- To operate with low current consumption is possible.
- 1/1 to 1/128 of the system clock frequency can be set.

■Low power consumption mode

• HALT mode: Suspends instruction execution. Keep a setting of the peripheral circuits.

• HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.

• HOLDX mode: Suspends instruction execution and operation of all the peripheral circuits except the modules

operating on the XT clock.

■ Standby Function

- HALT mode: Suspends instruction execution. Keep a setting of the peripheral circuits.
 - 1) The oscillator (XT and VCO and RC) retains state on HALT mode.
 - 2) There are the two ways of releasing the HALT mode.
 - (1) Generating a reset condition
 - (2) Generating an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The oscillator (XT and VCO and RC) automatically stop operation on HOLD mode.
 - 2) There are the five ways of releasing the HOLD mode.
 - (1) Generating a reset condition
 - (2) Enter the specified level to the INT0, INT1, INT2, INT3 at least one of the ports.
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt request generated in UART2
 - (5) Having an interrupt request generated in SIO0
- HOLDX mode: Suspends instruction execution and operation of all the peripheral circuits except the modules operating on the XT clock.
 - 1) The VCO oscillator and RC oscillator automatically stop operation.
 - 2) The XT oscillator retains state on HOLDX mode.
 - 3) There are seven ways of resetting the HOLDX mode.
 - (1) Generating a reset condition
 - (2) Enter the specified level to the INT0, INT1, INT2, INT3 at least one of the ports.
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt request generated in UART2
 - (5) Having an interrupt request generated in SIO0
 - (6) Having an interrupt source established in the Timer 8 circuit
 - (7) Having an interrupt source established in the Clock timer circuit

Reset

- External reset
- This IC is equipped with a detecting circuit of voltage drop. (VDET circuit)

The VDET circuit resets an IC at the time of the voltage drop detection.

- 1) Normal mode HALT mode HOLDX mode detection voltage : 2.90V ±0.10V
- 2) HOLD mode detection voltage : $1.42V \pm 0.15V$

■On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time monitor.
- Single-wire communication

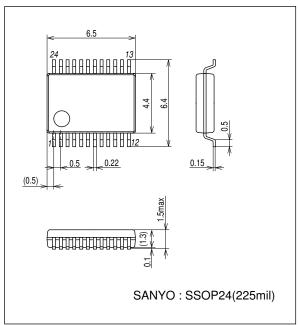
■Shipping Form

• SSOP24 (225mil) Lead free product

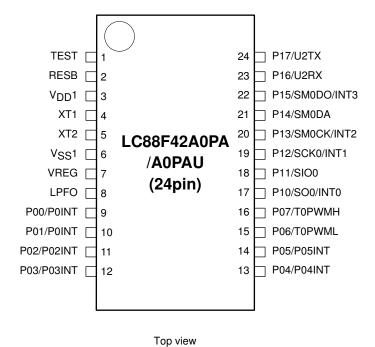
Package Dimensions

unit: mm (typ)

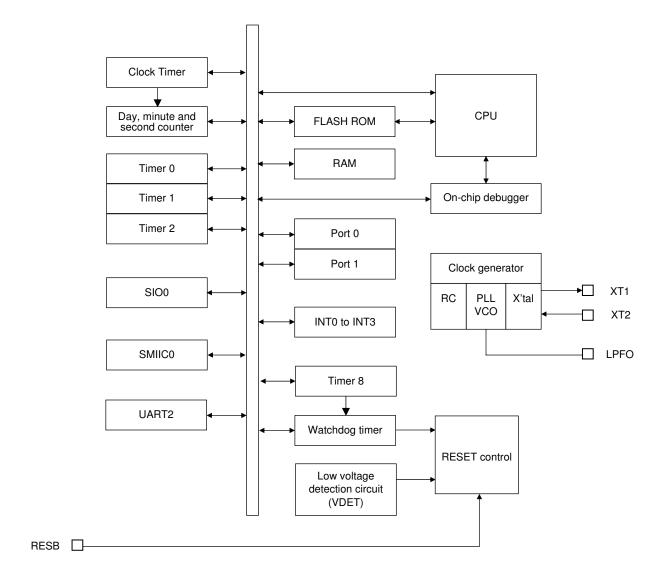
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Pin Assignment



System Block Diagram



Pin Description

Name	I/O	Description
V _{DD} 1	-	+ Power sources
V _{SS} 1	-	- Power sources
Port 0	I/O	8-bit I/O port
P00 to P07	7	• I/O specifiable in 1-bit units
		Pull-up resistors can be turned on and off in 1 bit units
		Port 0 interrupt input (P00 to P05)
		HOLD release input (P00 to P05)
		• Pin functions
		P06: Timer 0L output
		P07: Timer 0H output
Port 1	I/O	• 8-bit I/O port
P10 to P17	7	• I/O specifiable in 1-bit units
		Pull-up resistors can be turned on and off in 1 bit units (Except 5V tolerant port)
		• Pin functions
		P10: SIO0 data output/INT0 input/HOLD release input/Timer 2L capture input
		P11: SIO0 data input and output (5V tolerant port)
		P12: SIO0 clock input and output/INT1 input/HOLD release input/Timer 2H capture input (5V tolerant port)
		P13: SMIIC0 clock input and output/INT2 input/HOLD release input/Timer2 event Input/Timer 2L capture input
		P14: SMIIC0 data bus input and output
		P15: SMIIC0 data output (used in 3-wire SIO mode)/INT3 input/HOLD release Input/Timer 2 event input/Timer 2H
		capture input
		P16: UART2 receive data input (5V tolerant port)
		P17: UART2 transmit data output
		Interrupt acknowledge type
		INT0 to INT3: H level, L level, H edge, L edge, both edges selectable
XT1		Input terminal for 32.768kHz X'tal oscillation
XT2	0	Output terminal for 32.768kHz X'tal oscillation
RESB	I	• Reset pin
		• This must be set to low for 50µs or longer when the power is turned on and when a reset is required.
TEST	I/O	• TEST pin
		Used to communicate with on-chip debugger
		 Connect a pull-down resistor to this terminal. (100kΩ)
LPFO	0	LPF connection pin for PLLVCO
		Connect Low-Pass-Filter to this terminal (See Fig 6)
VREG	0	Regulator output pin
		Connect a bypass capacitor to this terminal. (0.1µF)

Port Output Types

The port output type and pull-up resistor must be set using the registers.

The pin data can be read regardless of the I/O setting of the port.

Pull-up register and the type of port (CMOS output/N channel open drain output) can be set for each port.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = 0V$

Parameter Maximum Supply		Symbol	Applicable Pin	Conditions		Specificat	ion		
		Symbol	/Remarks	Conditions	min	typ	max	unit	
Maximum Supply voltage		V _{DD} max(1)	V _{DD} 1		-0.3		+4.6		
Input voltage		V _I (1)	RESB, XT1		-0.3		V _{DD} (1)+0.3		
	ut/Output tage	V _{IO} (1)	P00 to P07, P10, P13 to P15, P17, XT2		-0.3		V _{DD} (1)+0.3	V	
		V _{IO} (2)	P11, P12, P16	$V_{DD}1 = V_{DD}(1)$	-0.3		6.0		
		V _{IO} (3)		$V_{DD}1 < V_{DD}(1)$	-0.3		3.6		
urrent	Peak output current	IOPH(1)	P00 to P07, P10 to P17	CMOS output selected Per 1 application pin	-10				
High level output current	Average output current (Note 1-1)	IOMH(1)	P00 to P07, P10 to P17	CMOS output selected Per 1 application pin	-7.5				
High le	Total output current	ΣΙΟΑΗ(1)	P00 to P07, P10 to P17	Total of all applicable pins	-25				
urrent	Peak output current	IOPL(1)	P00 to P07, P10 to P17	Per 1 application pin			20	mA	
Low level output current	Average output current (Note 1-1)	IOML(1)	P00 to P07, P10 to P17	Per 1 application pin			10		
Total output current		ΣIOAL(1)	P00 to P07, P10 to P17	Total of all applicable pins			25		
	owable power sipation	Pd max	SSOP24(225mil)	Ta = -40 to +85°C			150	mW	
•	erating nperature range	Topr			-40		+85	°C	
	rage nperature range	Tstg			-45		+125	°C	

Note 1-1: Average output current is average of current in 100ms interval.

Allowable Operating Conditions at Ta = -40 °C to +85 °C, $V_{SS}1 = 0V$

B	0	Applicable Pin	0 !!!!		Specific	cation	
Parameter	Symbol	/Remarks	Conditions	min	typ	max	unit
Operating supply voltage	V _{DD} (1)	V _{DD} 1		3.0		3.6	
Memory sustaining supply voltage	VHD	V _{DD} 1	RAM and register contents in HOLD mode.	1.2			
High level input voltage	V _{IH} (1)	P00 to P07 P10, P13 to P15, P17	V _{DD} 1=V _{DD} (1)	0.3×V _{DD} (1) +0.7		V _{DD} (1)	
	V _{IH} (2)	RESB	V _{DD} 1=V _{DD} (1)	0.75×V _{DD} (1)		V _{DD} (1)	
	V _{IH} (3)	P13, P14 (I ² C setting)	V _{DD} 1=V _{DD} (1)	0.7×V _{DD} (1)		V _{DD} (1)	V
	V _{IH} (4)	P11, P12, P16	V _{DD} 1=V _{DD} (1)	0.3×V _{DD} (1) +0.7		5.5	
Low level input voltage	V _{IL} (1)	P00 to P07 P10 to P17	V _{DD} 1=V _{DD} (1)	V _{SS}		0.1×V _{DD} (1) +0.4	
	V _{IL} (2)	RESB	V _{DD} 1=V _{DD} (1)	V _{SS}		0.25×V _{DD} (1)	
	V _{IL} (3)	P13, P14 (I ² C setting)	V _{DD} 1=V _{DD} (1)	V _{SS}		0.3×V _{DD} (1)	
Instruction cycle time	tCYC		V _{DD} 1=V _{DD} (1)	83.3			ns
Supply voltage rise time	Tpup	V _{DD} 1		1		100	ms
Oscillation	FmRC		Internal RC oscillation	0.5	1.0	2.0	MHz
frequency range	FmX'tal	XT1, XT2	32.768kHz crystal oscillation.		32.768		kHz

Electrical Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Symbol	Applicable Pin	Conditions			Specific	ation	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	P00 to P07, P10 to P17, RESB	Output disable Pull-up resistor OFF VIN=VDD(1) (including the off-leak current of the output Tr.)	V _{DD} (1)			1	μΑ
	I _{IH} (2)	XT1	V _{IN} =V _{DD} (1)	V _{DD} (1)		0.18		
Low level input current	I _{IL} (1)	P00 to P07, P10 to P17, RESB	Output disable Pull-up resistor OFF VIN=VSS (including the off-leak current of the output Tr.)	V _{DD} (1)	-1			μΑ
	I _{IL} (2)	XT1	V _{IN} =V _{SS}	V _{DD} (1)		-0.18		
High level output voltage	V _{OH} (1)	P00 to P07, P10 to P17	I _{OH} =-1.0mA, V _{DD} (1)	V _{DD} (1)	V _{DD} (1) -1.0			٧
	V _{OH} (2)		I _{OH} =-0.4mA, V _{DD} (1)	V _{DD} (1)	V _{DD} (1) -0.4			V
Low level output voltage	V _{OL} (1)	P00 to P07, P10 to P12, P15 to P17	I _{OL} =1.6mA	V _{DD} (1)			0.4	٧
	V _{OL} (2)	P13,P14	I _{OL} =3.0mA	V _{DD} (1)			0.4	
Pull-up resistor	Rpu(1)	P00 to P07,P10, P13 to P15,P17	V _{OH} =0.9V _{DD}	V _{DD} (1)	15	35	150	kΩ
Hysteresis voltage	VHYS(1)	RESB, P10 to P17	•P10 to P17: P1FSAn=1			0.1V _{DD}		٧
	VHYS(2)	Low voltage circuit detection voltage				0.05		V
Pin capacitance	СР	All pins	Conditions other than the measurement terminals: VIN=VSS f=1MHz Ta=25 °C			10		pF
Low voltage detection circuit detect voltage	VDET(1)	V _{DD} (1)	Enable low voltage detection circuit Excluding the HOLD mode (Note 3-1)		2.8	2.9	3.0	٧
	VDET(2)	V _{DD} (1)	Enable low voltage detection circuit HOLD mode		1.27	1.42	1.57	

Note 3-1: VDET(1) varies in a standard range.

Therefore, such voltage of the internal reset has individual difference.

But, in the voltage range of V_{DD}(1) to VDET(1), as for the IC, normal operating is possible.

Serial I/O Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

1. SIO0 Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

	Pa	arameter	Symbol	Applicable Pin	Conditions	1		Specifi	cation	
	Га	liaillelei	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
		Period	tSCK(1)	SCK0(P12)	• See Fig. 1.		4			
		Low level	tSCKL(1)	1						
		pulse width		_			2			
		High level	tSCKH(1)				2			
	Input clock	pulse width		_			2			
	ont c		tSCKHA(1)		Automatic communication mode	V _{DD} (1)	6			
	Inp			4	• See Fig. 1.	<u> </u>	-			tCYC
			tSCKHBSY		Automatic communication mode		23			
			(1a)	4	• See Fig. 1.] 				
			tSCKHBSY		Modes other than automatic		4			
>			(1b)		communication mode • See Fig. 1.		4			
Serial clock		Period	tSCK(2)	SCK0(P12)	CMOS output selected					
rial (Toriou	10011(2)	001(0(1 12)	• See Fig. 1.		4			
Sel		Low level	tSCKL(2)	†	300 i igi ii		I		I	
		pulse width	()					1/2		
		High level	tSCKH(2)	1				1/0		tSCK
	*	pulse width						1/2		
	Output clock		tSCKHA(2)		Automatic communication mode					
	put (CMOS output selected	V _{DD} (1)	6			
	Out			_	• See Fig. 1.					
			tSCKHBSY		Automatic communication mode					
			(2a)		CMOS output selected		4		23	tCYC
				4	• See Fig. 1.	-				
			tSCKHBSY		Modes other than automatic					
			(2b)		communication mode		4			
	Da	ta setup time	tsDI(1)	SIO0(P11)	See Fig. 1. Specified with respect to rising					
t	Da	ta setup time	(SDI(T)	3100(F11)	edge of SIOCLK		0.03			
inpu					• See fig. 1.		0.00			
Serial input	Da	ta hold time	thDI(1)	1		V _{DD} (1)				
Se							0.03			
1										
		Output	tdD0(1)	SO0(P10),	• (Note 4-1-2)					
	Input clock	delay time		SIO0(P11)					1+0\/0	
	nt cl								1tCYC +0.05	μs
put	lnp								+0.05	
Serial output				_		Vpp/1)				
ərial	¥		tdD0(2)		• (Note 4-1-2)	V _{DD} (1)				
S	Output clock								1tCYC	
	put								+0.05	
	Out								. 5.00	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to falling edge of SIOCLK. Specified as the time to the beginning of output state change in open drain output mode. See Fig. 1.

2. SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

	Do	ırameter	Symbol	Applicable Pin	Conditions			Specifi	ication	
	Га	liametei	Symbol	/Remarks	Cortallions	V _{DD} [V]	min	typ	max	unit
		Period	tSCK(3)	SCK0(P12)	• See Fig. 1.		2			
Serial clock	Input clock	Low level pulse width	tSCKL(3)			V _{DD} (1)	1			tCYC
Seri	Inpu	High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Da	ta setup time	tsDI(2)	SIO0(P11)	Specified with respect to rising edge of SIOCLKSee fig. 1.	V (4)	0.03			
Serial	Da	ta hold time	thDI(2)			V _{DD} (1)	0.03			μs
Serial output	Input clock	Output delay time	tdD0(3)	SO0(P10), SIO0(P11)	• (Note 4-2-2)	V _{DD} (1)			1tCYC +0.05	

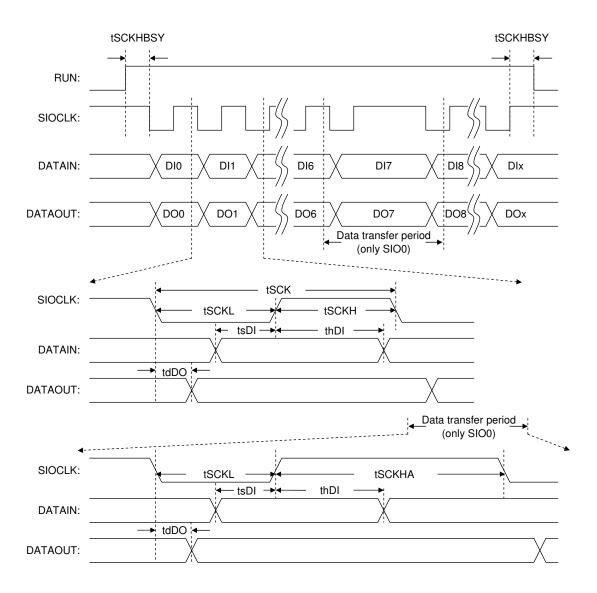
Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to falling edge of SIOCLK. Specified as the time to the beginning of output state change in open drain output mode. See Fig. 1.

3. SMIICO Simple SIO Mode Input/Output Characteristics (Note 4-3-1)

	Da	arameter	Symbol	Applicable Pin	Conditions			Specif	ication	
	Pa	arameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	ж	Period	tSCK(4)	SM0CK(P13)	• See Fig. 1.		4			
	Input clock	Low level pulse width	tSCKL(4)			V _{DD} (1)	2			.0.40
clock	In	High level pulse width	tSCKH(4)				2			tCYC
Serial clock	ck	Period	tSCK(5)	SM0CK(P13)	CMOS output selected See Fig. 1.		8			
	Output clock	Low level pulse width	tSCKL(5)			V _{DD} (1)		1/2		+0.0K
	On	High level pulse width	tSCKH(5)					1/2		tSCK
Serial input	Da	ta setup time	tsDI(3)	SM0DA(P14)	 Specified with respect to rising edge of SIOCLK See fig. 1. 	M (4)	0.03			
Serial	Da	ta hold time	thDI(3)			V _{DD} (1)	0.03			μs
Serial output	Output delay time		tdD0(4)	SM0DO(P15) SM0DA(P14)	Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 1.	V _{DD} (1)			1tCYC +0.05	μο

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.



^{*} Remarks: DIx and DOx denote the last bits communicated; x = 0 to 32768

Figure 1 Serial I/O Waveforms

4. SMIIC0 I²C Mode Input/Output Characteristics (Note 4-4-1)

Period ISCL SMOCK(P13) - See Fig. 2. Period ISCL SMOCK(P13) - See Fig. 2. Period ISCLX SMOCK(P13) - Specified as interval up to time when output state starts changing. Low level pulse width High level stochast pulse width High level starts changing. ISULY SMOCK(P13) - See fig. 2. SMOCK(P13) - See fig. 2. - Standard-mode - Specified as interval up to time when output state starts changing. IBUFX - SMOCK(P13) - See fig. 2. - When SMIIC register control bit, SHDS-1 - See fig. 2. - When SMIIC register control bit, SHDS-1 - See fig. 2. - When SMIIC register control bit, SHDS-1 - See fig. 2. - See fig. 2. - When SMIIC register control bit, SHDS-1 - See fig. 2. - See fig. 2. - See fig. 2. - Standard-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing. - Fast-mode - Specified as interval up to time when output state starts changing.		Pa	rameter		Symbol	Applicable Pin	Conditions		ļ .	Specif	fication	ı
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wnen output state starts changing.									1.1			

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

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Parameter		Symbol	Applicable Pin	Conditions			Specifi	cation	
Parameter		Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Data hold time	Input	tHD; DAT	SM0CK(P13) SM0DA(P14)	• See fig. 2.		0			
	Output	tHD; DATx		Specified as interval up to time when output state starts changing.	V _{DD} (1)	1		1.5	Tfilt
Data setup time	Input	tSU; DAT	SM0CK(P13) SM0DA(P14)	• See fig. 2.	V 40	1			-a.
	Output	tSU; DATx		Specified as interval up to time when output state starts changing.	V _{DD} (1)	1tSCL -1.5Tfilt			Tfilt
Fall time	Input	tF	SM0CK(P13) SM0DA(P14)	• See fig. 2.	V _{DD} (1)			300	
	Ħ	tF		When SMIIC register control bits, PSLW=1	V _{DD} (1)	20+0.1Cb		250	ns
	Output			When SMIIC register control bits, PSLW=0 Cb ≤ 400pF	V _{DD} (1)			100	

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: The value of Tfilt is determined by the values of the register SMICORG, bits 7 and 6 (BRP1,

BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC × 1
0	1	tCYC × 2
1	0	tCYC × 3
1	1	tCYC × 4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

 $250 \text{ns} \ge \text{Tfilt} > 140 \text{ns}$

Note 4-4-3: Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 400 pF$

Note 4-4-4: The standard-mode refers to a mode that is entered by configuring SMIC0BRG as follows:

 $250 \text{ns} \ge \text{Tfilt} > 140 \text{ns}$

BRDQ (bit5) = 1

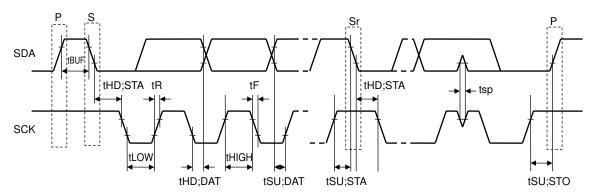
SCL frequency setting ≤ 100kHz

The fast-mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns \geq Tfilt > 140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz



S: Start condition

P: Stop condition

Sr: Restart condition

Figure 2 I²C Timing

5. UART2 Operating Conditions at Ta = -40 °C to +85 °C, $V_{SS}1 = 0V$

Parameter	Cumhal	Applicable Pin	Conditions	Specification				
	Symbol	/Remarks		٧ _{DD} [۷]	min	typ	max	unit
Transfer rate	UBR	U2RX(P16),		V _{DD} (1)			4096	tBGCYC
		U2TX(P17)			0		4096	IBGCTC

Note 5-1: tBGCYC denotes one cycle of the baud rate clock source.

6. Pulse Input Conditions at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

D	0	Applicable Pin	0.000		Specification			
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High/low level minimum pulse width	tPIH(1) tPIL(1)	INT0(P10), INT1(P12), INT2(P13), INT3(P15)	Interrupt source flag can be set. Event inputs for timer 2 is enabled.	V _{DD} (1)	2			tCYC
	tPIL(2)	RESB	Can be reset via the external reset pin. (Note 6-1)	V _{DD} (1)	50			μs
	tPIL(3)	V _{DD} (1)	Can be reset by the low voltage detection circuit. (Note 6-1)	(Note 6-2)	50			μs

Note 6-1: This parameter specifies the time required to ensure that the reset sequence is carried out without fail. The reset may be applied even if this time specification is not satisfied.

Note 6-2: (VDD1 voltage) ≤ (VDET circuit detection voltage)

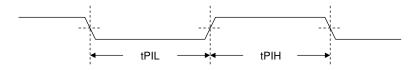


Figure 3 Pulse Input Timing Signal Waveform

7. Consumption Current Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Davamatar	Symbol	Applicable Pin	Conditions		Specification				
Parameter	/Remarks		V _{DD} [V]	min	typ	max	unit		
Normal mode consumption current (Note 7-1)	rrent System clock set to VCO (12MHz) Internal RC oscillation stopped		Internal RC oscillation stopped	V _{DD} (1)		10	15	mA	
	IDDOP(2)		FmX'tal=0kHz (oscillation stopped) System clock set to internal RC oscillation 1/1 frequency division mode	V _{DD} (1)		3.5	5		
	IDDOP(3)		FmX'tal=32.768kHz crystal oscillation mode System clock set to 32.768kHz Internal RC oscillation stopped 1/1 frequency division mode	V _{DD} (1)		35	150	μΑ	
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V _{DD} 1	HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to VCO (12MHz) • Internal RC oscillation stopped • 1/1 frequency division mode	V _{DD} (1)		3.5	5	mA	
	IDDHALT(2)		HALT mode • FmX'tal=0kHz (oscillation stopped) • System clock set to internal RC oscillation • 1/1 frequency division mode	V _{DD} (1)		0.2	1		
	IDDHALT(3)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	V _{DD} (1)		15	100	μА	
HOLD mode consumption current	IDDHOLD(1)	V _{DD} 1	HOLD mode	V _{DD} (1)		1	30	μΑ	
HOLDX mode consumption current	IDDHOLD(2)	V _{DD} 1	HOLDX mode • FmX'tal=32.768kHz crystal oscillation mode • Oscillation register control bits AMPSEL=1	V _{DD} (1)		8	50	μА	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

8. F-ROM Programming Characteristics at $Ta = +10^{\circ}C$ to $+55^{\circ}C$, $V_{SS}1 = 0V$

Doromotor	O. mala al	Applicable Pin	Conditions		Specification			
Parameter	Symbol	/Remarks	Conditions V _{DD} 1		min	typ	max	unit
Onboard programming current	I _{DD} FW(1)	V _{DD} 1	Excluding the current consumption of the Microcontroller.	V _{DD} (1)		5	10	mA
Onboard .	tFW(1)		• 128/512/1K-byte erase operation	V _{DD} (1)		20	30	ms
programming time	tFW(2)		2-byte programming operation	V _{DD} (1)		40	60	μs
times of rewriting	nFW(1)			V _{DD} (1)			500	time

Power Pin Treatment Condition 1 (VDD1, VSS1)

Connect capacitors that meet the following conditions between the V_{DD}1 and V_{SS}1 pins:

- Connect among the V_{DD}1 and V_{SS}1 pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
- The capacitance of C2 should be approximately $0.1\mu F$ or larger.
- Please mount a suitable capacitor about C1.
- \bullet The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.

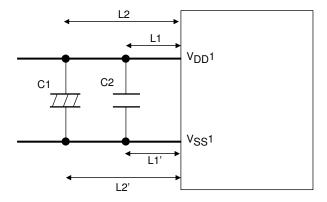


Figure 4

Power Pin Treatment Condition 2 (VREG, VSS1)

Connect capacitors that meet the following conditions between the VREG and VSS1 pins:

- Connect among the VREG and VSS1 pins and the capacitors C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1µF.
- The VREG and VSS1 traces must be thicker than the other traces.

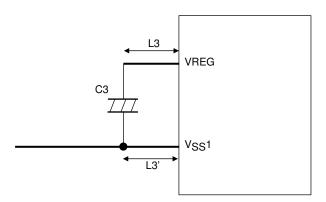


Figure 5

LPF Pin Treatment Condition (LPFO)

Insert a resistor and capacitors that meet the following conditions between the LPFO and VSS1 pins.

 $R1 = 3.3k\Omega$

 $C4 = 0.068 \mu F$

 $C5 = 0.0039 \mu F$

- Routing traces between the LPFO and VSS1 pins and the resistor and capacitors, and between R1 and C4 must be as short as possible.
- * After the PLL circuit is activated, 50ms or more is required for stabilizing oscillation.

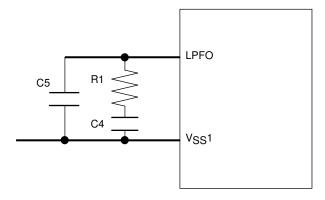


Figure 6

TEST Pin Treatment Condition (TEST)

Insert a resistor that meets the following condition between the TEST and VSS1 pins.

$$R_{TEST} = 100k\Omega$$

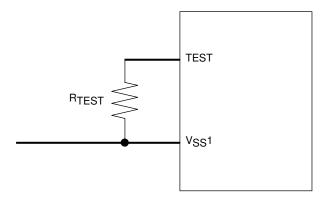
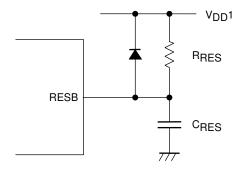


Figure 7

Reset Pin Treatment Condition (RESB)



(Note)

When the power is turned on, the RESB pin must be set to the low level.

(A reset period of 50µs or longer is required after the power has stabilized.)

Recommended value

RRES: $100k\Omega$ CRES: 0.033μ F

Figure 8 Reset Circuit

Crystal Oscillator Pin Treatment Condition (XT1, XT2)

Connect among the XT1 and XT2 pins and the circuit elements (C1, C2, Rd, X'tal) with the shortest possible lead wires.

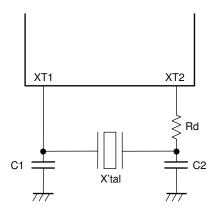


Figure 9 XT Oscillator Circuit

Example of Crystal Oscillator Circuit Characteristics

Given below are the characteristics of a sample crystal oscillator circuit that were measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Example of Crystal Oscillator Circuit Characteristics with a Crystal Resonator

				Cir	cuit Const	ant	Operating	Oscillator	
	Nominal Frequency	Vendor Name	Oscillator Name	C1	C1 C2		Voltage	Stabilization Time	Remarks
1				[pF]	[pF]	Rd [Ω]	Range	tms ^{X'tal} (typ)	
							[V]	[ms]	
3	32.768kHz	RIVER ELETEC	TFX-03 (CL=12.5pF)	15	15	680k	V _{DD} (1)	200	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the XT oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 10 and Figure 11).

Note: The shown in Table 1 is a reference value.

Circuit Constant: This is determined by evaluations in the oscillator manufacturer.

This value differs depending on the parts, board, and oscillator.

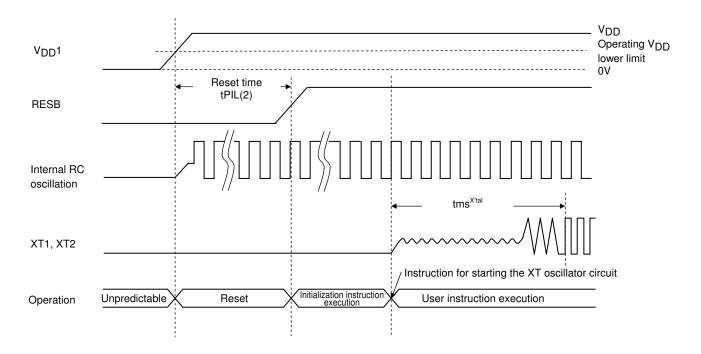


Figure 10 Reset Time and Oscillation Stabilization Time

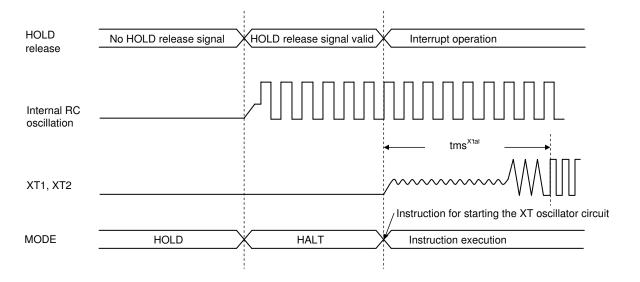


Figure 11 HOLD Release and Oscillation Stabilization Time

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