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SANYO Semiconductors
DATA SHEET

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LC8783P7PA/P6PA/M4PA /J3PA/J2PA/G1PA/G0PA /C8PA/96PA

CMOS IC
ROM 256K byte, RAM 12K byte
8-bit ETR Microcontroller

Overview

The LC8783P7PA/P6PA/M4PA/J3PA/J2PA/G1PA/G0PA/C8PA/96PA is an 8-bit ETR microcomputer that, centered around a CPU running at a minimum bus cycle time of 74.07 ns, integrate on a single chip a number of hardware features such as 256K-byte ROM (Max size), 12K-byte RAM(Max size), direct control of necessary CD mechanism and CD-DSP for car audio, in the radio reception, the on-chip high-performance PLL circuit provides a high-speed Lock-Up circuit to search for alternative frequency of RDS in a short time, the ability to control the C/N characteristics of a local oscillator, and the high S/N through the direct PLL configuration, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), four 12-bit PWM channels, an 8-bit 10-channel AD converter, a high-speed clock counter, a system clock frequency divider, and a 29-source 10-vector interrupt feature.

Features

Model name	ROM size (Byte)	RAM size (Byte)
LC878396PA	96K	6K
LC8783C8PA	128K	6K
LC8783G0PA	160K	6K
LC8783G1PA	160K	8K
LC8783J2PA	192K	8K
LC8783J3PA	192K	10K
LC8783M4PA	224K	10K
LC8783P6PA	256K	10K
LC8783P7PA	256K	12K

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■Minimum Bus Cycle Time
- 74.07ns (13.5MHz)

  Note: Bus cycle time indicates the speed to read ROM.

■Minimum Instruction Cycle Time (tCYC)
- 222ns (13.5MHz)

■Ports
- Normal withstand voltage I/O ports

  Ports whose I/O direction can be designated in 1 bit units: 57 (P1n, P2n, P30 to P35, P70 to P73, P8n, PBn, PCn, SI2Pm, PWM0, PWM1, XT2, n=0 to 7, m=0 to 3)

  Ports whose I/O direction can be designated in 2 bit units: 16 (PEn, PFn n=0 to 7)

  Ports whose I/O direction can be designated in 4 bit units: 8 (P0n n=0 to 7)
- Normal withstand voltage input ports: 1 (XT1)
- Main charge pump output ports: 1 (EO)
- Sub charge pump output ports: 1 (SUBPD)
- AM local oscillator input ports: 1 (AMIN)
- FM local oscillator input ports: 1 (FMIN)
- High-speed, universal counter input ports: 1 (HCTR)
- Universal counter input ports: 1 (LCTR)
- Internal low voltage output ports: 1 (VREG)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pin: 1 ($\overline{\text{RES}}$)
- Digital power pins: 6 ($V_{SS}n$, $V_{DD}n$ n=1, 2, 4)
- Analogue power pins: 2 (AV_{SS}, AV_{DD})

■Timers
- Timer 0: 16-bit programmable timer/counter with capture register

  Mode 0: 8-bit programmable timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels

  Mode 1: 8-bit programmable timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit programmable counter (with two 8-bit capture registers)

  Mode 2: 16-bit programmable timer with an 8-bit programmable prescaler (with two 16-bit capture registers)

  Mode 3: 16-bit programmable counter (with 2 16-bit capture registers)
- Timer 1: 16-bit programmable timer/counter that support PWM/ toggle output

  Mode 0: 8-bit programmable timer with an 8-bit prescaler (with toggle outputs) + 8-bit programmable timer/counter (with toggle outputs)

  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

  Mode 2: 16-bit programmable timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8 bits)

  Mode 3: 16-bit programmable timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit programmable timer with a 6-bit prescaler
- Timer 5: 8-bit programmable timer with a 6-bit prescaler
- Timer 6: 8-bit programmable timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit programmable timer with a 6-bit prescaler (with toggle outputs)
- Base timer

  1) The clock is selectable from the subclock (32.768kHz crystal oscillator), cycle clock (tCYC), and timer 0 prescaler output.

  2) Interrupts programmable in 5 different time schemes.

■High speed clock counter
1) Can count clocks with a maximum clock rate of 20MHz
(When High-speed clock counter is used, timer 0 cannot be used).
2) Can generate output real time.

■SIO: 3 channels
- SIO 0: 8 bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (4/3 to 512/3 tCYC transfer clock cycle)
  3) Automatic continuous data transmission (1 to 256 bits)
- SIO 1: 8 bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2 to or 3 to wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (Half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO2: 8 bit synchronous serial interface
  1) LSB first mode
  2) Built-in 3-bit baudrate generator (4/3 to 512/3 tCYC transfer clock cycle)
  3) Automatic continuous data transmission (1 to 32 bytes)

■UART: 2 channels
1) Full duplex
2) 7/8/9 bit data bits selectable
3) 1 stop bit (2 bits in continuous transmission mode)
4) Built-in 8-bit baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■AD Converter: 8 bits × 10 channels

■PWM: Multifrequency 12-bit PWM × 4 channels

■Remote control receiver noise filtering function (sharing pins with P73, INT3, and T0IN)
1) Noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC
2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

■Watchdog timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts

- 29 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer (BT0, 1)
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO1/SIO2/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- The Base timers are two interrupt sources of BT0 and BT1, it is one interrupt source by PWM0 and 1, it is one interrupt source by PWM4 and 5.

■Subroutine stack levels

- 6144 levels maximum (1/2 of capacity of RAM, the stack is allocated in RAM.)

■High-speed multiplication/division instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation circuits

- RC oscillator circuit (internal): For system clock
- Main XT crystal oscillator circuit: For system clock with internal Rf and Rd
- Sub XT crystal oscillator circuit: For time-of-day clock, for low-speed system clock with internal Rf and external Rd
- Multifrequency RC oscillator circuit (internal): For system clock
- PLL circuit (internal): For AM/FM tuner

■System clock divider function

- Can run on low current.
- The minimum instruction cycle selectable from 222ns, 444ns, 888ns, 1.78µs, 3.55µs, 7.10µs, 14.2µs, 28.4µs, and 56.8µs.

■PLL block

- Twelve reference frequencies when main XT is 13.5MHz: 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 30kHz, 50kHz, and 100kHz
- Range of input frequency
  1) AMIN: 0.5 to 40MHz
  2) FMIN: 10 to 150MHz
  3) HCTR: 0.4 to 12MHz
  4) LCTR: 100 to 500kHz
- Supports dead zone control.
- Built-in unlock detection circuit.

■Universal counter

- This 20-bit counter can be used for frequency measurement.

■Standby function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by system reset, detection VDET0 or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The main XT crystal oscillators, RC, and sub XT crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the Reset pin to the lower level.
     (2) Voltage descent detection (VDET1)
     (3) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
     (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The main XT crystal oscillators, and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the Reset pin to the low level.
     (2) Voltage descent detection (VDET0)
     (3) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the base timer circuit.

■Reset

- External reset
- Voltage descent detection (VDET0, VDET1) reset circuit (internal)

■Shipping form

- QIP100E (Lead Free Product)

■Flash ROM version

- LC87F83P7PA
- LC87F83P7PAU (User writing)

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter		Symbol	Pins/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}4$, AV_{DD}	$V_{DD}1=V_{DD}2=V_{DD}4=AV_{DD}$		-0.3		+6.5	V
Input voltage		V_I(1)	CF1, XT1, AMIN, FMIN, HCTR, LCTR			-0.3		V_{DD}+0.3	
Input/Output voltage		V_{IO}(1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports B, C, E, F SI2P0 to SI2P3 PWM0, PWM1, XT2			-0.3		V_{DD}+0.3	
Output voltage		V_O(1)	EO, SUBPD			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports 71 to 73 Ports B, C, E, F SI2P0 to SI2P3	CMOS output select. per 1 application pin.		-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 application pin.		-20			
		IOPH(3)	EO, SUBPD	Per 1 application pin.		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3 Ports 71 to 73 Ports B, C, E, F SI2P0 to SI2P3	CMOS output select. per 1 application pin.		-7.5			
		IOMH(2)	PWM0, PWM1	Per 1 application pin.		-15			
		IOMH(3)	EO, SUBPD	Per 1 application pin.		-3			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-25			
		ΣIOAH(2)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 0	Total of all applicable pins		-25			
		ΣIOAH(4)	Ports 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-45			
		ΣIOAH(5)	Ports 2, 3, B	Total of all applicable pins		-25			
		ΣIOAH(6)	Ports C	Total of all applicable pins		-25			
		ΣIOAH(7)	Ports 2, 3, B, C	Total of all applicable pins		-45			
		ΣIOAH(8)	Ports F	Total of all applicable pins		-25			
		ΣIOAH(9)	Ports 1, E	Total of all applicable pins		-25			
		ΣIOAH(10)	Ports 1, E, F	Total of all applicable pins		-45			
		ΣIOAH(11)	EO, SUBPD	Total of all applicable pins		-10			

Note 1-1: Average output current is average of current in 100ms interval.

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Parameter		Symbol	Pins/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 2, 3, 8 Ports B, C, E, F SI2P0 to SI2P3 XT2	Per 1 application pin.				10	mA
		IOPL(2)	PWM0, PWM1	Per 1 application pin.				20	
		IOPL(3)	EO, SUBPD	Per 1 application pin.				5	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1, 2, 3, 7 Ports 8, B, C, E, F SI2P0 to SI2P3 XT2	Per 1 application pin.				7.5	
		IOML(2)	PWM0, PWM1	Per 1 application pin.				20	
		IOML(3)	EO, SUBPD	Per 1 application pin.				5	
	Total output current	ΣIOAL(1)	Ports 7, XT2	Total of all applicable pins				25	
		ΣIOAL(2)	Ports 8	Total of all applicable pins				25	
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				45	
		ΣIOAL(4)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				25	
		ΣIOAL(5)	Ports 0	Total of all applicable pins				25	
		ΣIOAL(6)	Ports 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				45	
		ΣIOAL(7)	Ports 2, 3, B	Total of all applicable pins				25	
		ΣIOAL(8)	Ports C	Total of all applicable pins				25	
		ΣIOAL(9)	Ports 2, 3, B, C	Total of all applicable pins				45	
		ΣIOAL(10)	Ports F	Total of all applicable pins				25	
		ΣIOAL(11)	Ports 1, E	Total of all applicable pins				25	
		ΣIOAL(12)	Ports 1, E, F	Total of all applicable pins				45	
		ΣIOAL(13)	EO, SUBPD	Total of all applicable pins				10	
Maximum power consumption		Pd max	QIP100E	Ta = -40 to +85°C				400	mW
Operating temperature range		Topr				-40		+85	°C
Storage temperature range		Tstg				-45		+125	°C

Note 1-1: Average output current is average of current in 100ms interval.

Recommended operating range at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter	Symbol	Pins/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}4=AV_{DD}$	PLL operation		4.5	5.0	5.5	V
			CPU operation		3.0		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}4=AV_{DD}$	RAM and register contents in HOLD mode.		1.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 1, 2 SI2P0 to SI2P3 P71 to P73 P70 port input/ interrupt setting		3.0 to 5.5	$0.35V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Ports 0, 3, 8 Ports B, C, E, F PWM0, PWM1		3.0 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(3)$	Port70 Watchdog timer setting		3.0 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, $\overline{RES}$	When XT1 and XT2 general purpose input	3.0 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2 SI2P0 to SI2P3 P71 to P73 P70 port input/ interrupt setting		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
	$V_{IL}(2)$			3.0 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Ports 0, 3, 8 Ports B, C, E, F PWM0, PWM1		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
	$V_{IL}(4)$			3.0 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	Port70 Watchdog timer setting		3.0 to 5.5	V_{SS}		$0.8V_{DD}-1.0$	
	$V_{IL}(6)$	XT1, XT2, $\overline{RES}$	When XT1 and XT2 general purpose input	3.0 to 5.5	V_{SS}		$0.25V_{DD}$	
Input amplitude	$V_{IN}(1)$	FMIN, AMIN, HCTR, LCTR	Excluding CF ability setting="00"	4.5 to 5.5	0.04		1.5	Vrms
	$V_{IN}(2)$	FMIN, AMIN, HCTR	CF ability setting="00"	4.5 to 5.5	0.07		1.5	
	$V_{IN}(3)$	FMIN, LCTR	CF ability setting="00"	4.5 to 5.5	0.04		1.5	
Input frequency	FIN(1)	FMIN: $V_{IN}(1)$		4.5 to 5.5	10		150	MHz
	FIN(2)	FMIN: $V_{IN}(2)$		4.5 to 5.5	10		50	
	FIN(3)	FMIN: $V_{IN}(3)$		4.5 to 5.5	50		150	
	FIN(4)	AMIN(H): $V_{IN}(1)$ $V_{IN}(2)$		4.5 to 5.5	2		40	
	FIN(5)	AMIN(L): $V_{IN}(1)$ $V_{IN}(2)$		4.5 to 5.5	0.5		10	
	FIN(6)	HCTR: $V_{IN}(1)$ $V_{IN}(2)$		4.5 to 5.5	0.4		12	
	FIN(7)	LCTR: $V_{IN}(1)$ $V_{IN}(3)$		4.5 to 5.5	100		500	kHz
Instruction cycle time	tCYC (Note 2-1)			3.0 to 5.5	0.222			µs
Oscillation frequency range	FmCF(1)	CF1, CF2	13.5MHz crystal oscillation	3.0 to 5.5		13.5		MHz
	FmRC		Internal RC oscillation	3.0 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	3.0 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation	3.0 to 5.5		32.768		kHz

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter	Symbol	Pins/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2 Ports 3, 7, 8 Ports B, C, E, F SI2P0 to SI2P3 $\overline{RES}$ PWM0, PWM1	Output disable Pull-up resistor OFF $V_{IN}=V_{DD}$ (including the off-leak current of the output Tr.)	3.0 to 5.5			1	μA
	$I_{IH}(2)$	XT1, XT2	Using as an input port $V_{IN}=V_{DD}$	3.0 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	3.0 to 5.5	1	5	15	
	$I_{IH}(4)$	FMIN, AMIN, HCTR, LCTR	$V_{IN}=V_{DD}$	4.5 to 5.5			30	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2 Ports 3, 7, 8 Ports B, C, E, F SI2P0 to SI2P3 $\overline{RES}$ PWM0, PWM1	Output disable Pull-up resistor OFF $V_{IN}=V_{DD}$ (including the off-leak current of the output Tr.)	3.0 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	Using as an input port $V_{IN}=V_{SS}$	3.0 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	3.0 to 5.5	-15	-5	-1	
	$I_{IL}(4)$	FMIN, AMIN, HCTR, LCTR	$V_{IN}=V_{SS}$	4.5 to 5.5	-30			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 Ports B, C, E, F	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$	Ports 71, 72, 73 SI2P0 to SI2P3	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$	PWM0, PWM1 P30, P31(PWM4, 5 output mode)	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(4)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(5)$	EO, SUBPD	I_{OH}=-500μA	4.5 to 5.5	V_{DD}-1			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3 Ports B, C, E, F	I_{OL}=1.0mA	4.5 to 5.5			1.0	
	$V_{OL}(2)$	Ports 71, 72, 73 SI2P0 to SI2P3	I_{OL}=0.4mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$	PWM0, PWM1	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(4)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(5)$	Ports 70, 8, XT2	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$	EO, SUBPD	I_{OL}=500μA	4.5 to 5.5			1.0	
Pull-up resistation	Rpu(1)	Ports 0, 1, 2, 3 Ports 7 Ports B, C, E, F	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			3.0 to 5.5	15	35	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 7 SI2P0 to SI2P3		3.0 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• For pins other than that under test: $V_{IN}=V_{SS}$ • f=1MHz • Ta=25℃	3.0 to 5.5		10		pF
Power down detection voltage	VDET0	$V_{DD}1$	• Excluding the HOLD mode		3.0	3.3	3.6	V
	VDET1		• HOLD mode		1.1	1.6	2.1	

Serial input/output Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

1. SIO0 Serial input/output characteristics (Note 4-1-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 2.	3.0 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • See Fig. 2. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/reception mode • SIO2 is in use simultaneous. • See Fig. 2. • (Note 4-1-2)		6			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected. • See Fig. 2.	3.0 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • CMOS output selected. • See Fig. 2.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3)tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/reception mode • SIO2 is in use simultaneous. • CMOS output selected. • See Fig. 2.		tSCKH(2) +2tCYC		tSCKH(2) +(16/3)tCYC	
Serial input	Data setup time		tsDI(1)	SI0(P11), SB0(P11)	• Must be specified with respect to rising edge of SIOCLK • See fig. 2.	3.0 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	3.0 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode. • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		• (Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 2.

2. SIO1 Serial input/output characteristics (Note 4-2-1)

Parameter			Symbol	Pins/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 2.	3.0 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected. • See Fig. 2.		2			
		Low level pulse width	tSCKL(4)			3.0 to 5.5	1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SI1(P14), SB1(P14)	• Must be specified with respect to rising edge of SIOCLK • See fig. 2.	3.0 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 2.	3.0 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

3. SIO2 Serial input/output characteristics (Note 4-3-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK2 (SI2P2)	• See Fig. 2.	3.0 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• Continuous data transmission/reception mode of SIO0 is not in use simultaneous. • See Fig. 2. • (Note 4-3-2)		4			
			tSCKHA(5b)		• Continuous data transmission/reception mode of SIO0 is in use simultaneous. • See Fig. 2. • (Note 4-3-2)		7			
	Output clock	Frequency	tSCK(6)	SCK2 (SI2P2), SCK2O (SI2P3)	• CMOS output selected. • See Fig. 2.	3.0 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)				1/2			
		High level pulse width	tSCKH(6)				1/2			
			tSCKHA(6a)		• Continuous data transmission/reception mode of SIO0 is not in use simultaneous. • CMOS output selected. • See Fig. 2.		tSCKH(6) +(5/3)tCYC		tSCKH(6) +(10/3)tCYC	tCYC
			tSCKHA(6b)		• Continuous data transmission/reception mode of SIO0 is in use simultaneous. • CMOS output selected. • See Fig. 2.		tSCKH(6) +(5/3)tCYC		tSCKH(6) +(19/3)tCYC	
Serial input	Data setup time		tsDI(3)	SI2(SI2P1), SB2(SI2P1)	• Must be specified with respect to rising edge of SIOCLK • See fig. 2.	3.0 to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Output delay time		tdD0(5)	SO2(SI2P0), SB2(SI2P1)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 2.	3.0 to 5.5			(1/3)tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input, a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Pulse input conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	3.0 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	3.0 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	3.0 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/28.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	3.0 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	3.0 to 5.5	200			µs

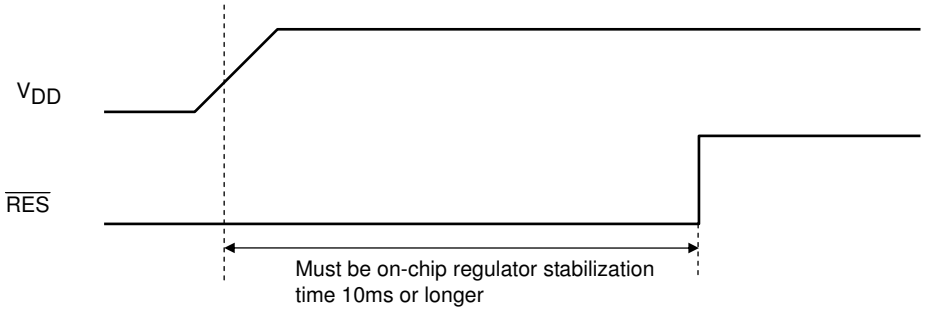


Fig. Timing of Power-on Reset Operation

AD converter characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87) AN8(P70) AN9(P71)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	3.0 to 5.5	7.104(tCYC=0.222µs)			µs
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	3.0 to 5.5	14.21(tCYC=0.222µs)			
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

Parameter	Symbol	Pins/ Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}4$ =AV_{DD}	• FmCF=13.5MHz crystal oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 13.5MHz • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio.	4.5 to 5.5		8.0	10.0	mA
	IDDOP(2)			3.0 to 4.5		6.0	8.0	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		0.8	1.2	
	IDDOP(4)			3.0 to 4.5		0.6	1.0	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • Internal RC oscillation stopped • System clock set to 1MHz with frequency variable RC oscillation • 1/2 frequency division ratio.	4.5 to 5.5		0.8	2.0	
	IDDOP(6)			3.0 to 4.5		0.5	1.5	
	IDDOP(7)		• FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		300	500	μA
	IDDOP(8)			3.0 to 4.5		250	450	
	IDDOP(9)		• FmCF=13.5MHz crystal oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 13.5MHz • Internal RC oscillation operation • Frequency variable RC oscillation stopped • 1/1 frequency division ratio. • FM Amp ON 130MHz Reception • HCTR Amp ON IF count 10.7MHz	4.5 to 5.5		15.0	20.0	mA

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

General-purpose I/O port "L" output when the above-mentioned data is measured

However, the P0 port is an input setting because of the mode setting

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}4$ =AV_{DD}	• HALT mode • FmCF=13.5MHz crystal oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 13.5MHz • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio.	4.5 to 5.5		2.0	3.0	mA
	IDDHALT(2)			3.0 to 4.5		1.8	2.5	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		0.5	1.0	
	IDDHALT(4)			3.0 to 4.5		0.3	0.8	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • Internal RC oscillation stopped • System clock set to 1MHz with frequency variable RC oscillation • 1/2 frequency division ratio.	4.5 to 5.5		1.0	2.0	
	IDDHALT(6)			3.0 to 4.5		0.8	1.5	
	IDDHALT(7)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio.	4.5 to 5.5		250	500	μA
	IDDHALT(8)			3.0 to 4.5		200	400	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	• HOLD mode	4.5 to 5.5		1.5	20.0	
	IDDHOLD(2)			3.0 to 4.5		1.0	18.0	
Time-base clock HOLD mode consumption current	IDDHOLD(3)	$V_{DD}1$	• Timer HOLD mode • FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		150	300	
	IDDHOLD(4)			3.0 to 4.5		100	200	
Intermittent for time-base clock mode consumption current	IDDCLOCK(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}4$ =AV_{DD}	• Intermittent for clock mode • Each 500ms is shifted to a normal mode, and 20 steps are executed. • FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio.	4.5 to 5.5		250	500	
	IDDCLOCK(2)			3.0 to 4.5		200	400	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

General-purpose I/O port "L" output when the above-mentioned data is measured

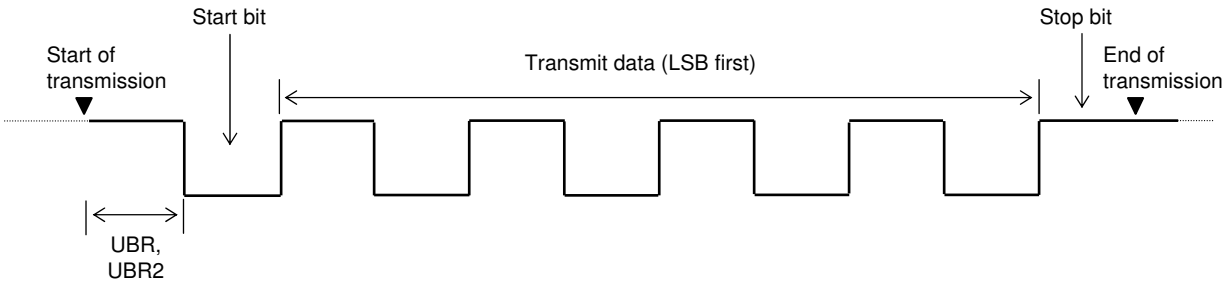
However, the P0 port is an input setting because of the mode setting

UART(Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}4 = AV_{SS} = 0V$

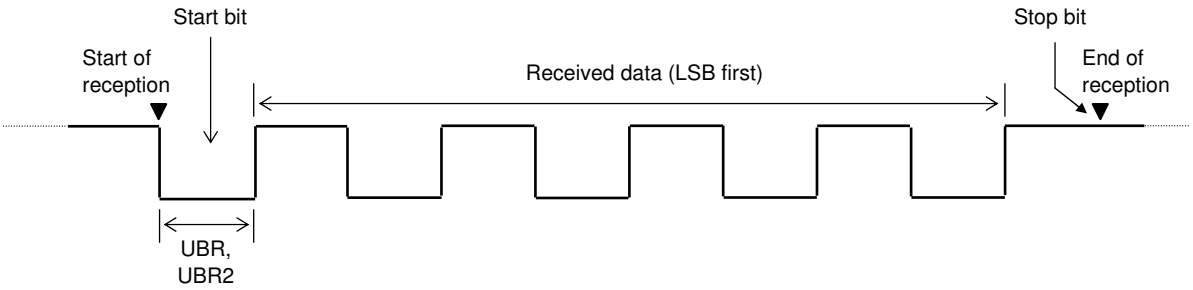
Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer clock rate	UBR, UBR2	UTX1(P32), RTX1(P33), UTX2(P34), RTX2(P35)		3.0 to 5.5	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: No

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



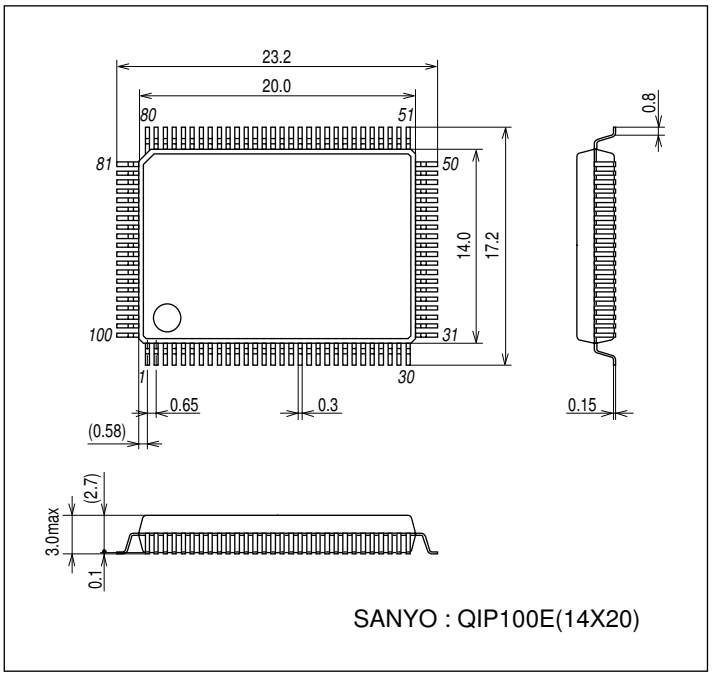
Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



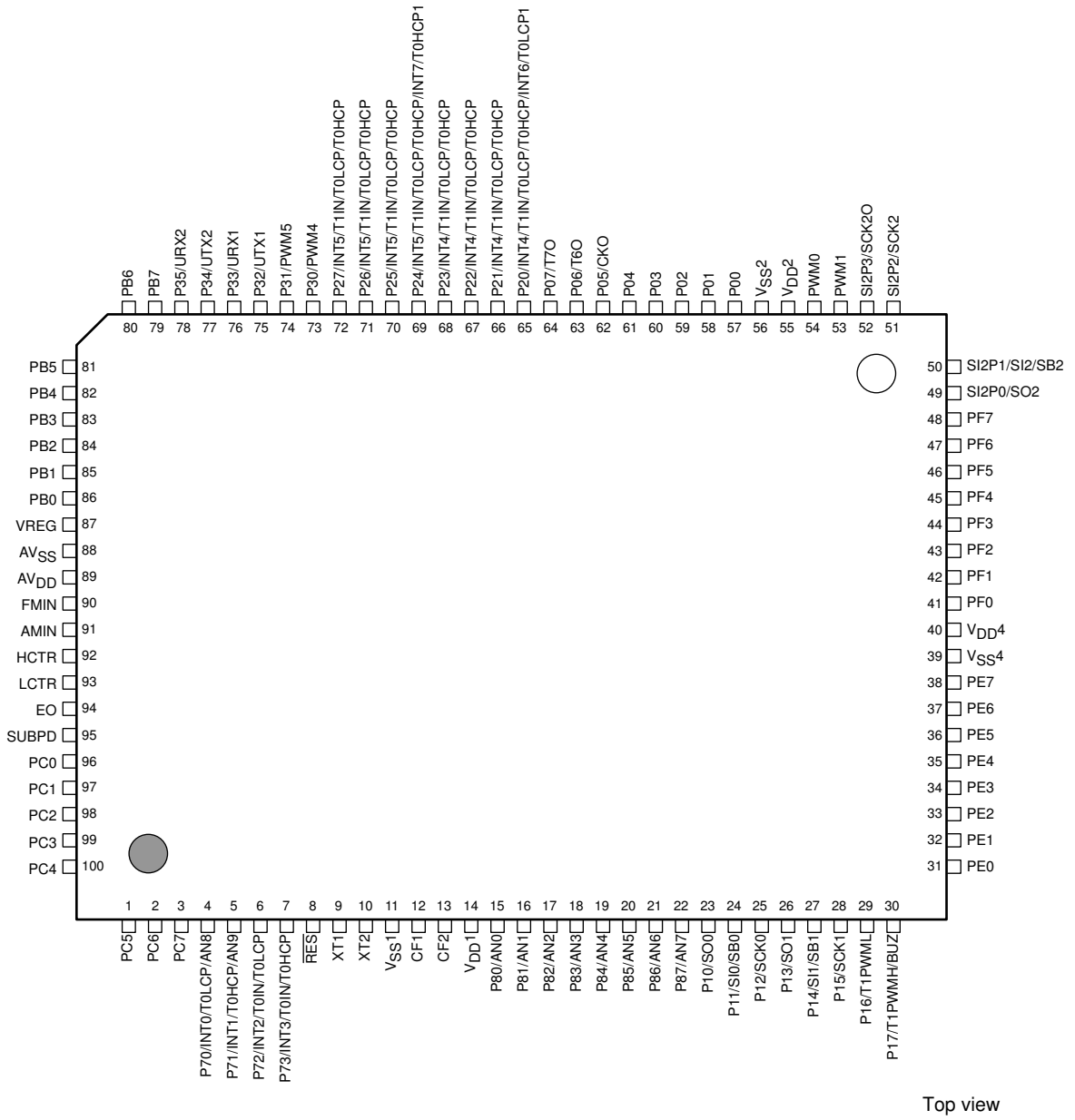
Package Dimensions

unit : mm (typ)

3151A



Pin Assignment



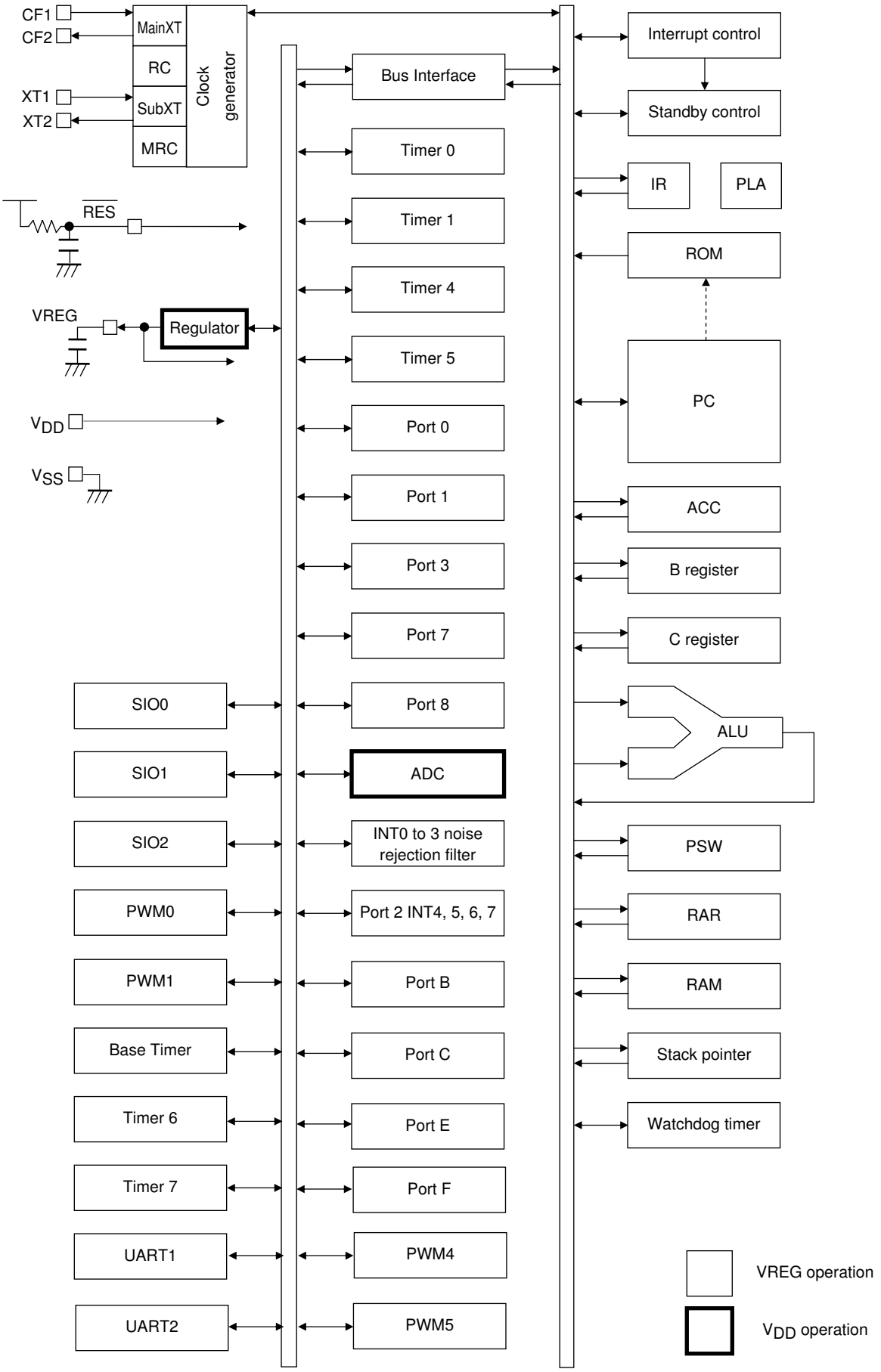
Top view

SANYO: QIP100E (Lead Free Product)

PIN No.	NAME
1	PC5
2	PC6
3	PC7
4	P70/INT0/T0LCP/AN8
5	P71/INT1/T0HCP/AN9
6	P72/INT2/T0IN/T0LCP
7	P73/INT3/T0IN/T0HCP
8	$\overline{RES}$
9	XT1
10	XT2
11	$V_{SS}1$
12	CF1
13	CF2
14	$V_{DD}1$
15	P80/AN0
16	P81/AN1
17	P82/AN2
18	P83/AN3
19	P84/AN4
20	P85/AN5
21	P86/AN6
22	P87/AN7
23	P10/SO0
24	P11/SI0/SB0
25	P12/SCK0
26	P13/SO1
27	P14/SI1/SB1
28	P15/SCK1
29	P16/T1PWML
30	P17/T1PWMH/BUZ
31	PE0
32	PE1
33	PE2
34	PE3
35	PE4
36	PE5
37	PE6
38	PE7
39	$V_{SS}4$
40	$V_{DD}4$
41	PF0
42	PF1
43	PF2
44	PF3
45	PF4
46	PF5
47	PF6
48	PF7
49	SI2P0/SO2
50	SI2P1/SI2/SB2

PIN No.	NAME
51	SI2P2/SCK2
52	SI2P3/SCK2O
53	PWM1
54	PWM0
55	$V_{DD}2$
56	$V_{SS}2$
57	P00
58	P01
59	P02
60	P03
61	P04
62	P05/CKO
63	P06/T6O
64	P07/T7O
65	P20/INT4/T1IN/T0LCP/T0HCP/INT6/T0LCP1
66	P21/INT4/T1IN/T0LCP/T0HCP
67	P22/INT4/T1IN/T0LCP/T0HCP
68	P23/INT4/T1IN/T0LCP/T0HCP
69	P24/INT5/T1IN/T0LCP/T0HCP/INT7/T0HCP1
70	P25/INT5/T1IN/T0LCP/T0HCP
71	P26/INT5/T1IN/T0LCP/T0HCP
72	P27/INT5/T1IN/T0LCP/T0HCP
73	P30/PWM4
74	P31/PWM5
75	P32/UTX1
76	P33/URX1
77	P34/UTX2
78	P35/URX2
79	PB7
80	PB6
81	PB5
82	PB4
83	PB3
84	PB2
85	PB1
86	PB0
87	VREG
88	AV_{SS}
89	AV_{DD}
90	FMIN
91	AMIN
92	HCTR
93	LCTR
94	EO
95	SUBPD
96	PC0
97	PC1
98	PC2
99	PC3
100	PC4

System Block Diagram



Pin Description

<table>
<tr><th>Name</th><th>Pin No.</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$
$V_{SS}2$
$V_{SS}4$
AV_{SS}</td><td>11
56
39
88</td><td>-</td><td>• Power supply pin
• Connect it with GND</td><td>No</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}4$
AV_{DD}</td><td>14
55
40
89</td><td>-</td><td>• Power supply pin
• Connect it with V_{DD}</td><td>No</td></tr>
<tr><td>Port 0
P00
P01
P02
P03
P04
P05
P06
P07</td><td>
57
58
59
60
61
62
63
64</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistor can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Other functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10
P11
P12
P13
P14
P15
P16
P17</td><td>
23
24
25
26
27
28
29
30</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P10: SIO0 data output
P11: SIO0 data input, bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input, bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output
P17: Timer 1 PWMH output, beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20
P21
P22
P23
P24
P25
P26
P27</td><td>
65
66
67
68
69
70
71
72</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P20: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT6 input/timer 0L capture 1 input
P21 to P23: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/
timer 0H capture input
P24: INT5 input/HOLD release input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT7 input/timer 0H capture 1 input
P25 to P27: INT5 input/HOLD release input/timer 1 event input/timer0L capture input/
timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>INT5</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>INT6</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>INT7</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30
P31
P32
P33
P34
P35</td><td>
73
74
75
76
77
78</td><td>I/O</td><td>• 6-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P30: PWM4 output
P31: PWM5 output
P32: UART1 transmit
P33: UART1 receive
P34: UART2 transmit
P35: UART2 receive</td><td>Yes</td></tr>
</table>

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<table>
<tr><th>Name</th><th>Pin No.</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>Port 7
P70
P71
P72
P73</td><td>
4
5
6
7</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer/ AD converter input port
P71: INT1 input/HOLD release input/Timer 0H capture input/ AD converter input port
P72: INT2 input/HOLD release input/Timer 0 event input/timer0L capture input
P73: INT3 input with noise filter/Timer 0 event input/timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Y</td><td>Y</td><td>N</td><td>Y</td><td>Y</td></tr>
<tr><td>INT1</td><td>Y</td><td>Y</td><td>N</td><td>Y</td><td>Y</td></tr>
<tr><td>INT2</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>INT3</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
</table>
</td><td>No</td></tr>
<tr><td>Port 8
P80
P81
P82
P83
P84
P85
P86
P87</td><td>
15
16
17
18
19
20
21
22</td><td>I/O</td><td>• 8-bit I/O port (Output: N-channel open drain)
• I/O specifiable in 1-bit units
• Other functions
P80 to P87: AD converter input port</td><td>No</td></tr>
<tr><td>Port B
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7</td><td>
86
85
84
83
82
81
80
79</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port C
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7</td><td>
96
97
98
99
100
1
2
3</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port E
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7</td><td>
31
32
33
34
35
36
37
38</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 2-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
<tr><td>Port F
PF0
PF1
PF2
PF3
PF4
PF5
PF6
PF7</td><td>
41
42
43
44
45
46
47
48</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 2-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
</table>

Continued on next page.

Continued from preceding page.

Name	Pin No.	I/O	Function Description	Option
SIO2 SI2P0 SI2P1 SI2P2 SI2P3	 49 50 51 52	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Other functions: SI2P0: SIO2 data output SI2P1: SIO2 data input, bus input/output SI2P2: SIO2 clock input/output SI2P3: SIO2 clock output	No
PWM0	54	I/O	• PWM0 output port • General-purpose I/O available	No
PWM1	53	I/O	• PWM1 output port • General-purpose I/O available	No
$\overline{RES}$	8	I	• Reset pin Must connect it with $V_{DD}1$ through RC (Refer to Page27 Figure 1)	No
XT1	9	I	• Input terminal for 32.768kHz X'tal oscillation • Other functions: General-purpose input port Must be set for input with software and connected to $V_{SS}1$ if not to be used.	No
XT2	10	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other functions: General-purpose I/O port Must be set for general-purpose output and kept open if not to be used. Please connect suitable dumping resistance for the crystal used between the terminal when you use it as Output terminal for 32.768kHz X'tal oscillation.	No
CF1	12	I	• Input terminal for 13.5MHz X'tal oscillation	No
CF2	13	O	• Output terminal for 13.5MHz X'tal oscillation	No
EO	94	O	• Output terminal for main charge pump	No
SUBPD	95	O	• Output terminal for sub charge pump	No
FMIN	90	I	• Input terminal for FM VCO (local oscillator) • The signal input to this pin must be capacitor coupled (Note.1) • Input frequency: 10 to 150MHz Please open the terminal when you do not use this terminal. Moreover, please make the pull-down of this terminal effective with software.	No
AMIN	91	I	• Input terminal for AM VCO (local oscillator) • The signal input to this pin must be capacitor coupled (Note.1) • Input frequency: 0.5 to 40MHz Please open the terminal when you do not use this terminal. Moreover, please make the pull-down of this terminal effective with software.	No
HCTR	92	I	• Input terminal for Universal counter • The signal input to this pin must be capacitor coupled (Note.1) • Input frequency: 0.4 to 12MHz Please open the terminal when you do not use this terminal. Moreover, please make the pull-down of this terminal effective with software.	No
LCTR	93	I	• Input terminal for Universal counter • The signal input to this pin must be capacitor coupled (Note.1) • Input frequency: 100 to 500kHz Please open the terminal when you do not use this terminal. Moreover, please make the pull-down of this terminal effective with software.	No
VREG	87	O	• Internal low voltage output • Connect a bypass capacitor to this pin. (Refer to Page27)	No

Note.1: Put the coupling capacitor near the terminal. About 100pF of capacity is preferable.
Especially, adjust the capacity of HCTR and LCTR to 1000pF or less.

Port Output Configuration

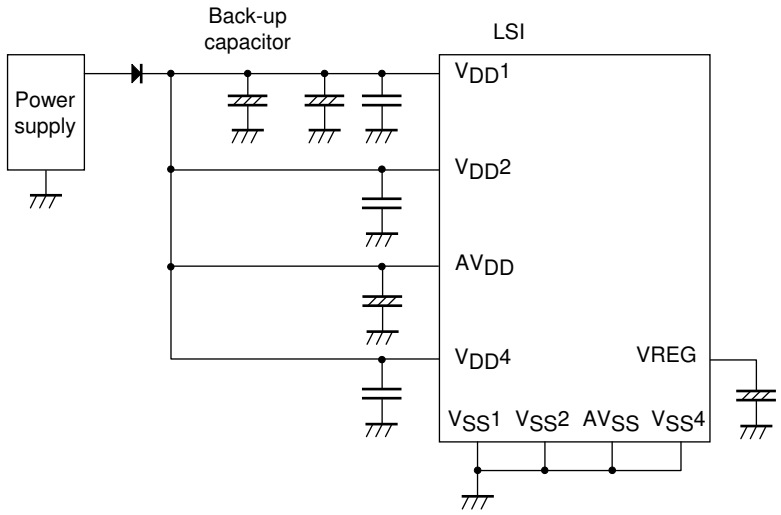
The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port	Options selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17 P20 to P27 P30 to P35	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PB0 to PB7 PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PE0 to PE7 PF0 to PF7	-	No	CMOS	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
SI2P0, SI2P2, SI2P3 PWM0, PWM1	-	No	CMOS	No
SI2P1	-	No	CMOS (when selected as ordinary port) N-channel open drain (When SIO2 data is selected)	No
FMIN, AMIN, HCTR, LCTR	-	No	Input only	No
EO, SUBPD	-	No	Output only	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz quartz oscillator N-channel open drain (when in general-purpose output mode)	No

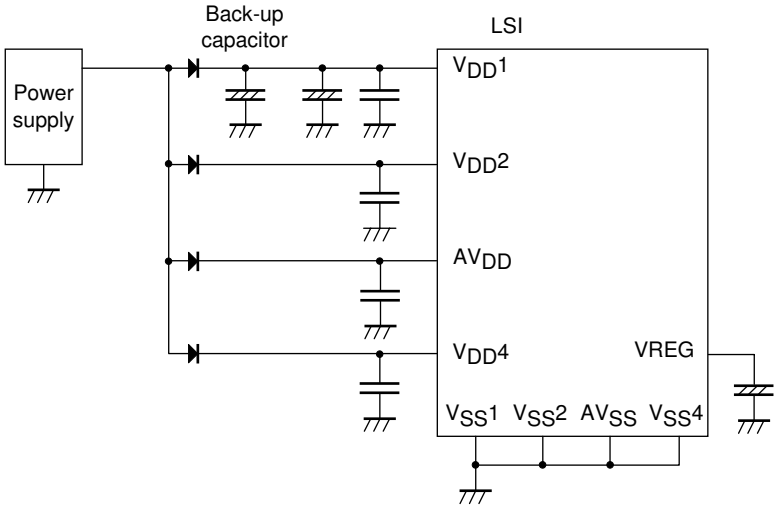
Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

*1: Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, AV_{SS} and $V_{SS}4$ pins.

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



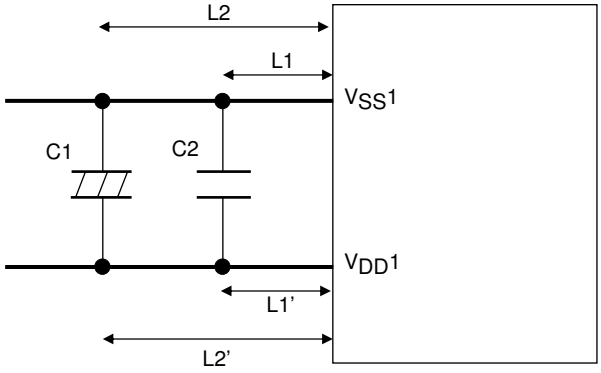
(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



$V_{DD}1$, $V_{SS}1$ Terminal condition

It is necessary to place capacitors between $V_{DD}1$ and $V_{SS}1$ as describe below.

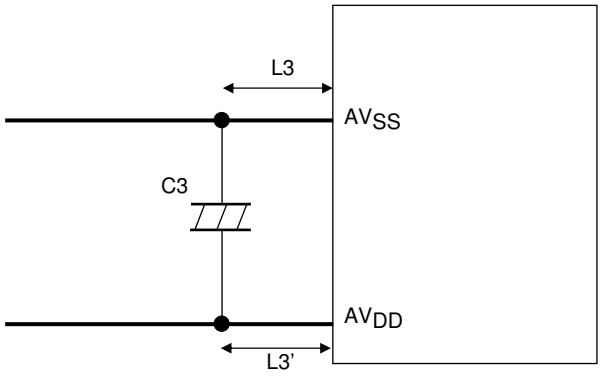
- Place capacitors as close to $V_{DD}1$ and $V_{SS}1$ as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than 0.1µF.
- Please mount a suitable capacitor about C1.
- Use thicker pattern for $V_{DD}1$ and $V_{SS}1$.



AV_{DD}, AV_{SS} Terminal condition

It is necessary to place capacitors between AV_{DD} and AV_{SS} as describe below.

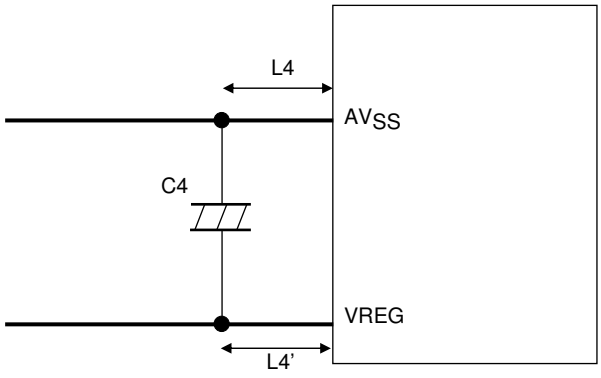
- Place capacitors as close to AV_{DD} and AV_{SS} as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L3 = L3').
- Capacitance of C3 must be more than 1µF.
- Use thicker pattern for AV_{DD} and AV_{SS}.



VREG, AV_{SS} Terminal condition

It is necessary to place capacitors between VREG and AV_{SS} as describe below.

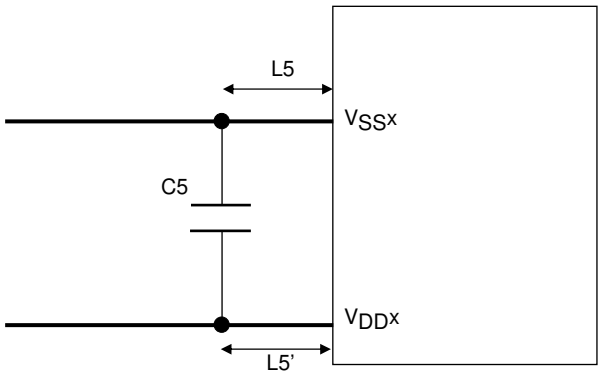
- Place capacitors as close to VREG and AV_{SS} as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L4 = L4').
- Capacitance of C4 must be more than 1μF to 10μF.
- Use thicker pattern for VREG and AV_{SS}.

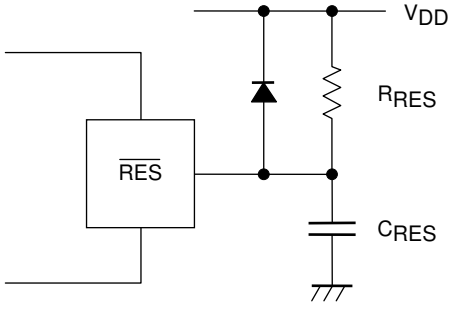


$V_{DD}x$, $V_{SS}x$ Terminal condition x=2, 4

It is necessary to place capacitors between $V_{DD}x$ and $V_{SS}x$ as describe below.

- Place capacitors as close to $V_{DD}x$ and $V_{SS}x$ as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L5 = L5').
- Capacitance of C5 must be more than 0.1μF.
- Use thicker pattern for $V_{DD}x$ and $V_{SS}x$.





(Note) Select C_{RES} and R_{RES} value to assure that reset is generated after the V_{DD} becomes higher than the minimum operating voltage.

Recommended value
C_{RES}: 0.47μF
R_{RES}: 270kΩ

Figure 1 Reset circuit

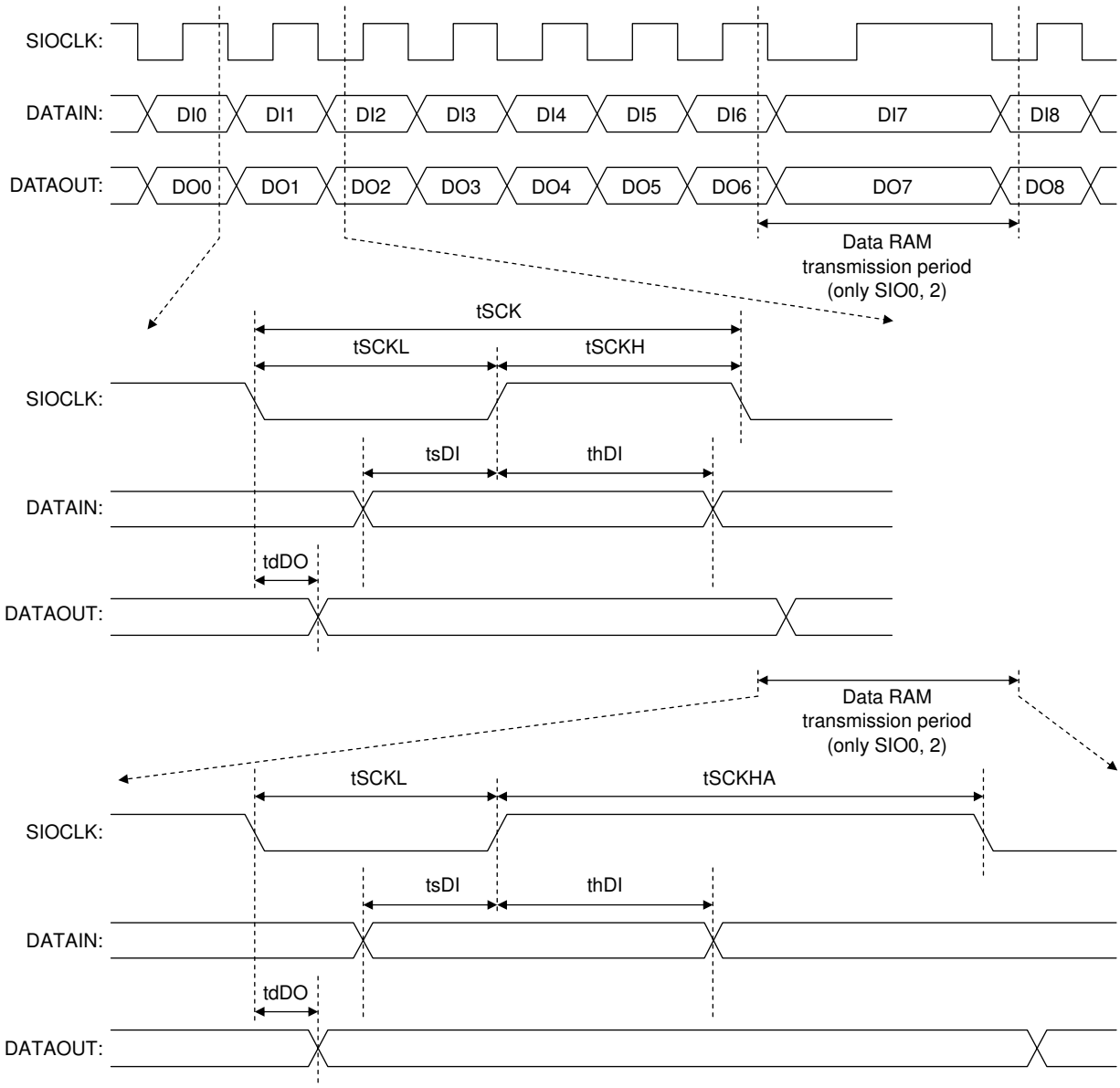


Figure 2 Serial input/output test condition

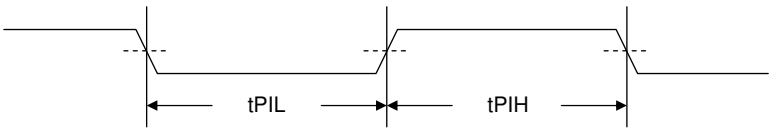


Figure 3 Pulse input timing condition