Ordering number : ENA1067

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

TIG067SS — N-Channel IGBT Light-Controlling Flash Applications

Features

- Low-saturation voltage
- Enhansment type
- High speed switching
- 4.0V drive
- Built-in Gate-to-Emitter protection diode
- Halogen free compliance

Specifications

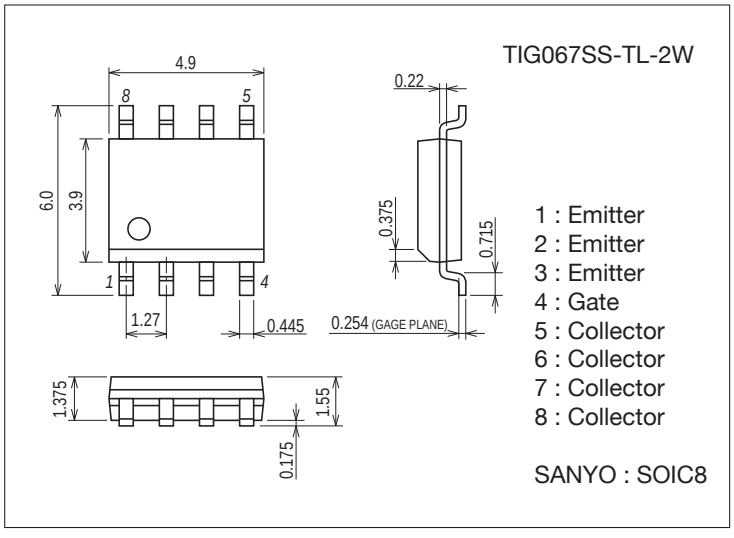
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Emitter Voltage (DC)	V_{CES}		400	V
Collector-to-Emitter Voltage (Pulse)	V_{CESP}	PW≤1ms	450	V
Gate-to-Emitter Voltage (DC)	V_{GES}		±6	V
Gate-to-Emitter Voltage (Pulse)	V_{GESP}	PW≤1ms	±8	V
Collector Current (Pulse)	I_{CP}	C_M=600μF	150	A
Maximum Collector-to-Emitter dv / dt	dv / dt	V_{CE}≤320V, starting Tch=25°C	1500	V / μs
Allowable Power Dissipation	P_D	When mounted on FR4 substrate (11,680mm²×1.6mm)	1.2	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-40 to +150	°C

Package Dimensions

unit : mm (typ)

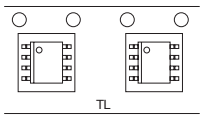
7072-002



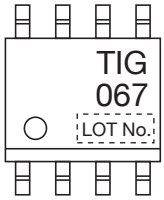
Product & Package Information

- Package : SOIC8
- JEITA, JEDEC : SC-87, SOT-96
- Minimum Packing Quantity : 2500 pcs./reel

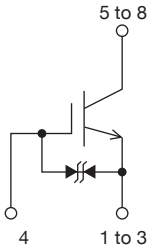
Packing Type: TL



Marking



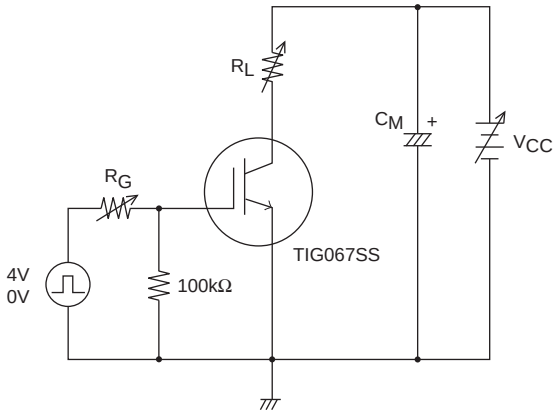
Electrical Connection



Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C=2mA, V_{GE}=0V	400			V
Collector-to-Emitter Cutoff Current	I_{CES}	V_{CE}=320V, V_{GE}=0V			10	μA
Gate-to-Emitter Leakage Current	I_{GES}	V_{GE}=±6V, V_{CE}=0V			±10	μA
Gate-to-Emitter Threshold Voltage	$V_{GE(off)}$	V_{CE}=10V, I_C=1mA	0.4		1.0	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=150A, V_{GE}=4V		3.8	5	V
Input Capacitance	Cies	V_{CE}=10V, f=1MHz		5100		pF
Output Capacitance	Coes			59		pF
Reverse Transfer Capacitance	Cres			43		pF
Fall Time	t_f	I_C=150A, V_{CC}=320V, Resistor load V_{GE}=4V, R_G=36Ω		270		ns

Fig1 Large Current R Load Switching Circuit

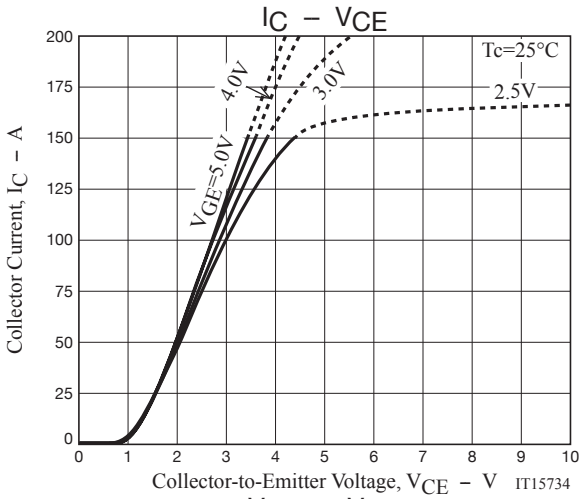


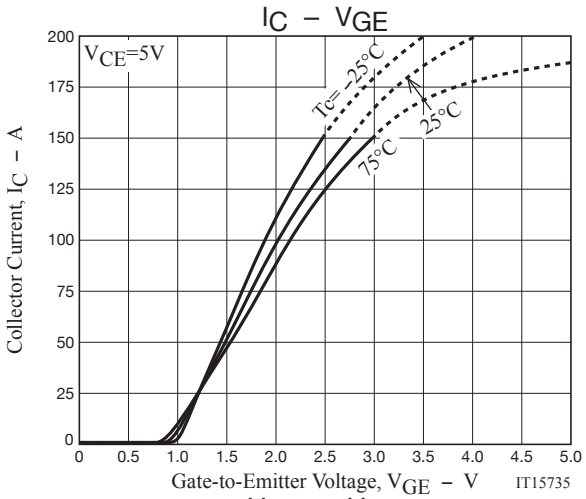
Note1. Gate Series Resistance $R_G \geq 36\Omega$ is recommended for protection purpose at the time of turn OFF. However, if dv / dt ≤ 1500 / μs is satisfied at customer's actual set evaluation, $R_G < 36\Omega$ can also be used.

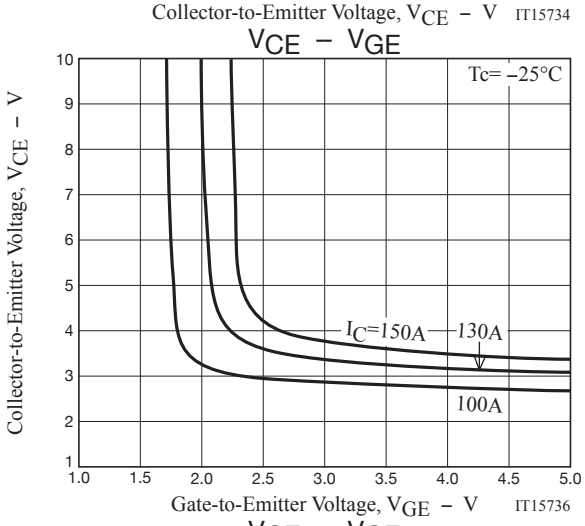
Note2. The collector voltage gradient dv / dt must be smaller than 1500V / μs to protect the device when it is turned off.

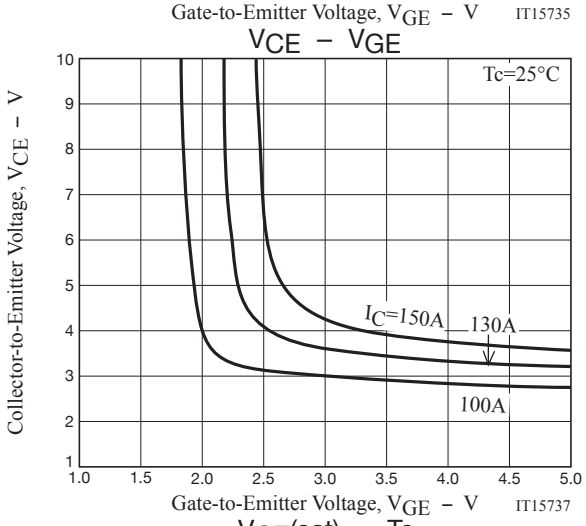
Ordering Information

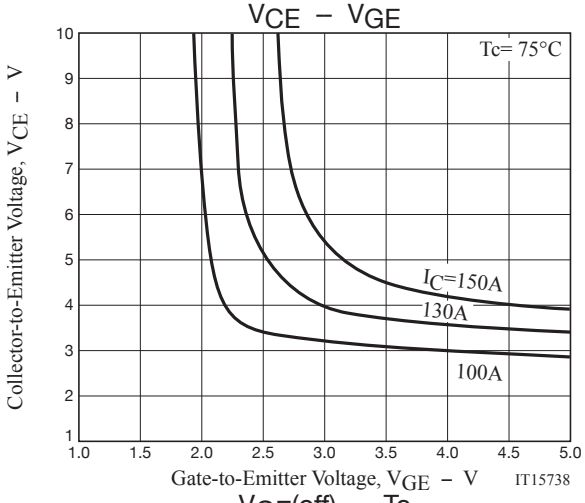
Device	Package	Shipping	memo
TIG067SS-TL-2W	SOIC8	2,500pcs./reel	Pb Free and Halogen Free

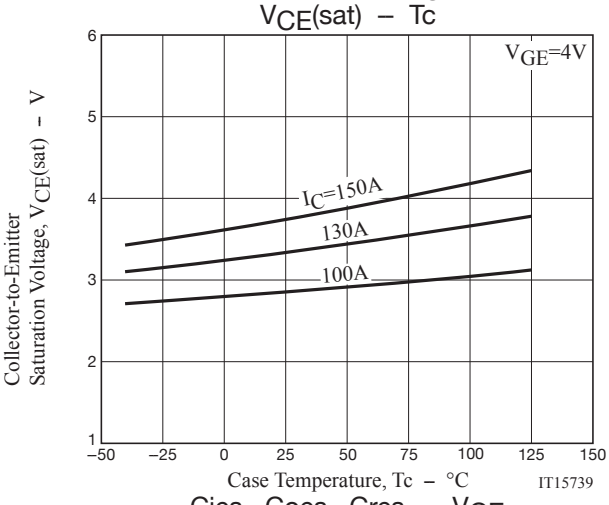

IC – VCE
Tc=25°C
2.5V
3.0V
4.0V
VGE=5.0V
Collector Current, IC – A
Collector-to-Emitter Voltage, VCE – V
IT15734

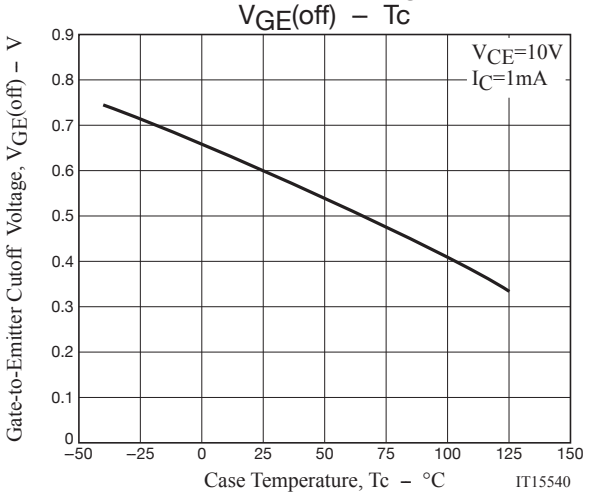

IC – VGE
VCE=5V
Tc=–25°C
25°C
75°C
Collector Current, IC – A
Gate-to-Emitter Voltage, VGE – V
IT15735

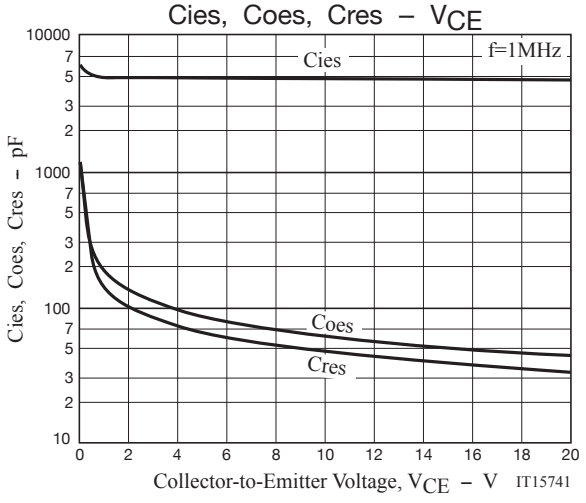

VCE – VGE
Tc= –25°C
IC=150A
130A
100A
Collector-to-Emitter Voltage, VCE – V
Gate-to-Emitter Voltage, VGE – V
IT15736


VCE – VGE
Tc=25°C
IC=150A
130A
100A
Collector-to-Emitter Voltage, VCE – V
Gate-to-Emitter Voltage, VGE – V
IT15737

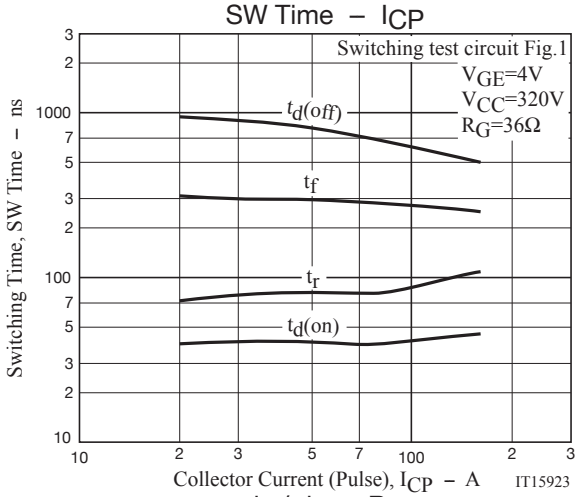

VCE – VGE
Tc= 75°C
IC=150A
130A
100A
Collector-to-Emitter Voltage, VCE – V
Gate-to-Emitter Voltage, VGE – V
IT15738


VCE(sat) – Tc
VGE=4V
IC=150A
130A
100A
Collector-to-Emitter Saturation Voltage, VCE(sat) – V
Case Temperature, Tc – °C
IT15739

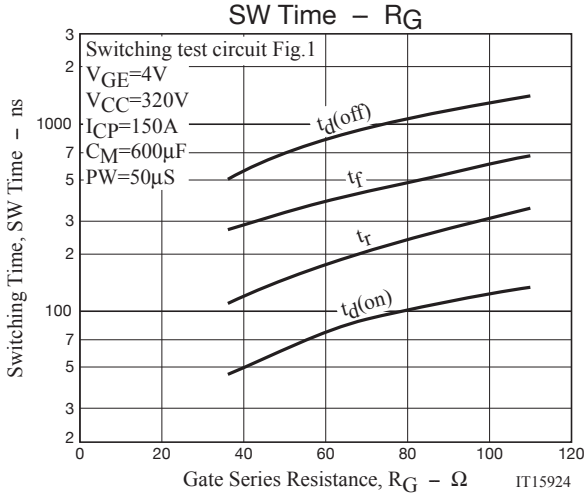

VGE(off) – Tc
VCE=10V
IC=1mA
Gate-to-Emitter Cutoff Voltage, VGE(off) – V
Case Temperature, Tc – °C
IT15540


Cies, Coes, Cres – VCE
f=1MHz
Cies
Coes
Cres
Cies, Coes, Cres – pF
Collector-to-Emitter Voltage, VCE – V
IT15741

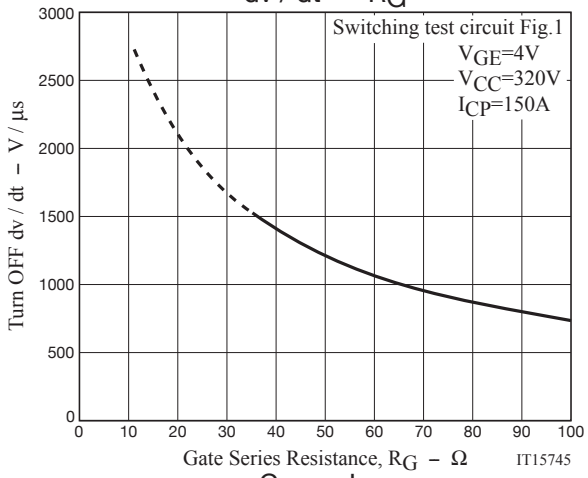
SW Time – I_{CP}



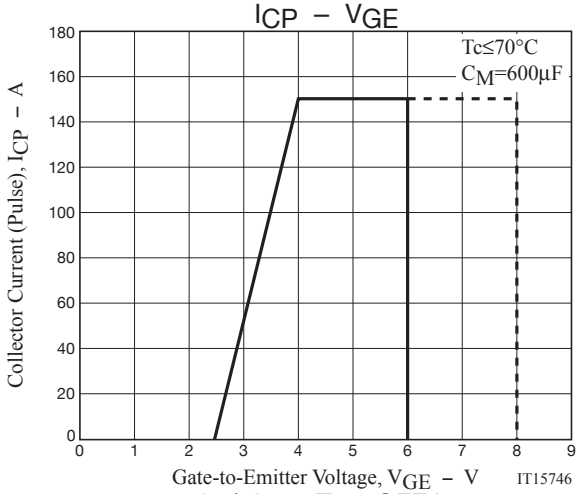
SW Time – R_G



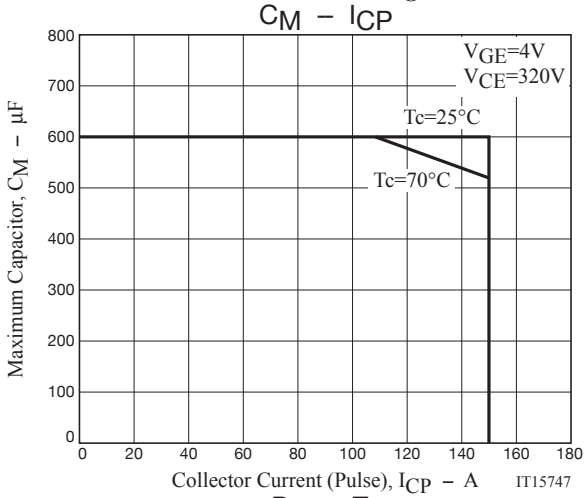
dv / dt – R_G



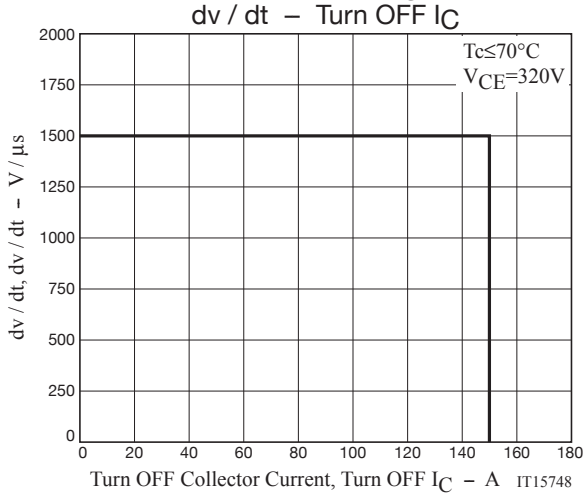
I_{CP} – V_{GE}



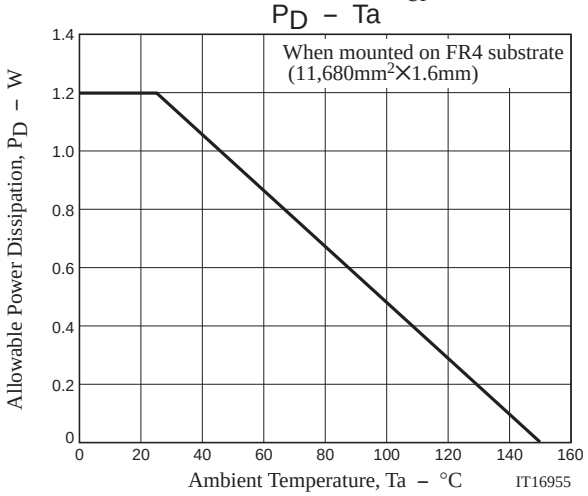
C_M – I_{CP}



dv / dt – Turn OFF I_C



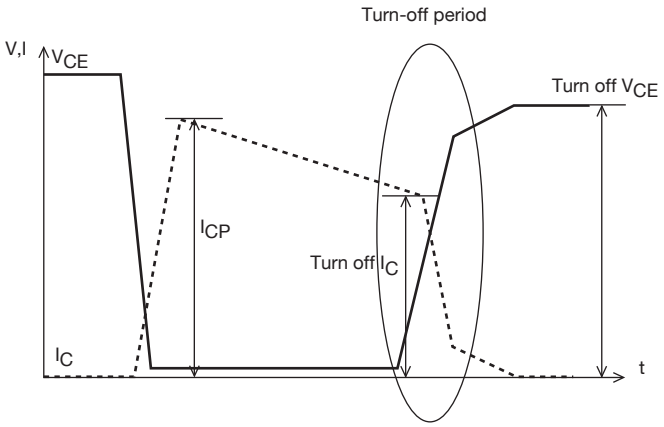
P_D – Ta



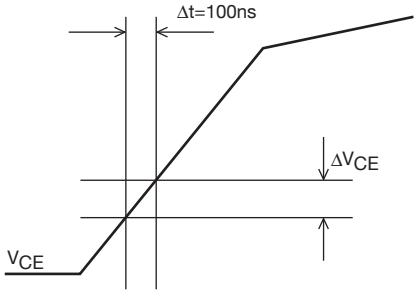
Definition of dv/dt

dv/dt is defined as the maximum slope of the below V_{CE} curve during turn-off period.
$dv/dt=\Delta V_{CE}/\Delta t=\Delta V_{CE}/100ns$

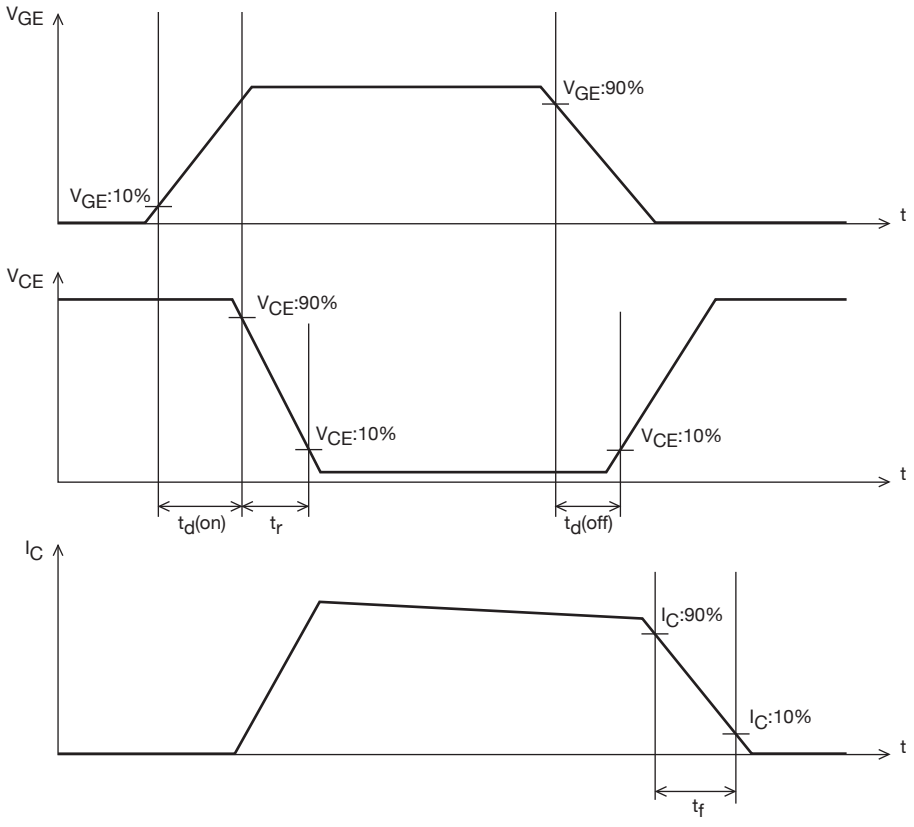
Overall waveform



Enlarged picture of turn-off period



Definition of Switching Time



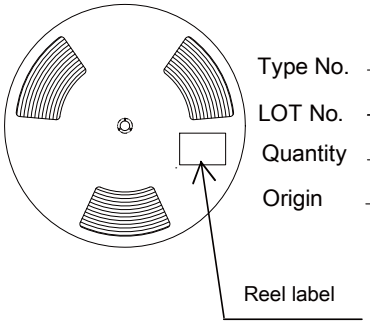
Taping Specification

TIG067SS-TL-2W

1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX W206-112	Outer BOX W207-124
SOIC8	B202-101	2,500	12,500	25,000	5 reels contained Dimensions :mm(external) 340×95×340	2 inner boxes contained Dimensions :mm(external) 360×210×375

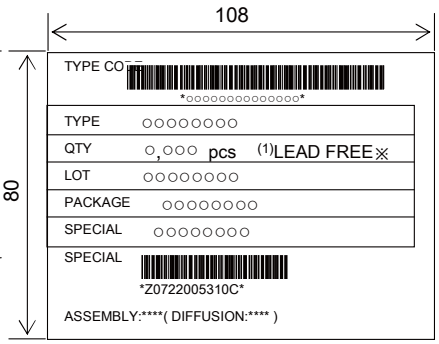
Packing method



Reel label,Inner box label
(unit: mm)

NOTE(1)
The LEAD FREE 4 description shows that it is complete lead free.

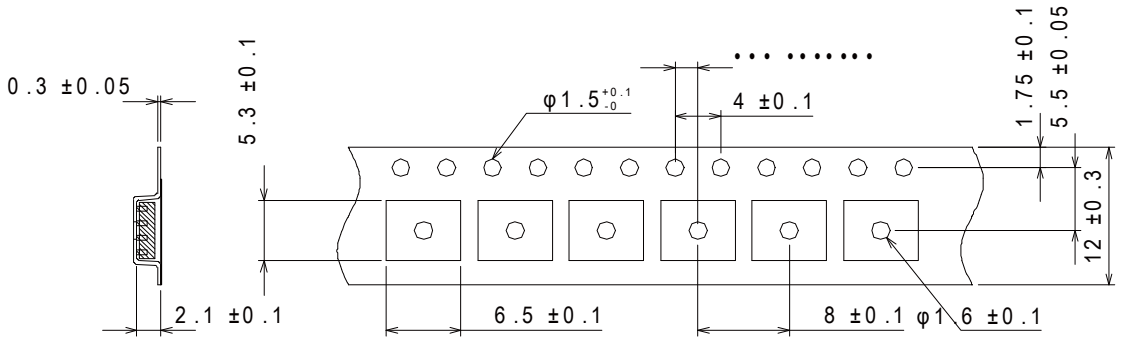
Outer box label
It is a label at the time of factory shipments.
The form of a label may change in physical distribution process.



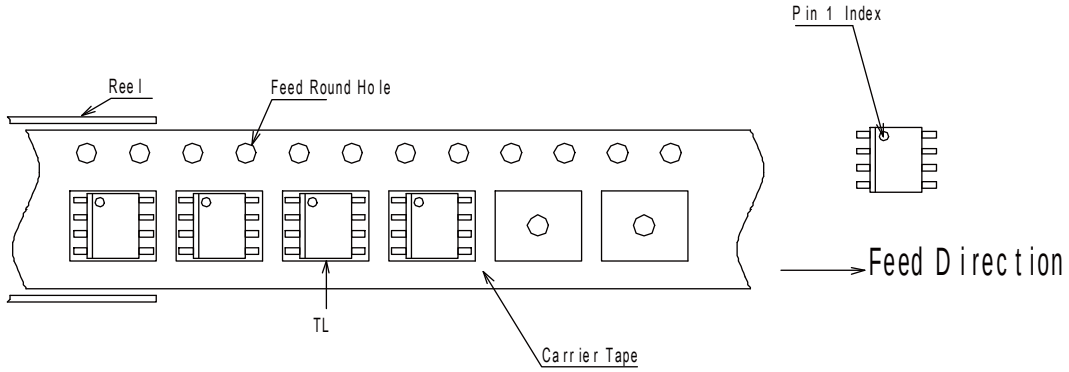
Label	JEITA Phase
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit: mm)

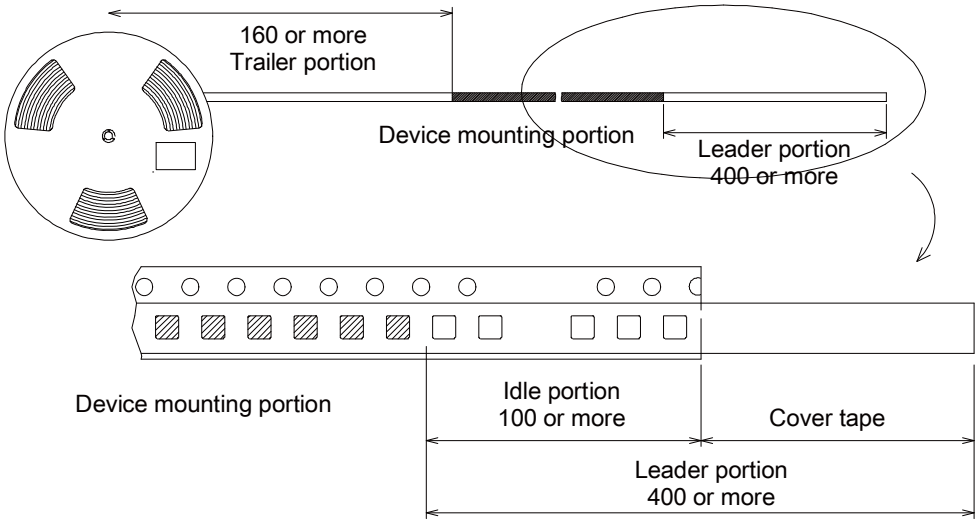


2-2. Device placement direction



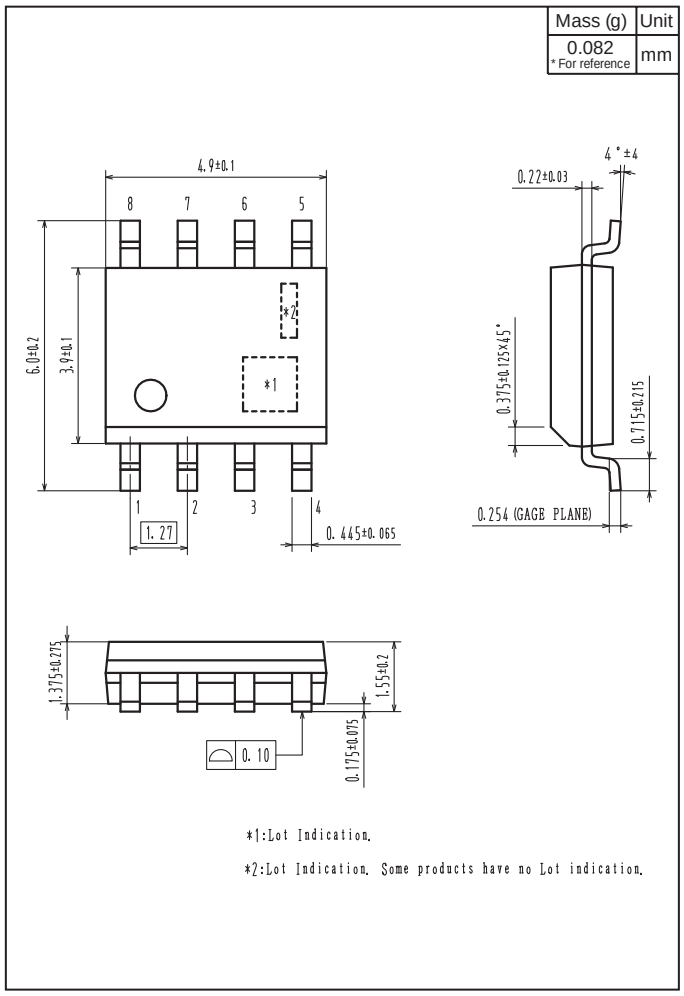
Packing type·····TL

2-3. Leader portion and trailer portion (unit: mm)

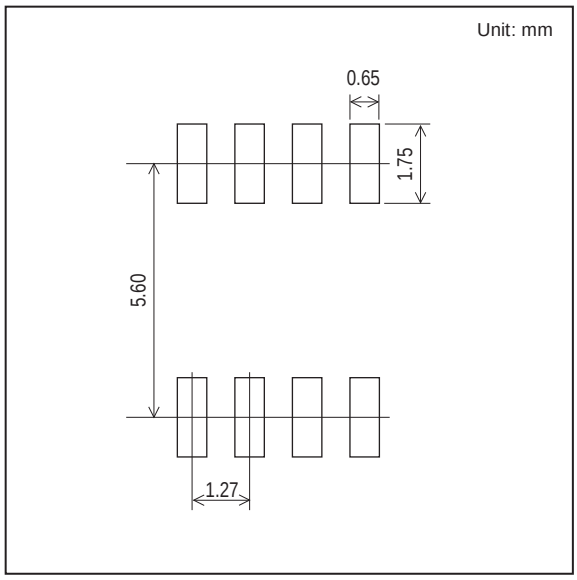


Outline Drawing

TIG067SS-TL-2W



Land Pattern Example



Note : TIG067SS has protection diode between gate and emitter but handling it requires sufficient care to be taken.

This catalog provides information as of October, 2012. Specifications and information herein are subject to change without notice.