Ordering number : ENA0747B

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

N-Channel Silicon MOSFET

2SK4125 — General-Purpose Switching Device Applications

Features

- ON-resistance $R_{DS}(on)$=0.47Ω (typ.)
- Input capacitance Ciss=1200pF (typ.)
- 10V drive

Specifications

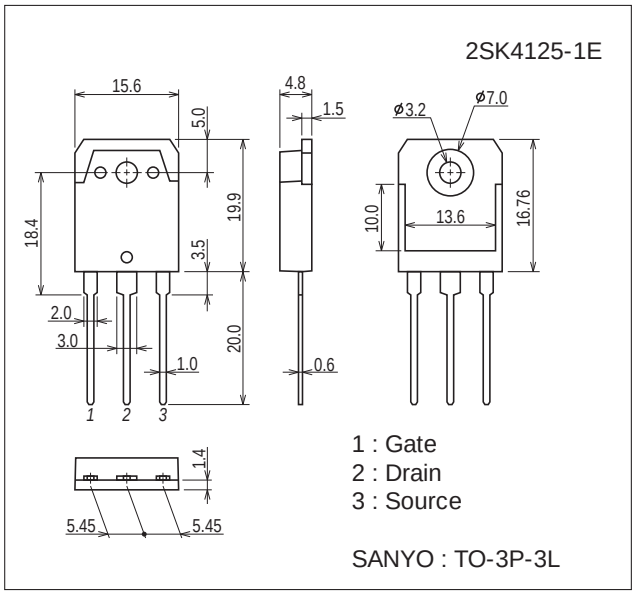
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		600	V
Gate-to-Source Voltage	V_{GSS}		±30	V
Drain Current (DC)	I_D		17	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	52	A
Allowable Power Dissipation	P_D		2.5	W
		Tc=25°C (SANYO's ideal heat dissipation condition)*1	170	W
Channel Temperature	Tch		150	℃
Storage Temperature	Tstg		−55 to +150	℃
Avalanche Energy (Single Pulse) *2	E_{AS}		78.8	mJ
Avalanche Current *3	I_{AV}		17	A

*1 SANYO's condition is radiation from backside.
The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminium.
*2 V_{DD}=50V, L=500μH, I_{AV}=17A (Fig.1)
*3 L≤500μH, single pulse

Package Dimensions

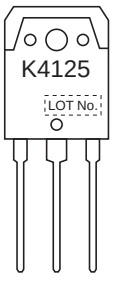
unit : mm (typ)
7539-002



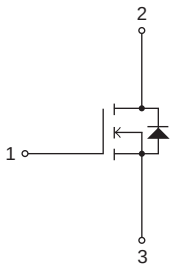
Product & Package Information

- Package : TO-3P-3L
- JEITA, JEDEC : SC-65, TO-247, SOT-199
- Minimum Packing Quantity : 30 pcs./magazine

Marking



Electrical Connection



Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0V	600			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=480V, V_{GS}=0V			100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V			±100	nA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=1mA	3		5	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=8.5A	4.5	9		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)	I_D=7A, V_{GS}=10V		0.47	0.61	Ω
Input Capacitance	Ciss	V_{DS}=30V, f=1MHz		1200		pF
Output Capacitance	Coss			220		pF
Reverse Transfer Capacitance	Crss			50		pF
Turn-ON Delay Time	t_d(on)	See Fig.2		26.5		ns
Rise Time	t_r			82		ns
Turn-OFF Delay Time	t_d(off)			145		ns
Fall Time	t_f			52		ns
Total Gate Charge	Qg	V_{DS}=200V, V_{GS}=10V, I_D=17A		46		nC
Gate-to-Source Charge	Qgs			8.3		nC
Gate-to-Drain "Miller" Charge	Qgd			26.7		nC
Diode Forward Voltage	V_{SD}	I_S=17A, V_{GS}=0V		1.0	1.3	V

Fig.1 Avalanche Resistance Test Circuit

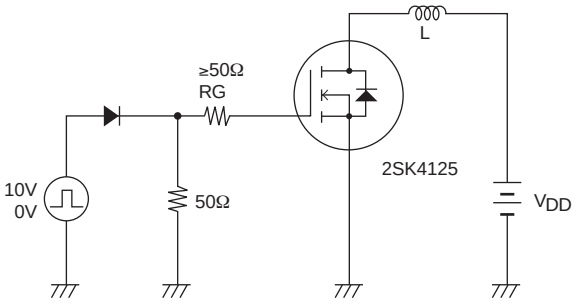
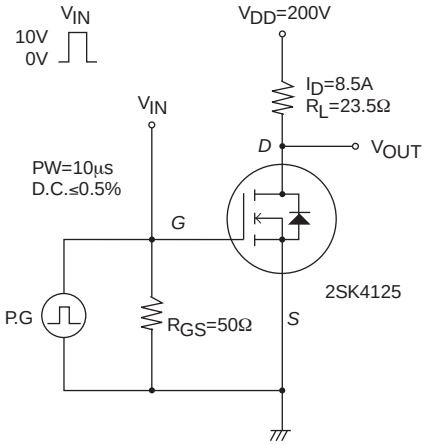
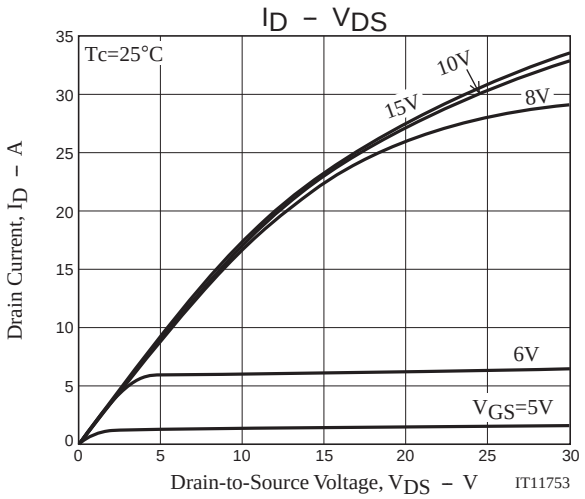


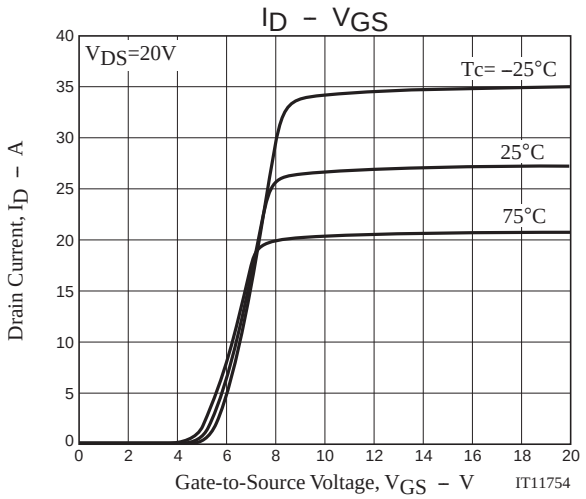
Fig.2 Switching Time Test Circuit



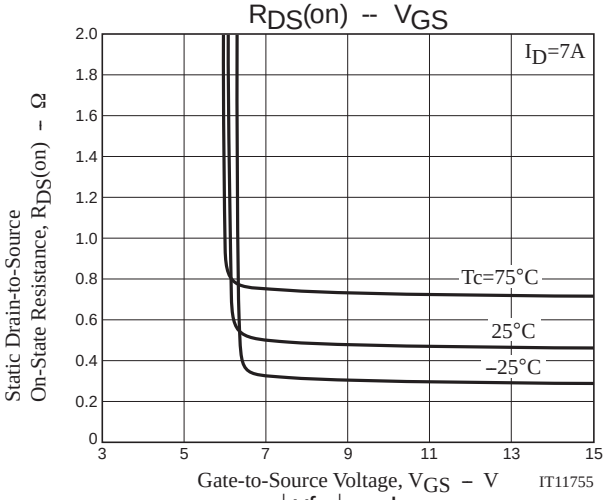
Ordering Information

Device	Package	Shipping	memo
2SK4125-1E	TO-3P-3L	30pcs./magazine	Pb Free

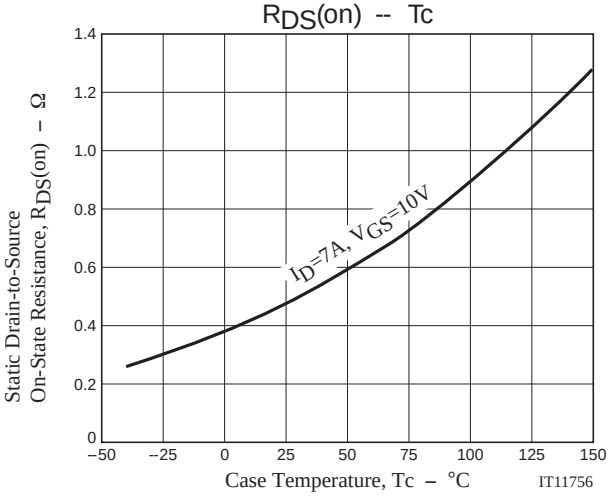




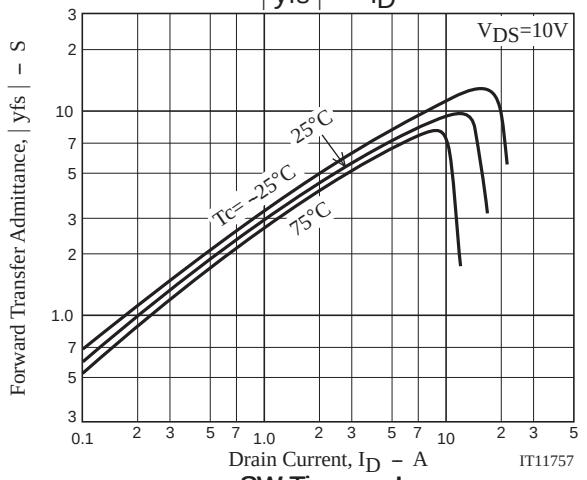
$R_{DS}(on)$ -- V_{GS}



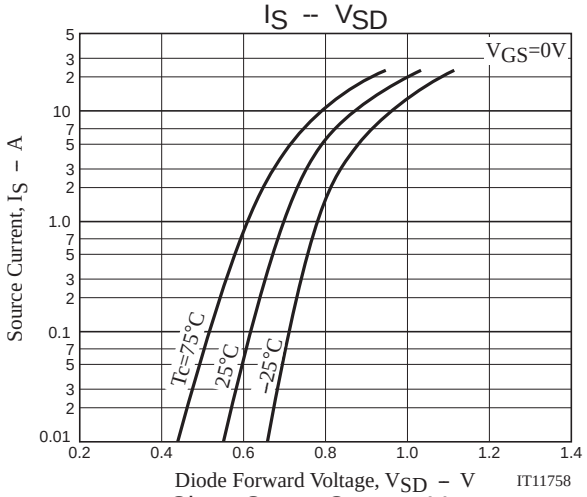
$R_{DS}(on)$ -- Tc



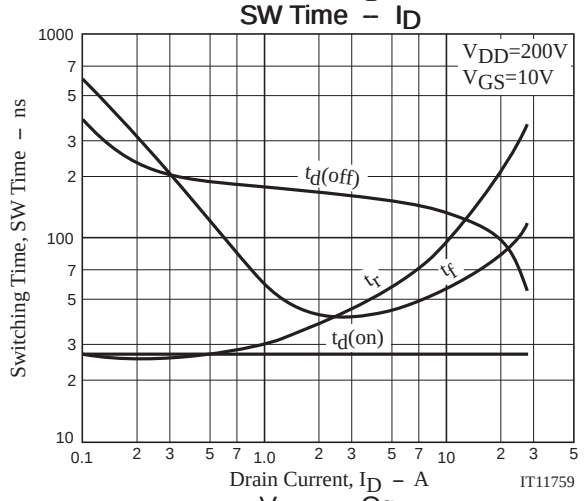
$|yfs|$ -- I_D



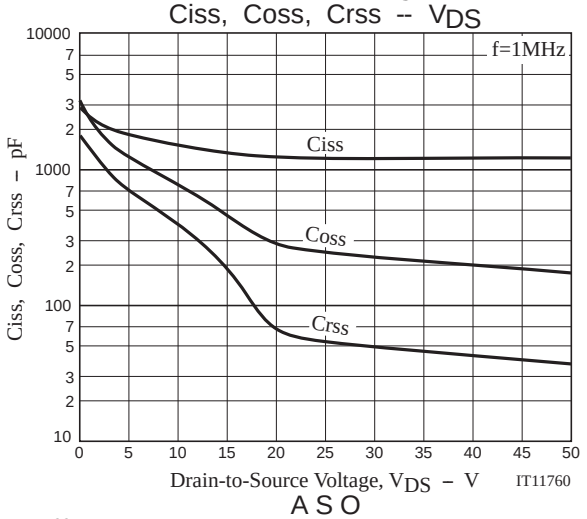
I_S -- V_{SD}



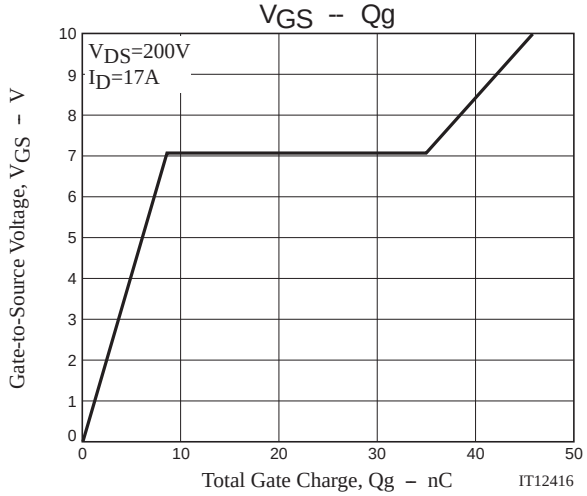
SW Time – I_D



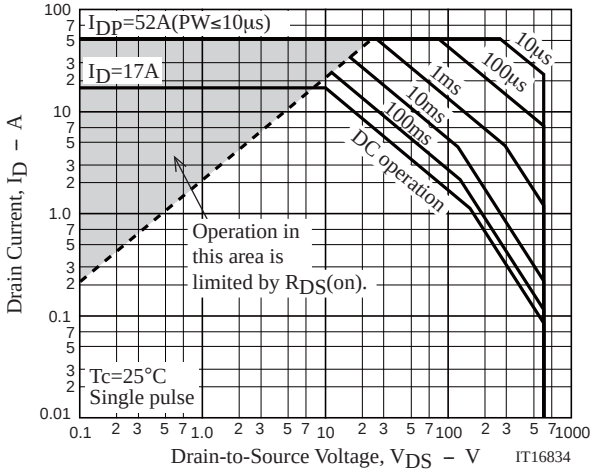
Ciss, Coss, Crss -- V_{DS}

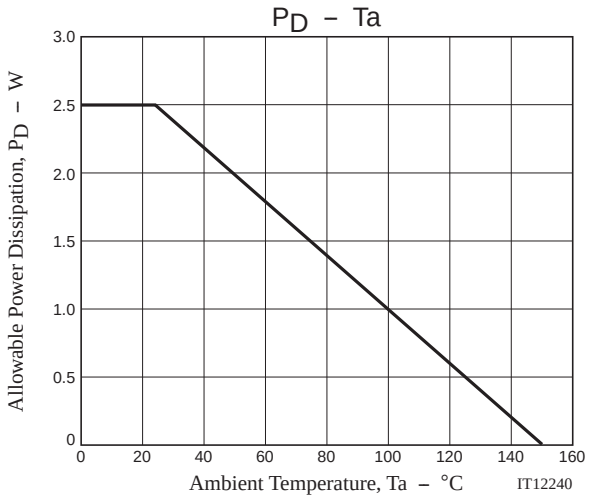


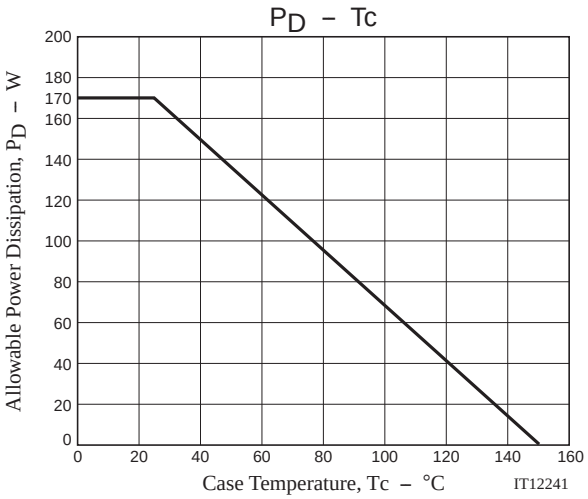
V_{GS} -- Qg

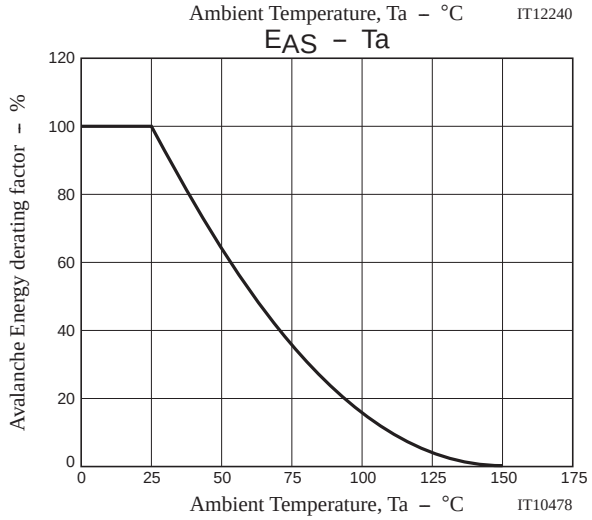


A S O




PD – Ta
Allowable Power Dissipation, PD – W
3.0
2.5
2.0
1.5
1.0
0.5
0
0 20 40 60 80 100 120 140 160
Ambient Temperature, Ta – °C
IT12240


PD – Tc
Allowable Power Dissipation, PD – W
200
180
170
160
140
120
100
80
60
40
20
0
0 20 40 60 80 100 120 140 160
Case Temperature, Tc – °C
IT12241


EAS – Ta
Avalanche Energy derating factor – %
120
100
80
60
40
20
0
0 25 50 75 100 125 150 175
Ambient Temperature, Ta – °C
IT10478

Magazine Specification

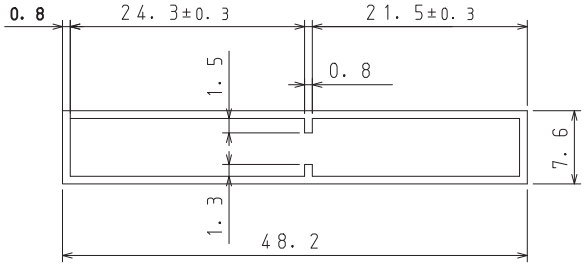
2SK4125-1E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			Packing format	
	Magazine	Inner box	Outer box	Inner BOX	Outer BOX
TO-3P-3L	30	450	1800	SPD-0V0001 15 magazines contained Dimensions:mm(external) 568×150×55	SPD-LV0010 4 inner boxes contained Dimensions:mm(external) 590x225x178

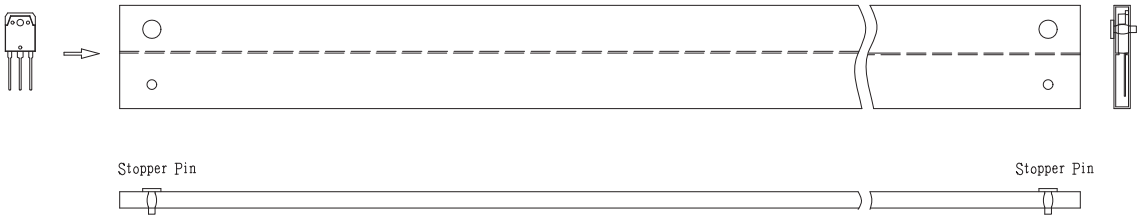
2. Magazine dimensions

(unit:mm)

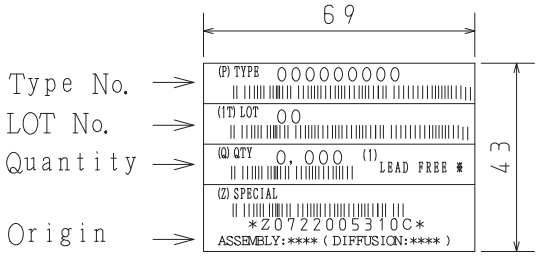


Tolerance=±0.2mm
Thickness=0.8±0.2mm
Length =508.0±1mm
Material =PVC or PET
(Antistatic treatment)

3. Storage method to magazine

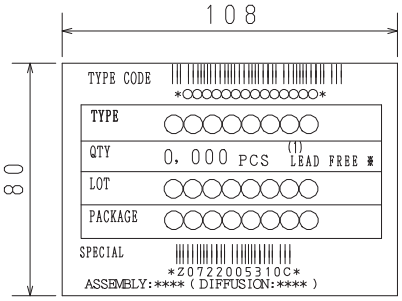


4. Inner box label (unit:mm)



5. Outer box label (unit:mm)

It is a label at the time of factory shipments.
The form of a label may change in physical distribution process.

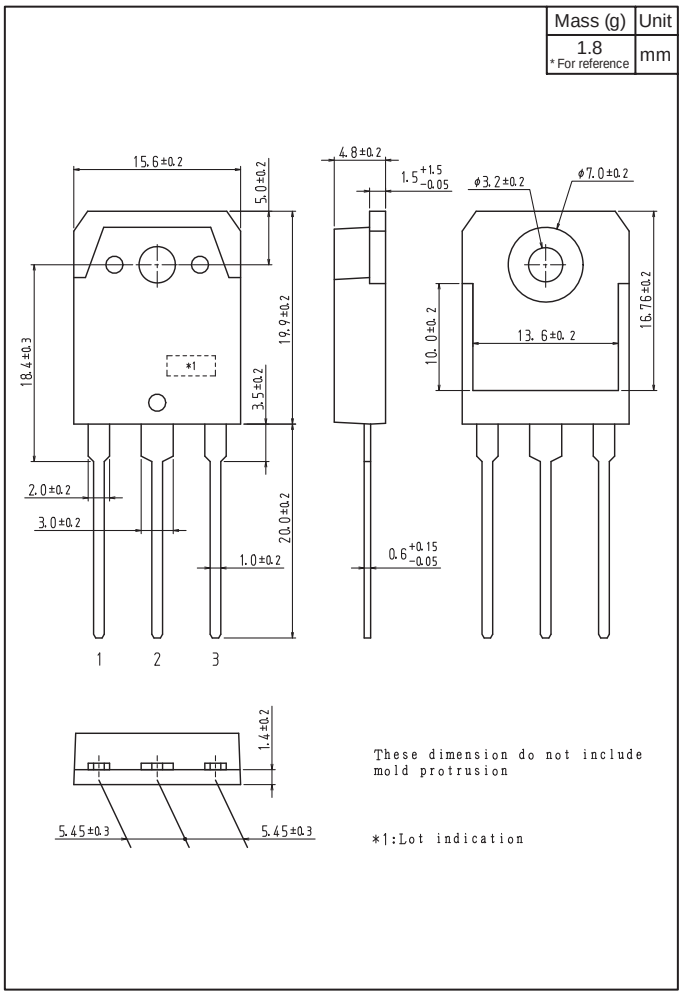


NOTE (1)
The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

Outline Drawing

2SK4125-1E



Note on usage : Since the 2SK4125 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

This catalog provides information as of June, 2012. Specifications and information herein are subject to change without notice.