Ordering number : EN3025A

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

2SA1705 — PNP Epitaxial Planar Silicon Transistor

Low-Frequency Power Amplifier Applications

Applicaitons

- Voltage regulators, relay drivers, lamp drivers

Features

- Adoption of FBET process
- Fast switching speed

Specifications

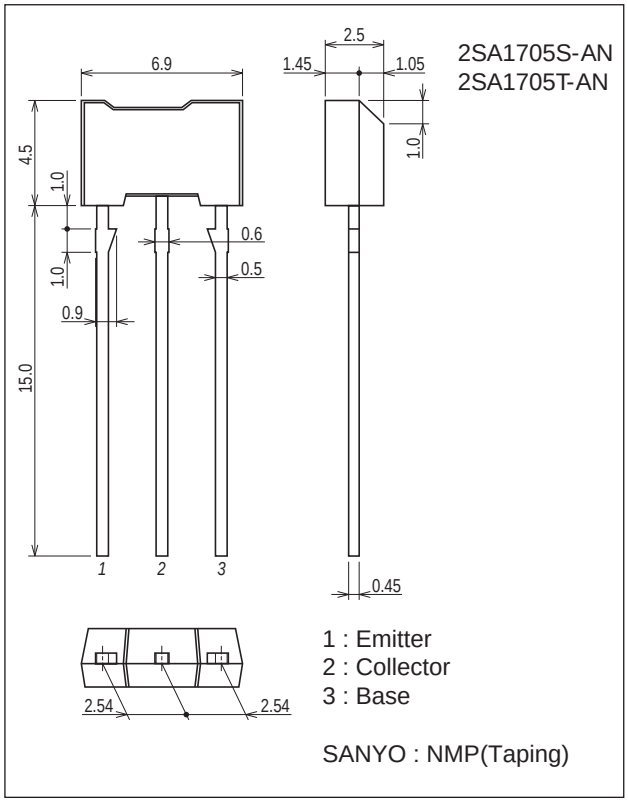
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		−60	V
Collector-to-Emitter Voltage	V_{CEO}		−50	V
Emitter-to-Base Voltage	V_{EBO}		−5	V
Collector Current	I_C		−1	A
Collector Current (Pulse)	I_{CP}		−2	A
Collector Dissipation	P_C		0.9	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Package Dimensions

unit : mm (typ)

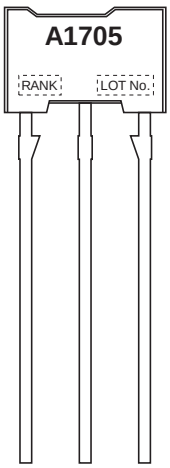
7540-001



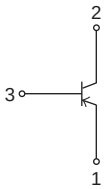
Product & Package Information

- Package : NMP(Taping)
- JEITA, JEDEC : SC-71
- Minimum Packing Quantity : 2,500 pcs./box

Marking(NMP(Taping))



Electrical Connection



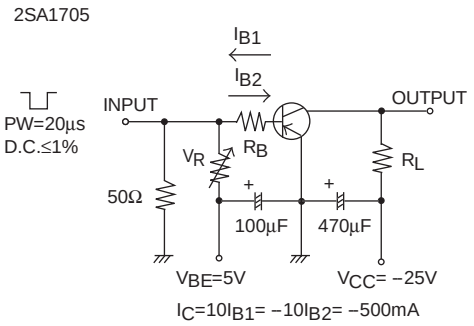
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=−50V, I_E=0A			−100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB}=−4V, I_C=0A			−100	nA
DC Current Gain	$h_{FE}1$	V_{CE}=−2V, I_C=−100mA	140*		400*	
	$h_{FE}2$	V_{CE}=−2V, I_C=−1A	30			
Gain-Bandwidth Product	f_T	V_{CE}=−10V, I_C=−50mA		150		MHz
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=−500mA, I_B=−50mA		−180	−500	mV
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=−500mA, I_B=−50mA		−0.9	−1.2	V
Output Capacitance	Cob	V_{CB}=−10V, f=1MHz		12		pF
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=−10μA, I_E=0A	−60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=−1mA, R_{BE}=∞	−50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=−10μA, I_C=0A	−5			V
Turn-ON Time	t_{on}	See specified Test Circuit.		40		ns
Storage Time	t_{stg}			300		ns
Fall Time	t_f			30		ns

* : The 2SA1705 is classified by 100mA h_{FE} as follows :

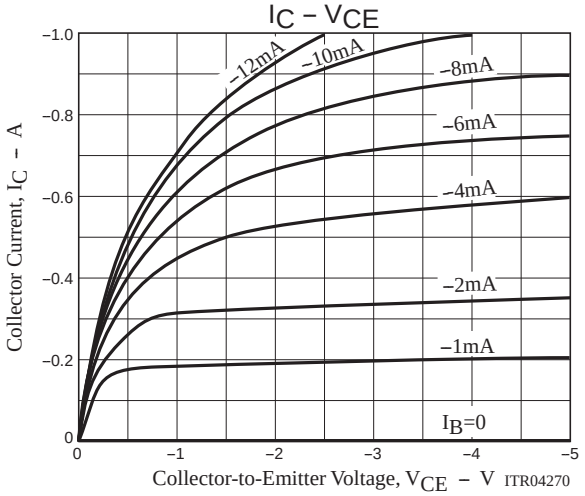
Rank	S	T
h_{FE}	140 to 280	200 to 400

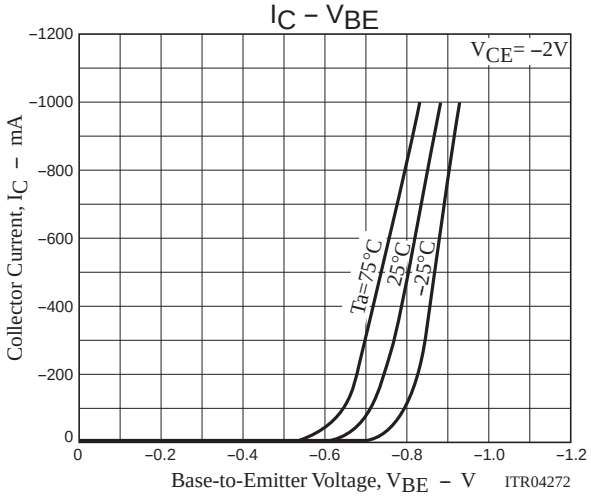
Switching Time Test Circuit

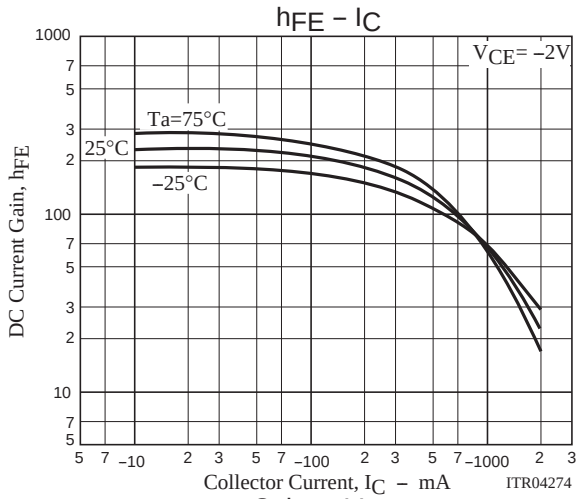


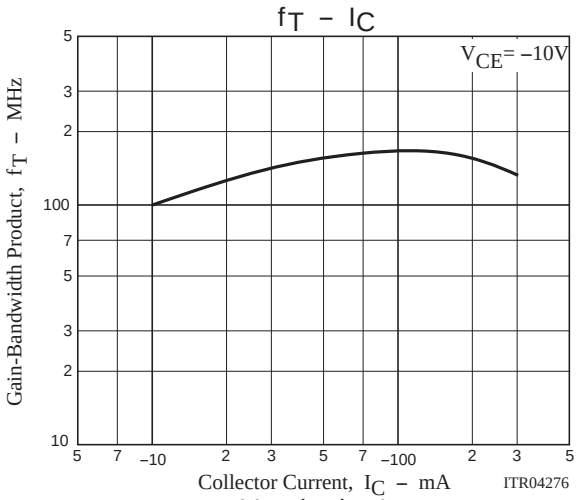
Ordering Information

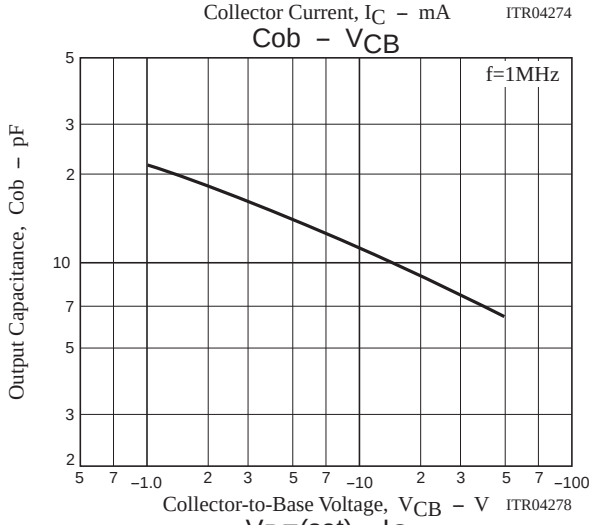
Device	Package	Shipping	memo
2SA1705S-AN	NMP(Taping)	2,500pcs./box	Pb Free
2SA1705T-AN	NMP(Taping)	2,500pcs./box	

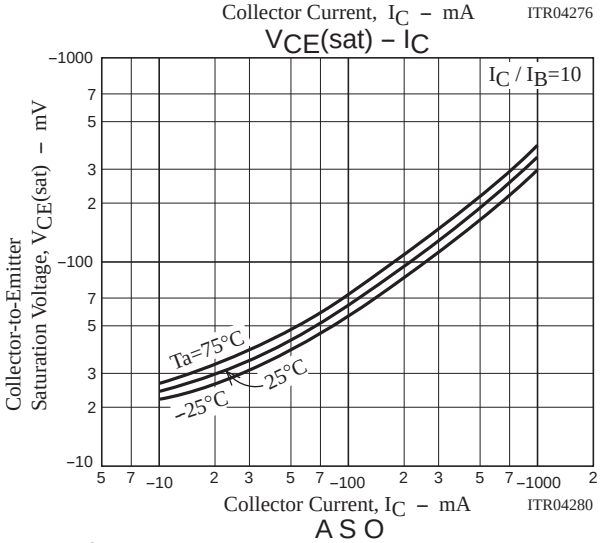


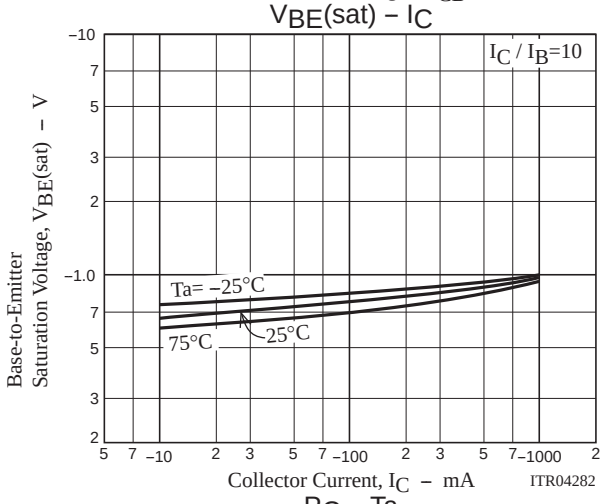


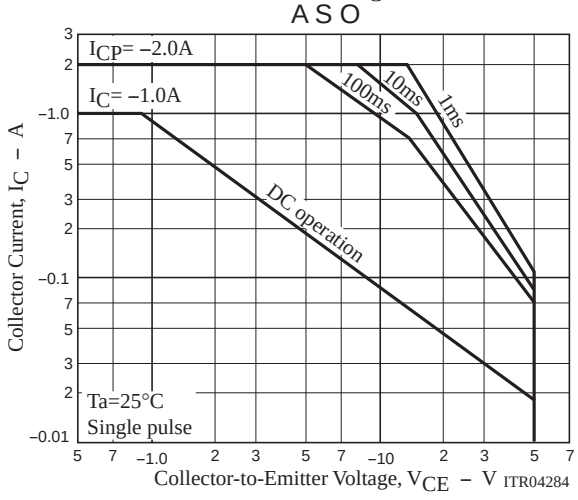

hFE – IC
VCE= –2V
Ta=75°C
25°C
–25°C
DC Current Gain, hFE
Collector Current, IC – mA
ITR04274

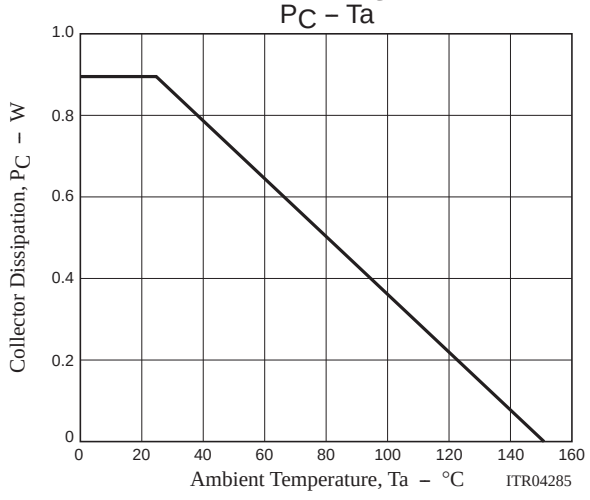

fT – IC
VCE= –10V
Gain-Bandwidth Product, fT – MHz
Collector Current, IC – mA
ITR04276


Cob – VCB
f=1MHz
Output Capacitance, Cob – pF
Collector-to-Base Voltage, VCB – V
ITR04278


VCE(sat) – IC
IC / IB=10
Ta=75°C
25°C
–25°C
Collector-to-Emitter Saturation Voltage, VCE(sat) – mV
Collector Current, IC – mA
ITR04280


VBE(sat) – IC
IC / IB=10
Ta= –25°C
75°C
25°C
Base-to-Emitter Saturation Voltage, VBE(sat) – V
Collector Current, IC – mA
ITR04282


A S O
ICP= –2.0A
IC= –1.0A
100ms
10ms
1ms
DC operation
Ta=25°C
Single pulse
Collector Current, IC – A
Collector-to-Emitter Voltage, VCE – V
ITR04284


PC – Ta
Collector Dissipation, PC – W
Ambient Temperature, Ta – °C
ITR04285

Bag Packing Specification

2SA1705S-AN, 2SA1705T-AN

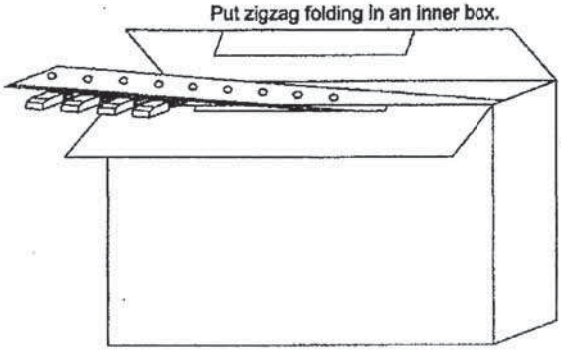
NMP (Zigzag folding)

Storage package Outline name	Package type	Maximum Number of devices contained (pcs.)		Packing format	
		Inner box No.	Storage quantity	Outer box (C—6)	Outer box (C—8)
NMP	AN/AZ	C—3 Inner box Dimensions :mm(external) 330×45×125	2,500	8 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(external) 585×345×195	4 inner boxes contained(10,000pcs.) Outer box Dimensions:mm(external) 345×300×195

1. Packing format

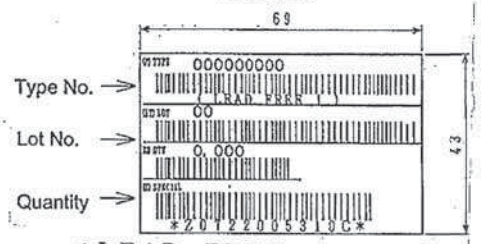
Packing method

Put zigzag folding in an inner box.



2. Bar code label

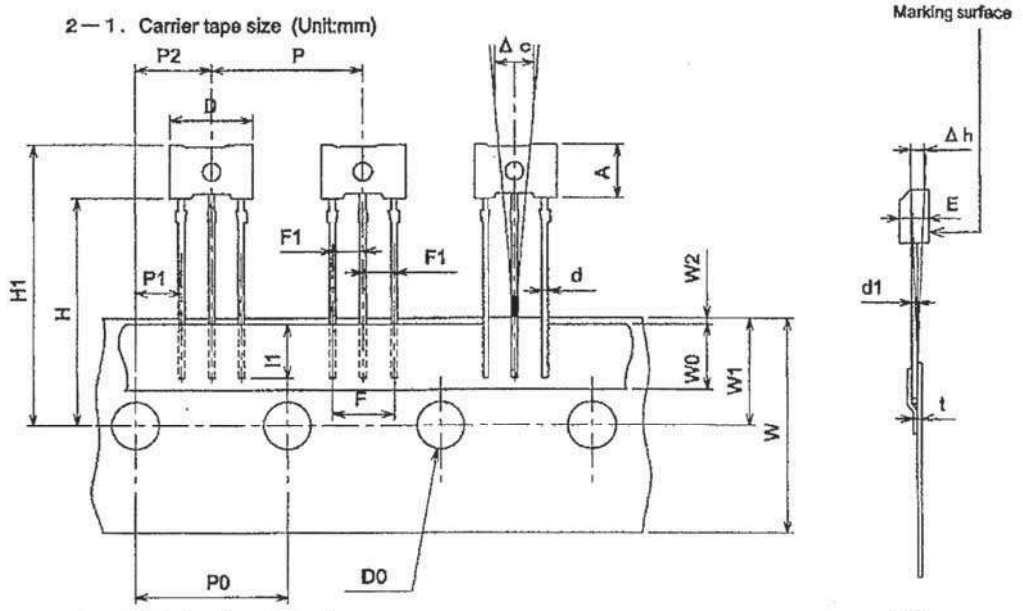
(Unit : mm)



*LEAD FREE 1:
Lead-free External terminal surface treatment product.

2. Taping specifications

2—1. Carrier tape size (Unit:mm)



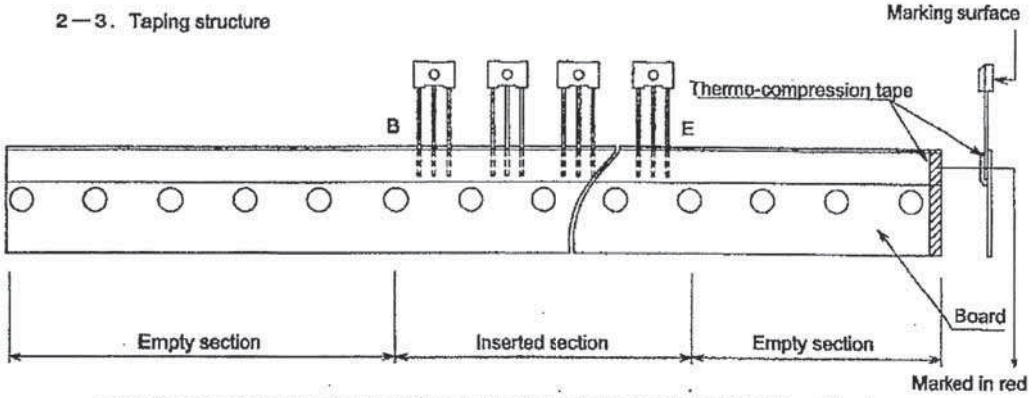
2—2. Taping size standard

Unit:mm

Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.9	±0.2
	E	2.5	±0.2
Work piece height	A	4.5	±0.2
Lead wire diameter	d	0.5	±0.1
Lead wire thickness	d1	0.45	±0.1
Bonded lead wire	I1	3.0MIN	
Pitch between products	P	12.7	±0.5
Pitch between perforations	P0	12.7	±0.2
Total pitch for 21 perforations	P0×20	254.0	±1.0
Distance between lead wire	F	5.0	+0.8 -0.2
Lead wire pitch distance	F1	2.54	+0.4 -0.1
Displacement of perforations	P1	3.81	±0.3
	P2	6.35	±0.3
Displacement of tape	W2	0～0.5	

Item	Symbol	Standard	Tolerance
Tape width	W	18.0	±0.5
Adhesive tape	W0	6.0	±0.5
Displacement of perforations	W1	9.0	±0.5
Work piece bottom surface position	H	19.0	+1.0 -0.5
Work piece upper limit position	H1	23.5	±1.0
Perforations diameter	D0	φ4.0	±0.2
Tape thickness (total thickness)	t	0.6	±0.2
Product inclination	Δ c	0	±0.7
Product inclination	Δ h	0	±1.0

2—3. Taping structure



- Provide an empty section for about three to five pieces in leading and end portions of the tape.
- Provide an empty section in the fold-back portion.
- Provide marking in red to the E-side end of the board.

Outline Drawing

2SA1705S-AN, 2SA1705T-AN