


**SANYO Semiconductors**

# DATA SHEET

An ON Semiconductor Company


**LC75879PT**

CMOS IC

## 1/4, 1/3-Duty General-Purpose LCD Display Driver

### Overview

The LC75879PT is the 1/4 duty and 1/3 duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being able to drive up to 272 segments directly, the LC75879PT can also control up to 8 general-purpose output ports. Because it has the PWM output of a maximum of 3 ch, the brightness control of the LED backlight of RGB can be done. Incorporation of an oscillation circuit helps to reduce the number of external resistors and capacitors required.

### Features

- Support for 1/4-duty 1/3-bias or 1/3-duty 1/3-bias drive techniques under serial data control.  
When 1/4-duty: Capable of driving up to 272 segments  
When 1/3-duty: Capable of driving up to 207 segments
- Serial data input supports CCB format communication with the system controller (Support 3.3V and 5V operation).
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output portfunction.  
(Support for up to 8 general-purpose output ports)
- Support for the PWM output function of a maximum of 3ch (It can output from the general-purpose output port).
- Support for clock output function of 1ch (It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- Built-in display contrast adjustment circuit.
- The INH pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit (Incorporation of resistor and capacitor for an oscillation).

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

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## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^{\circ}\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                   | Symbol              | Conditions                          | Ratings              | Unit               |
|-----------------------------|---------------------|-------------------------------------|----------------------|--------------------|
| Maximum supply voltage      | $V_{DD\text{ max}}$ | $V_{DD}$                            | -0.3 to +6.8         | V                  |
| Input voltage               | $V_{IN1}$           | CE, CL, DI, $\overline{\text{INH}}$ | -0.3 to +6.8         | V                  |
|                             | $V_{IN2}$           | OSCI, $V_{DD1}$ , $V_{DD2}$         | -0.3 to $V_{DD}+0.3$ |                    |
| Output voltage              | $V_{OUT}$           | S1 to S69, COM1 to COM4, P1 to P8   | -0.3 to $V_{DD}+0.3$ | V                  |
| Output current              | $I_{OUT1}$          | S1 to S68                           | 300                  | $\mu\text{A}$      |
|                             | $I_{OUT2}$          | COM1 to COM4, S69                   | 3                    | mA                 |
|                             | $I_{OUT3}$          | P1 to P8                            | 5                    |                    |
| Allowable power dissipation | $P_d\text{ max}$    | $T_a=85^{\circ}\text{C}$            | 200                  | mW                 |
| Operating temperature       | $T_{opr}$           |                                     | -40 to +85           | $^{\circ}\text{C}$ |
| Storage temperature         | $T_{stg}$           |                                     | -55 to +125          | $^{\circ}\text{C}$ |

**Allowable Operating Ranges** at  $T_a = -40$  to  $+85^{\circ}\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                              | Symbol       | Conditions                                                                | Ratings     |              |             | Unit          |
|----------------------------------------|--------------|---------------------------------------------------------------------------|-------------|--------------|-------------|---------------|
|                                        |              |                                                                           | min         | typ          | max         |               |
| Supply voltage                         | $V_{DD}$     | $V_{DD}$                                                                  | 4.5         |              | 6.3         | V             |
| Input voltage<br>*1                    | $V_{DD1}$    | $V_{DD1}$                                                                 |             | $2/3V_{DD0}$ | $V_{DD0}$   | V             |
|                                        | $V_{DD2}$    | $V_{DD2}$                                                                 |             | $1/3V_{DD0}$ | $V_{DD0}$   |               |
| Input high level voltage               | $V_{IH1}$    | CE, CL, DI, $\overline{\text{INH}}$                                       | $0.4V_{DD}$ |              | 6.3         | V             |
|                                        | $V_{IH2}$    | OSCI: External clock operating mode                                       | $0.4V_{DD}$ |              | $V_{DD}$    |               |
| Input low level voltage                | $V_{IL1}$    | CE, CL, DI, $\overline{\text{INH}}$                                       | 0           |              | $0.2V_{DD}$ | V             |
|                                        | $V_{IL2}$    | OSCI: External clock operating mode                                       | 0           |              | $0.2V_{DD}$ |               |
| External clock<br>operating frequency  | $f_{CK}$     | OSCI: External clock operating mode<br>[Figure4]                          | 10          | 300          | 600         | kHz           |
| External clock duty cycle              | $D_{CK}$     | OSCI: External clock operating mode<br>[Figure4]                          | 30          | 50           | 70          | %             |
| Data setup time                        | $t_{ds}$     | CL, DI [Figure2], [Figure3]                                               | 160         |              |             | ns            |
| Data hold time                         | $t_{dh}$     | CL, DI [Figure2], [Figure3]                                               | 160         |              |             | ns            |
| CE wait time                           | $t_{cp}$     | CE, CL [Figure2], [Figure3]                                               | 160         |              |             | ns            |
| CE setup time                          | $t_{cs}$     | CE, CL [Figure2], [Figure3]                                               | 160         |              |             | ns            |
| CE hold time                           | $t_{ch}$     | CE, CL [Figure2], [Figure3]                                               | 160         |              |             | ns            |
| High level clock pulse width           | $t_{\phi H}$ | CL [Figure2], [Figure3]                                                   | 160         |              |             | ns            |
| Low level clock pulse width            | $t_{\phi L}$ | CL [Figure2], [Figure3]                                                   | 160         |              |             | ns            |
| Rise time                              | $t_r$        | CE, CL, DI [Figure2], [Figure3]                                           |             | 160          |             | ns            |
| Fall time                              | $t_f$        | CE, CL, DI [Figure2], [Figure3]                                           |             | 160          |             | ns            |
| $\overline{\text{INH}}$ switching time | $t_c$        | $\overline{\text{INH}}$ , CE [Figure5], [Figure6]<br>[Figure7], [Figure8] | 10          |              |             | $\mu\text{s}$ |

Note : \*1.  $V_{DD0}=0.70V_{DD}$  to  $V_{DD}$

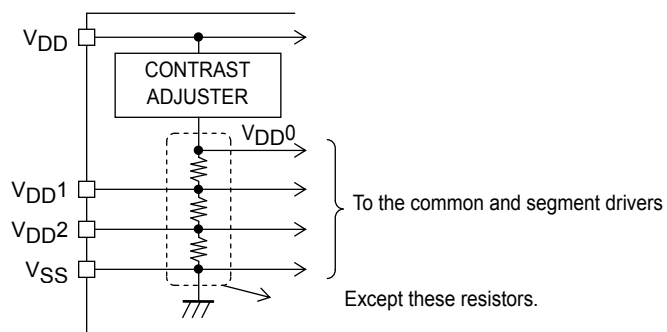
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## Electrical Characteristics for the Allowable Operating Ranges

| Parameter                            | Symbol     | Pin                                 | Conditions                                                                                                                                                                    | Ratings               |                     |                  | Unit          |
|--------------------------------------|------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------------|------------------|---------------|
|                                      |            |                                     |                                                                                                                                                                               | min                   | typ                 | max              |               |
| Hysteresis                           | $V_H$      | CE, CL, DI, $\overline{\text{INH}}$ |                                                                                                                                                                               |                       | 0.03V <sub>DD</sub> |                  | V             |
| Input high level current             | $I_{IH1}$  | CE, CL, DI, $\overline{\text{INH}}$ | $V_I=6.3\text{V}$                                                                                                                                                             |                       |                     | 5.0              | $\mu\text{A}$ |
|                                      | $I_{IH2}$  | OSCI                                | $V_I=V_{DD}$ : External clock operating mode                                                                                                                                  |                       |                     | 5.0              |               |
| Input low level current              | $I_{IL1}$  | CE, CL, DI, $\overline{\text{INH}}$ | $V_I=0\text{V}$                                                                                                                                                               | -5.0                  |                     |                  | $\mu\text{A}$ |
|                                      | $I_{IL2}$  | OSCI                                | $V_I=0\text{V}$ : External clock operating mode                                                                                                                               | -5.0                  |                     |                  |               |
| Output high level voltage *1         | $V_{OH1}$  | S1 to S69                           | $I_O=-20\mu\text{A}$                                                                                                                                                          | V <sub>DD0</sub> -0.9 |                     |                  | V             |
|                                      | $V_{OH2}$  | COM1 to COM4                        | $I_O=-100\mu\text{A}$                                                                                                                                                         | V <sub>DD0</sub> -0.9 |                     |                  |               |
|                                      | $V_{OH3}$  | P1 to P8                            | $I_O=-1\text{mA}$                                                                                                                                                             | V <sub>DD</sub> -0.9  |                     |                  |               |
| Output low level voltage             | $V_{OL1}$  | S1 to S69                           | $I_O=20\mu\text{A}$                                                                                                                                                           |                       |                     | 0.9              | V             |
|                                      | $V_{OL2}$  | COM1 to COM4                        | $I_O=100\mu\text{A}$                                                                                                                                                          |                       |                     | 0.9              |               |
|                                      | $V_{OL3}$  | P1 to P8                            | $I_O=1\text{mA}$                                                                                                                                                              |                       |                     | 0.9              |               |
| Output middle level voltage *1<br>*2 | $V_{MID1}$ | S1 to S69                           | 1/3 bias $I_O=\pm 20\mu\text{A}$                                                                                                                                              | $2/3V_{DD0}-0.9$      |                     | $2/3V_{DD0}+0.9$ | V             |
|                                      | $V_{MID2}$ | S1 to S69                           | 1/3 bias $I_O=\pm 20\mu\text{A}$                                                                                                                                              | $1/3V_{DD0}-0.9$      |                     | $1/3V_{DD0}+0.9$ |               |
|                                      | $V_{MID3}$ | COM1 to COM4                        | 1/3 bias $I_O=\pm 100\mu\text{A}$                                                                                                                                             | $2/3V_{DD0}-0.9$      |                     | $2/3V_{DD0}+0.9$ |               |
|                                      | $V_{MID4}$ | COM1 to COM4                        | 1/3 bias $I_O=\pm 100\mu\text{A}$                                                                                                                                             | $1/3V_{DD0}-0.9$      |                     | $1/3V_{DD0}+0.9$ |               |
| Oscillator frequency                 | fosc       | Internal oscillator circuit         | Internal oscillator operating mode                                                                                                                                            | 240                   | 300                 | 360              | kHz           |
| Current drain                        | $I_{DD1}$  | V <sub>DD</sub>                     | Power-saving mode                                                                                                                                                             |                       |                     | 100              | $\mu\text{A}$ |
|                                      | $I_{DD2}$  | V <sub>DD</sub>                     | V <sub>DD</sub> =6.3V<br>Output open<br>Internal oscillator operating mode                                                                                                    |                       | 1000                | 2000             |               |
|                                      | $I_{DD3}$  | V <sub>DD</sub>                     | V <sub>DD</sub> =6.3V<br>Output open<br>External clock operating mode<br>f <sub>CK</sub> =300kHz<br>V <sub>IH2</sub> =0.5V <sub>DD</sub> V <sub>IL2</sub> =0.1V <sub>DD</sub> |                       | 1000                | 2000             |               |

Note: \*1. V<sub>DD0</sub>=0.70V<sub>DD</sub> to V<sub>DD</sub>

Note: \*2. Excluding the bias voltage generation divider resistors built in the V<sub>DD1</sub> and V<sub>DD2</sub>. (See Figure 1.)



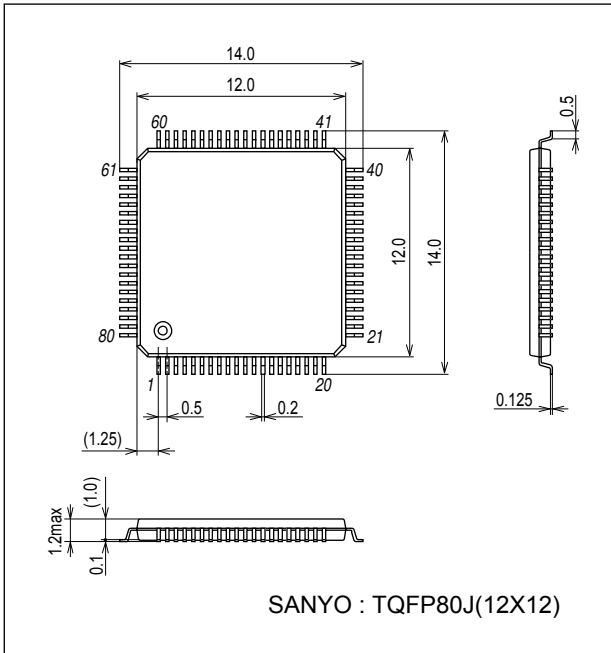
[Figure 1]



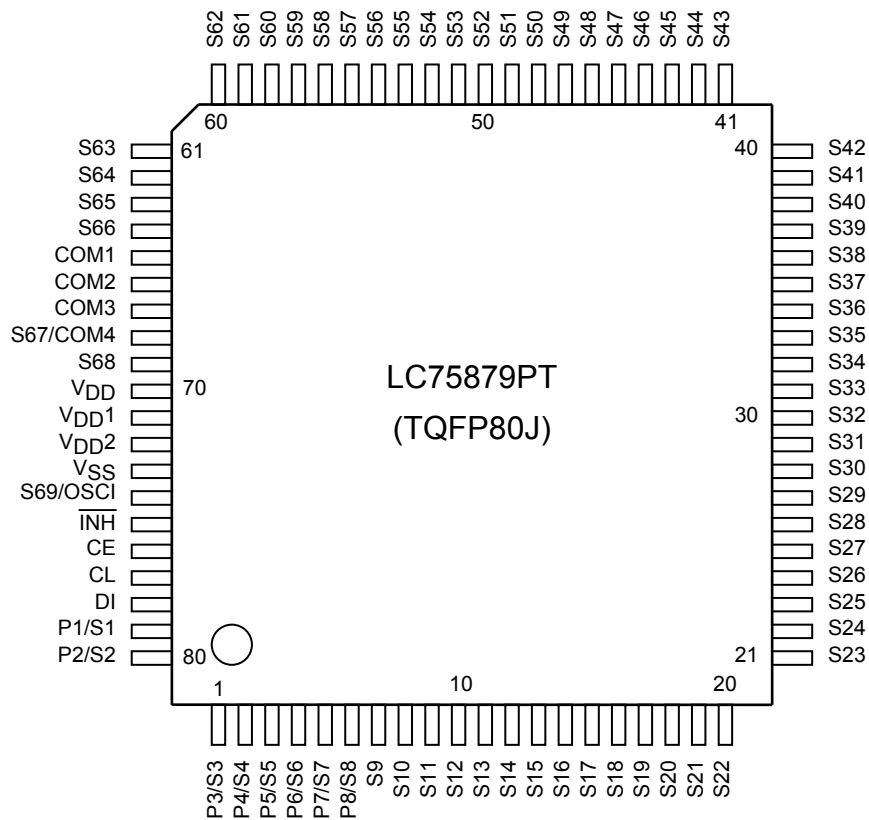
## Package Dimensions

unit : mm (typ)

3290

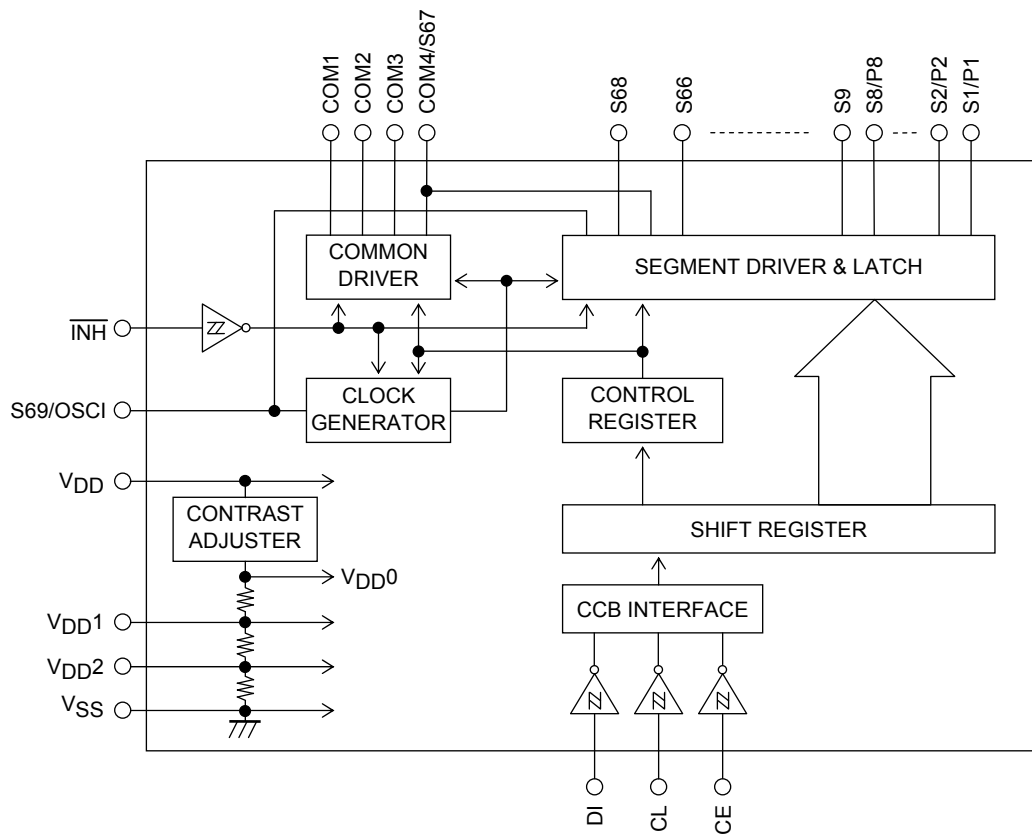


## Pin Assignment



Top view

## Block Diagram



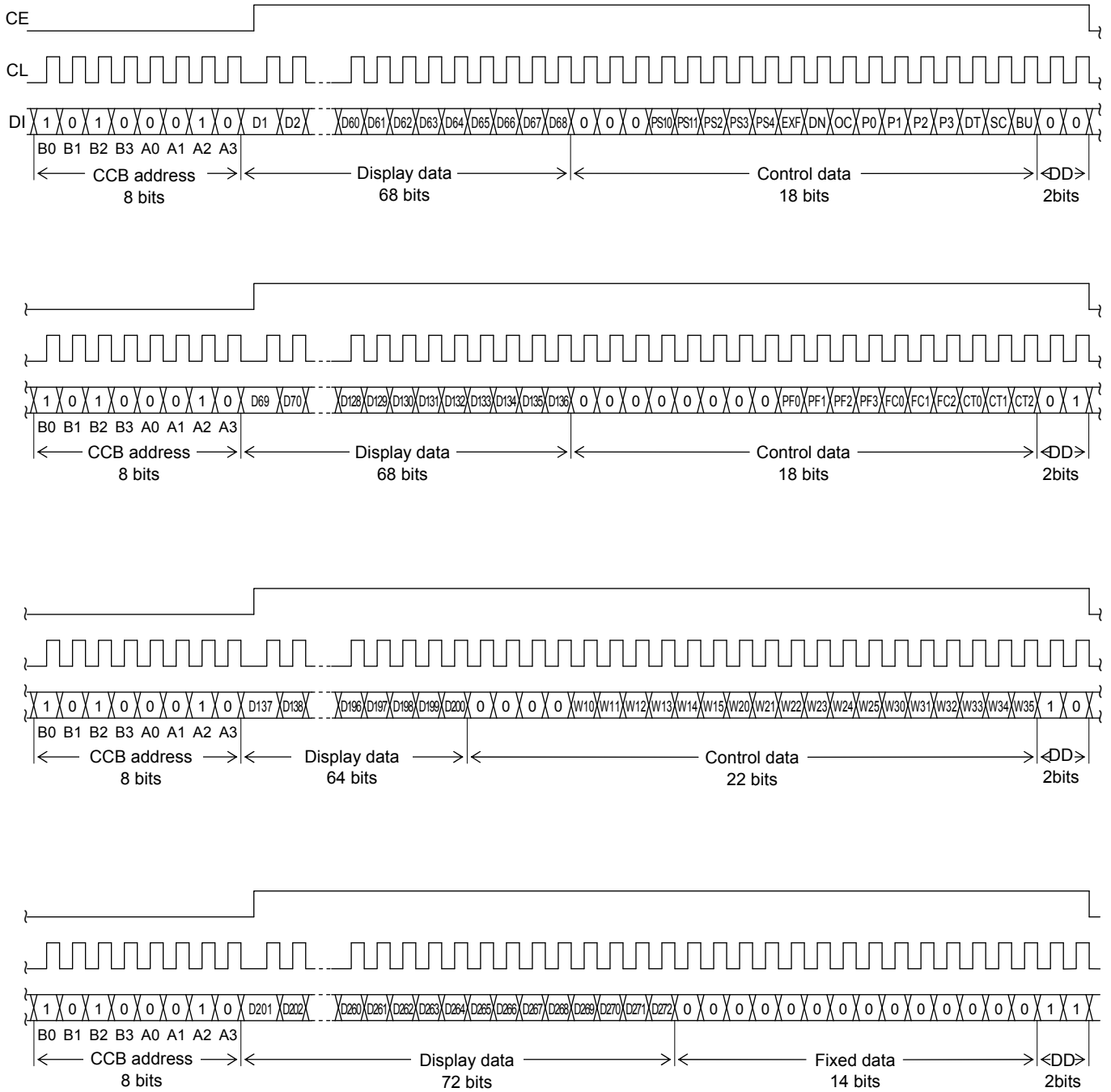
## Pin Functions

| Pin                                | Pin No.                            | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Active                                                                              | I/O | Handling when unused |
|------------------------------------|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|----------------------|
| S1/P1 to S8/P8<br>S9 to S66<br>S68 | 79, 80,<br>1 to 6<br>7 to 64<br>69 | Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S8/P8 pins can be used as general-purpose output ports under serial data control.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | -                                                                                   | O   | OPEN                 |
| COM1 to COM3<br>COM4/S67           | 65 to 67<br>68                     | Common driver outputs<br>The frame frequency is fo[Hz].<br>The COM4/S67 pin can be used as a segment output in 1/3 duty.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                   | O   | OPEN                 |
| S69/OSCI                           | 74                                 | Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -                                                                                   | I/O | OPEN                 |
| CE                                 | 76                                 | Serial data transfer inputs. Must be connected to the controller.<br>CE: Chip enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | H                                                                                   | I   | GND                  |
| CL                                 | 77                                 | CL: Synchronization clock                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  | I   |                      |
| DI                                 | 78                                 | DI: Transfer data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -                                                                                   | I   |                      |
| $\overline{\text{INH}}$            | 75                                 | Display off control input<br>• $\overline{\text{INH}}=\text{low}(\text{V}_{\text{SS}})$ ...Display forced off S1/P1 to S8/P8=low ( $\text{V}_{\text{SS}}$ )<br>(These pins are forcibly set to the general-purpose output port function and held at the $\text{V}_{\text{SS}}$ level.)<br>S9 to S66,S68=low( $\text{V}_{\text{SS}}$ )<br>COM1 to COM3=low( $\text{V}_{\text{SS}}$ )<br>COM4/S67=low( $\text{V}_{\text{SS}}$ )<br>S69/OSCI=low( $\text{V}_{\text{SS}}$ )<br>(This pin is forcibly set to the segment output port function and held at the $\text{V}_{\text{SS}}$ level.)<br>Stops the internal oscillator. Inhibits external clock input.<br>Display contrast adjustment circuit stopped.<br>• $\overline{\text{INH}}=\text{high}(\text{V}_{\text{DD}})$ ...Display on<br>Enables the internal oscillator circuit.<br>(Internal oscillator operating mode)<br>Enables external clock input.<br>(External clock operating mode)<br>Display contrast adjustment circuit operation is enabled.<br>However, serial data transfer is possible when the display is forced off. | L                                                                                   | I   | GND                  |
| $\text{V}_{\text{DD1}}$            | 71                                 | Used to apply the LCD drive 2/3 bias voltage externally.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                   | I   | OPEN                 |
| $\text{V}_{\text{DD2}}$            | 72                                 | Used to apply the LCD drive 1/3 bias voltage externally.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                   | I   | OPEN                 |
| $\text{V}_{\text{DD}}$             | 70                                 | Power supply pin. A power voltage of 4.5 to 6.3V must be applied to this pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -                                                                                   | -   | -                    |
| $\text{V}_{\text{SS}}$             | 73                                 | Ground pin. Must be connected to ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                   | -   | -                    |

## Serial Data Input

1. 1/4 duty

(1) When CL is stopped at the low level



Note: DD is the direction data.

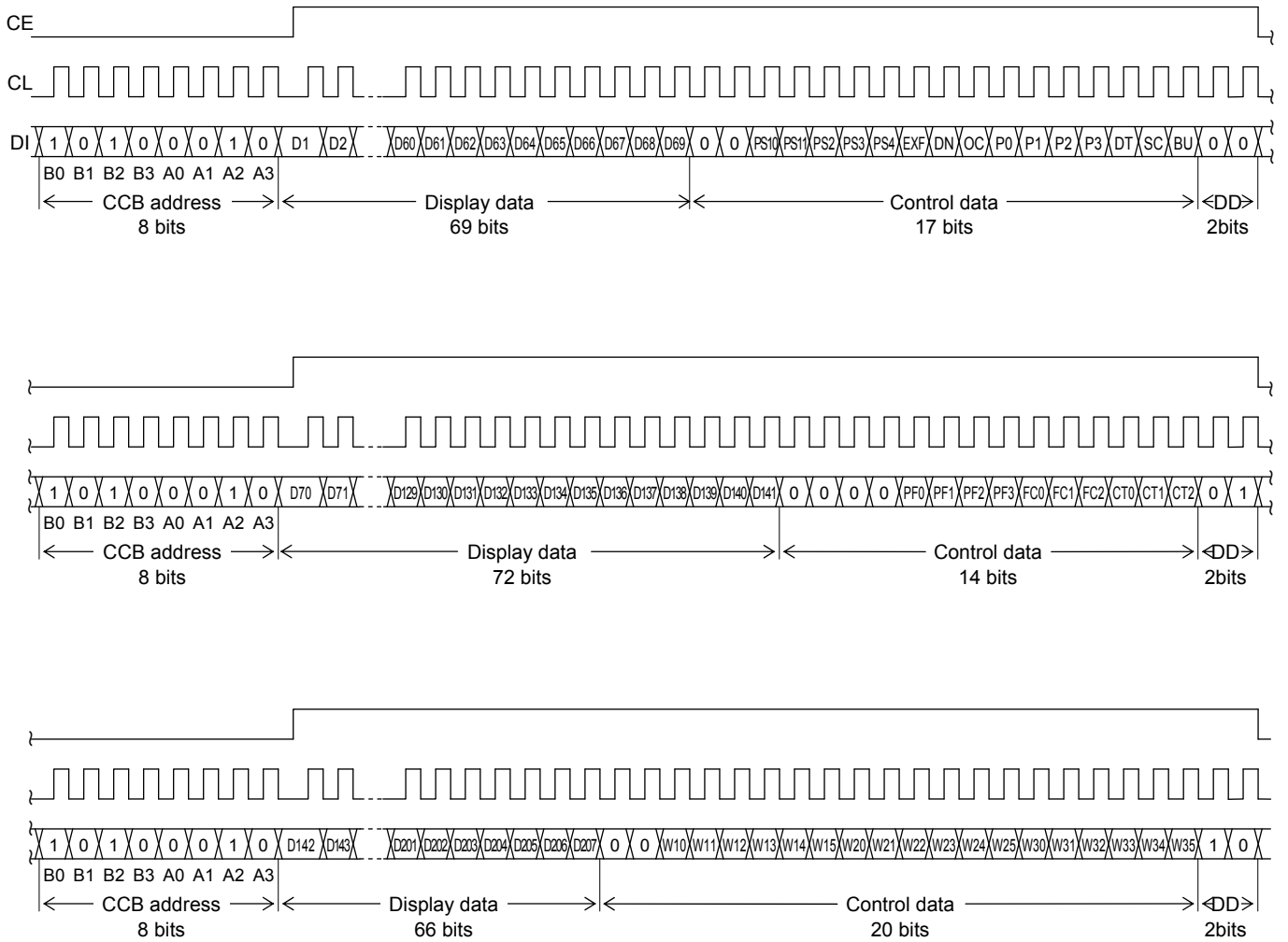




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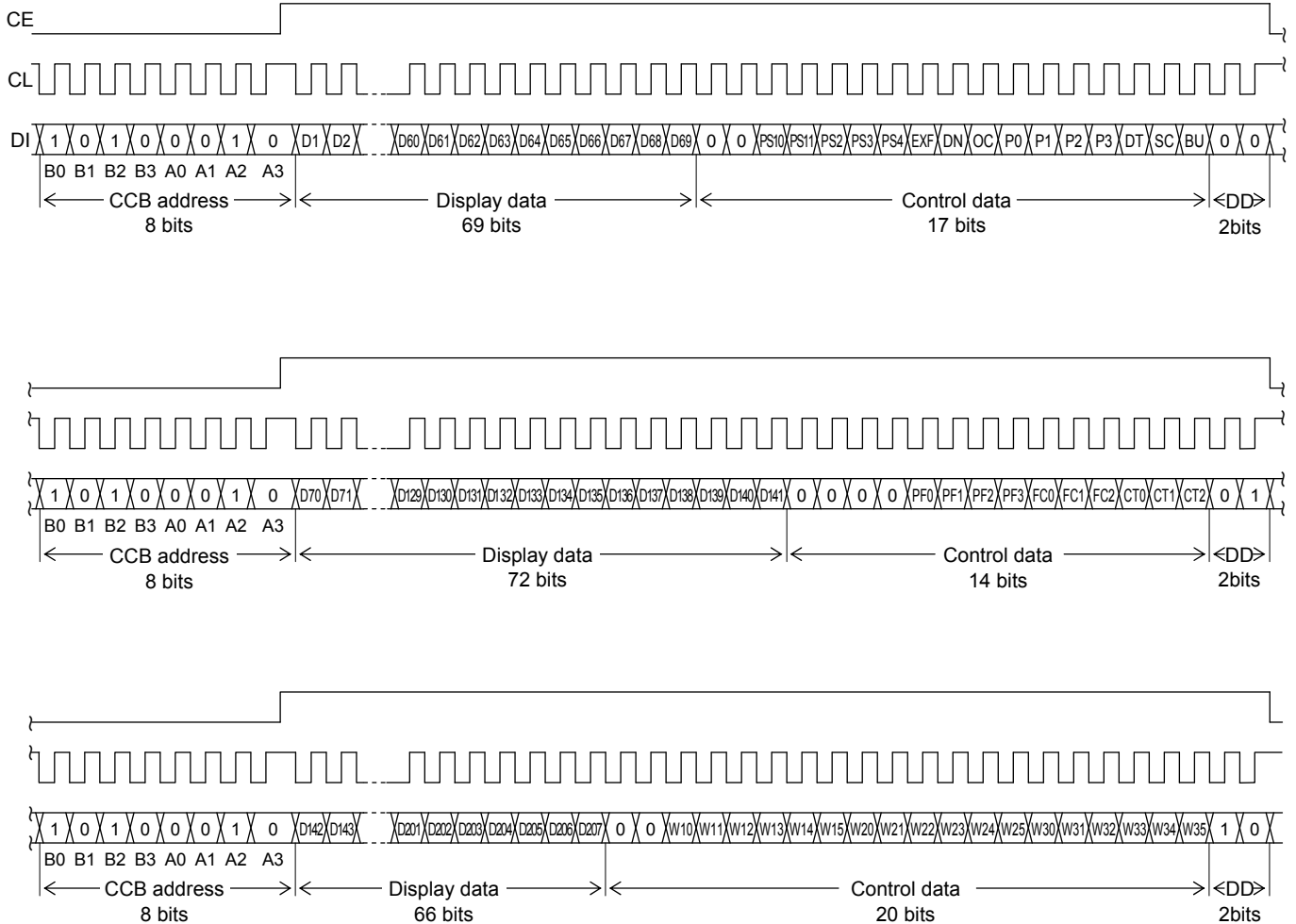
## 2. 1/3 duty

### (1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the low level



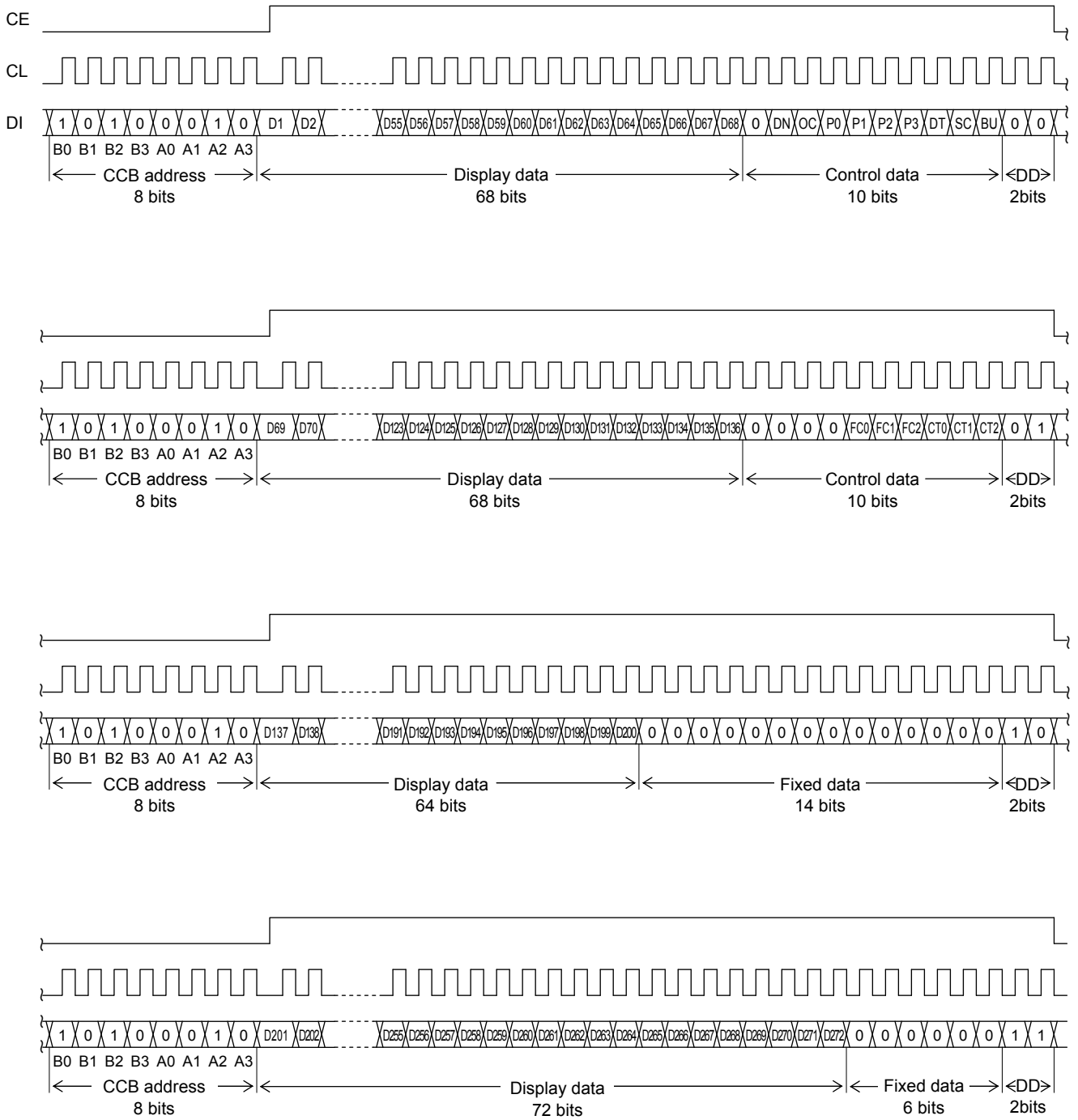
Note: DD is the direction data.

- CCB address ..... “45H”
- D1 to D207 ..... Display data
- PS10, PS11, PS2 to PS4 ..... General-purpose output port (P1 to P4) function setting control data
- EXF ..... External clock operating frequency setting control data
- DN ..... S68 pin and S69/OSCI pin state setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- CT0 to CT2 ..... Display contrast setting control data
- W10 to W15, W20 to W25, ... PWM data of the PWM output
- W30 to W35

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### 3. 1/4 duty (Simple mode transfer)

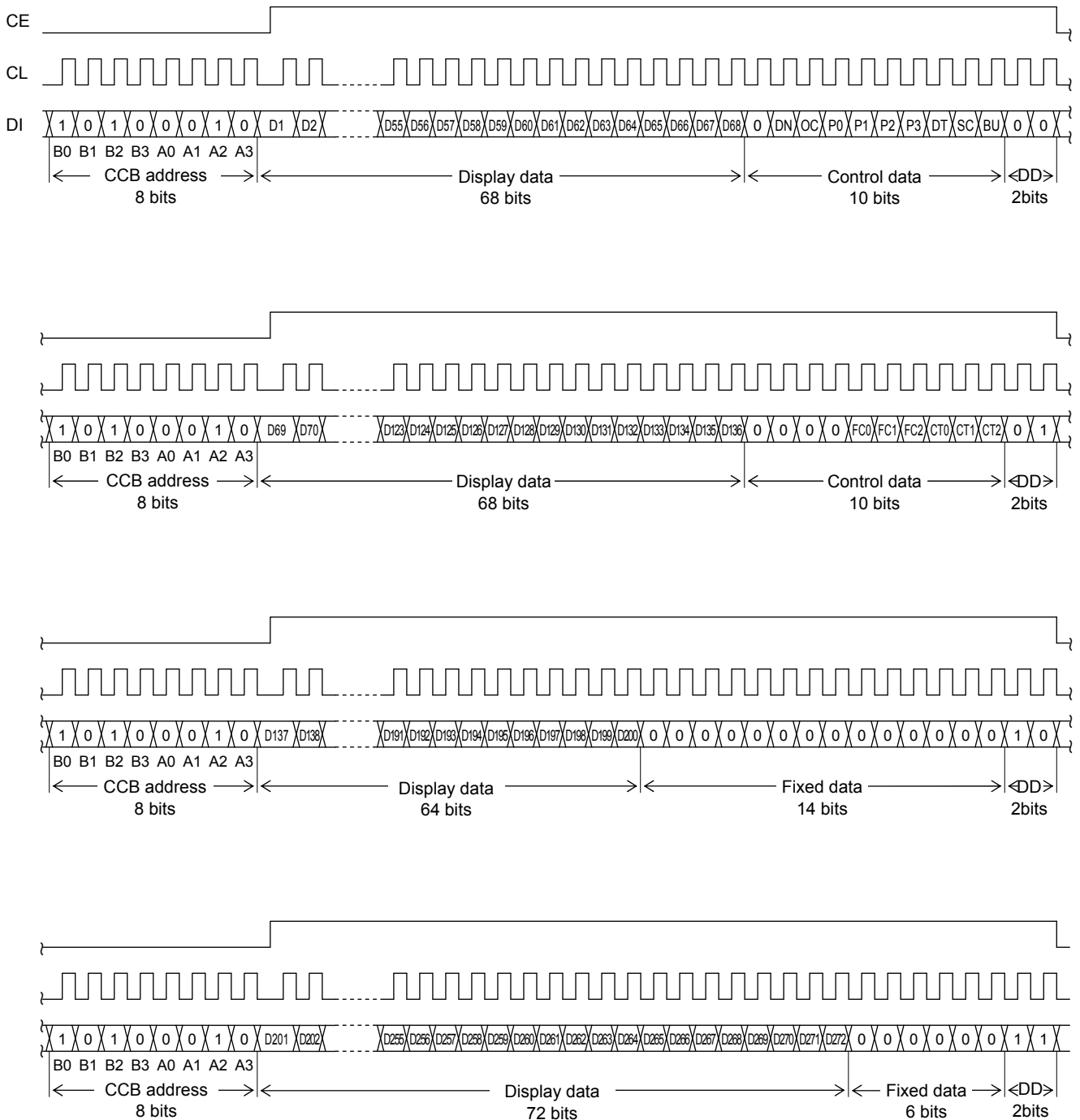
#### (1) When CL is stopped at the low level



Note: DD is the direction data.

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(2) When CL is stopped at the high level

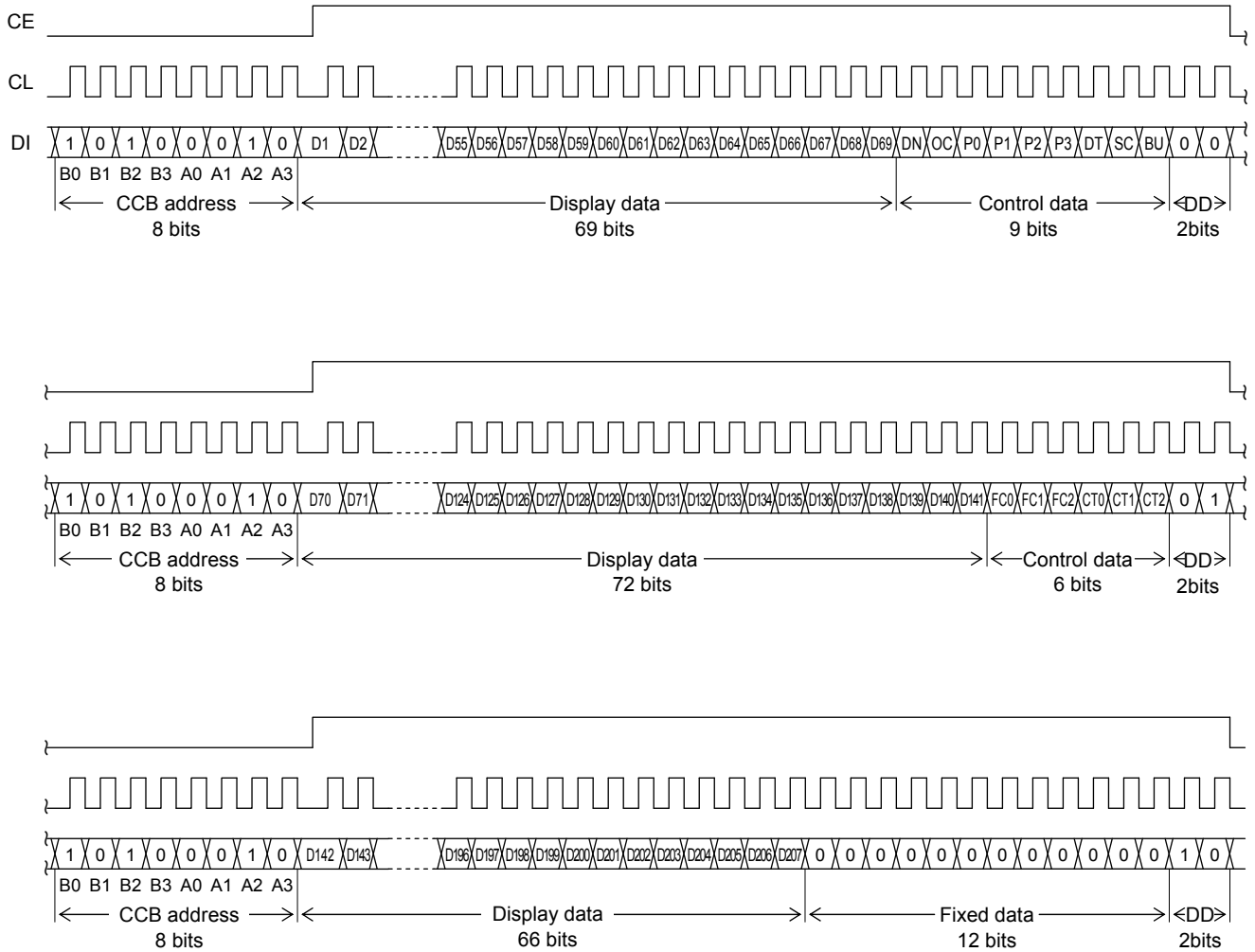


Note: DD is the direction data.

- CCB address ..... "45H"
- D1 to D272 ..... Display data
- DN ..... S68 pin and S69/OSCI pin state setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- CT0 to CT2 ..... Display contrast setting control data

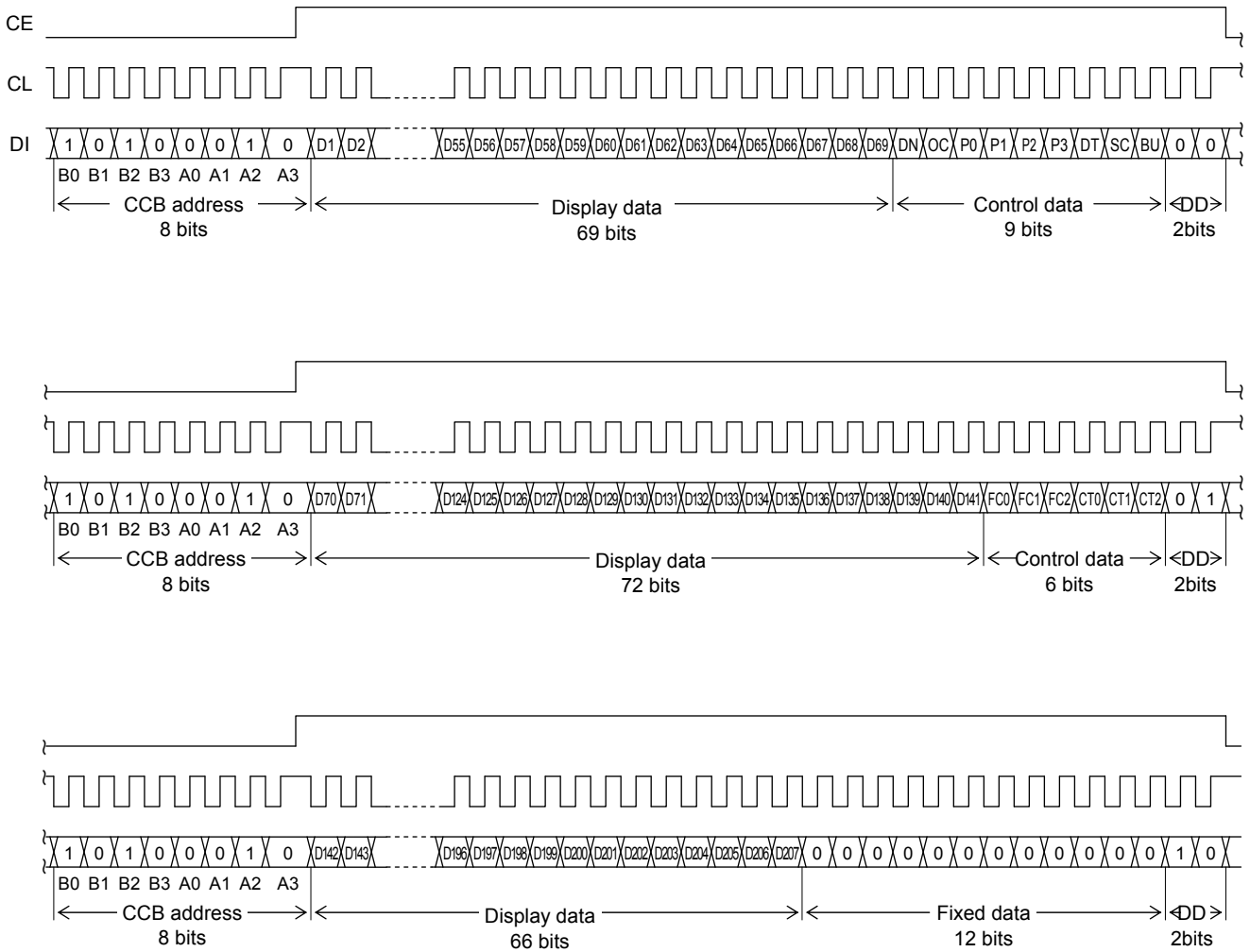
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## 4. 1/3 duty (Simple mode transfer) (1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level



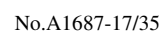
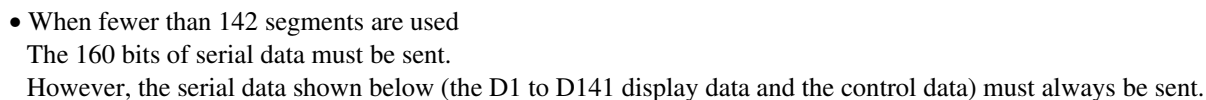
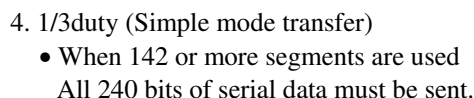
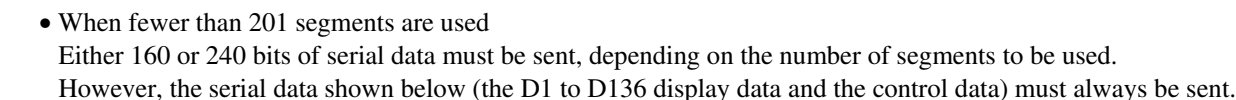
Note: DD is the direction data

- CCB address ..... “45H”
- D1 to D207 ..... Display data
- DN ..... S68 pin and S69/OSCI pin state setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- CT0 to CT2 ..... Display contrast setting control data





- When 201 or more segments are used  
All 320 bits of serial data must be sent.



## Control Data Functions

### (1) PS10 and PS11, PS2 to PS4 ... General-purpose output port (P1 to P4) function setting control data

These control data bits set the general-purpose output function (High or low level output), clock output function or PWM output function of the P1 output pin, and the general-purpose output function (High or low level output) or PWM output function of the P2 to P4 output pins.

However, be careful of being unable to set a PWM output function when the external clock operating frequency is set the  $f_{CK2}=38[\text{kHz}]$  typ (EXF="1") in external clock operating mode (OC="1").

In addition, be careful of setting of the general-purpose output function (High or low level output) in the case of the simple mode transfer forcibly.

| PS10 | PS11 | General-purpose output port (P1) function                           |
|------|------|---------------------------------------------------------------------|
| 0    | 0    | General-purpose output function (High or low level output )         |
| 1    | 0    | Clock output function (Clock frequency : $f_{osc}/2$ , $f_{CK}/2$ ) |
| 0    | 1    | Clock output function (Clock frequency : $f_{osc}/8$ , $f_{CK}/8$ ) |
| 1    | 1    | PWM output function (Support for PWM data W10 to W15)               |

| PS2 | General-purpose output port (P2) function                   |
|-----|-------------------------------------------------------------|
| 0   | General-purpose output function (High or low level output ) |
| 1   | PWM output function (Support for PWM data W20 to W25)       |

| PS3 | General-purpose output port (P3) function                   |
|-----|-------------------------------------------------------------|
| 0   | General-purpose output function (High or low level output ) |
| 1   | PWM output function (Support for PWM data W30 to W35)       |

| PS4 | General-purpose output port (P4) function                   |
|-----|-------------------------------------------------------------|
| 0   | General-purpose output function (High or low level output ) |
| 1   | PWM output function (Support for PWM data W10 to W15)       |

### (2) EXF ... External clock operating frequency setting control data

This control data bit sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC="1") is set. However, be careful of setting the  $f_{CK1}=300[\text{kHz}]$  typ when the external clock operating mode (OC="1") is set in the case of the simple mode transfer forcibly. In addition, this data is effective only when external clock operating mode (OC="1") is set.

| EXF | External clock operating frequency $f_{CK}[\text{kHz}]$ |
|-----|---------------------------------------------------------|
| 0   | $f_{CK1}=300[\text{kHz}]$ typ                           |
| 1   | $f_{CK2}=38[\text{kHz}]$ typ                            |

### (3) DN ... S68 pin and S69/OSCI pin state setting control data

This control data bit sets state of the S68 pin and the S69/OSCI pin.

| DN | Number of display segments |                   | Pin state             |                            |
|----|----------------------------|-------------------|-----------------------|----------------------------|
|    | 1/4 duty                   | 1/3 duty          | S68                   | S69/OSCI                   |
| 0  | Up to 264 segments         | Up to 201 segment | "L"(V <sub>SS</sub> ) | "L"(V <sub>SS</sub> )/OSCI |
| 1  | Up to 272 segments         | Up to 207 segment | S68                   | S69/OSCI                   |

Note: "L" (V<sub>SS</sub>) : Low (V<sub>SS</sub>) level output

S68 : Segment output

"L" (V<sub>SS</sub>)/OSCI : Low (V<sub>SS</sub>) level output in internal oscillator operating mode (OC=0)

External clock input in external clock operating mode (OC=1)

S69/OSCI : Segment output in internal oscillator operating mode (OC=0)

External clock input in external clock operating mode (OC=1)

(4) OC ... Internal oscillator operating mode/external clock operating mode switching control data

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

| OC | Fundamental clock operating mode   | I/O pin (S69/OSCI) state |
|----|------------------------------------|--------------------------|
| 0  | Internal oscillator operating mode | S69                      |
| 1  | External clock operating mode      | OSCI                     |

Note: S69 : Segment output

OSCI : External clock input

(5) P0 to P3 ... Segment output port/general-purpose output port switching control data

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S8/P8 output pins.

| Control data |    |    |    | Output pin state |       |       |       |       |       |       |       |
|--------------|----|----|----|------------------|-------|-------|-------|-------|-------|-------|-------|
| P0           | P1 | P2 | P3 | S1/P1            | S2/P2 | S3/P3 | S4/P4 | S5/P5 | S6/P6 | S7/P7 | S8/P8 |
| 0            | 0  | 0  | 0  | S1               | S2    | S3    | S4    | S5    | S6    | S7    | S8    |
| 0            | 0  | 0  | 1  | P1               | S2    | S3    | S4    | S5    | S6    | S7    | S8    |
| 0            | 0  | 1  | 0  | P1               | P2    | S3    | S4    | S5    | S6    | S7    | S8    |
| 0            | 0  | 1  | 1  | P1               | P2    | P3    | S4    | S5    | S6    | S7    | S8    |
| 0            | 1  | 0  | 0  | P1               | P2    | P3    | P4    | S5    | S6    | S7    | S8    |
| 0            | 1  | 0  | 1  | P1               | P2    | P3    | P4    | P5    | S6    | S7    | S8    |
| 0            | 1  | 1  | 0  | P1               | P2    | P3    | P4    | P5    | P6    | S7    | S8    |
| 0            | 1  | 1  | 1  | P1               | P2    | P3    | P4    | P5    | P6    | P7    | S8    |
| 1            | 0  | 0  | 0  | P1               | P2    | P3    | P4    | P5    | P6    | P7    | P8    |

Note1: Sn(n=1 to 8): Segment output ports

Pn(n=1 to 8): General-purpose output ports

Note2: When are setting (P0,P1,P2,P3)=(1,0,0,1), (1,0,1,0), (1,0,1,1) and (1,1,X,X), the all P1/S1 to P8/S8 output pins selects the segment output port.  
X: don't care

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports (general-purpose output function).

| Output pin | Correspondence display data |          |
|------------|-----------------------------|----------|
|            | 1/4 duty                    | 1/3 duty |
| S1/P1      | D1                          | D1       |
| S2/P2      | D5                          | D4       |
| S3/P3      | D9                          | D7       |
| S4/P4      | D13                         | D10      |
| S5/P5      | D17                         | D13      |
| S6/P6      | D21                         | D16      |
| S7/P7      | D25                         | D19      |
| S8/P8      | D29                         | D22      |

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port and is set general-purpose output function, the S4/P4 output pin will output a high level when the display data D13 is 1, and will output a low level when D13 is 0.

(6) DT ... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data

This control data bit selects either 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive.

| DT | Drive scheme            | The COM4/S67 pin state |
|----|-------------------------|------------------------|
| 0  | 1/4-duty 1/3-bias drive | COM4                   |
| 1  | 1/3-duty 1/3-bias drive | S67                    |

Note: COM4 : Common output

S67 : Segment output

(7) SC ... Segment on/off control data

This control data bit controls the on/off state of the segments.

| SC | Display state |
|----|---------------|
| 0  | On            |
| 1  | Off           |

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(8) BU ... Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

| BU | Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0  | Normal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1  | Power saving mode<br>( In this mode, the internal oscillator circuit stops oscillation (the S69/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC=0) and the IC stops receiving external clock signals (the S69/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC=1).<br>The common and segment output pins go to the V <sub>SS</sub> level. However, the S1/P1 to S8/P8 output pins can be used as general-purpose output ports under the control of the data bits P0 to P3.<br>(The general-purpose output port P1 to P4 can not be used as clock output or PWM output). |

(9) PF0 to PF3 ... PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the  $f_{CK2}=38[\text{kHz}]$  typ (EXF="1") in external clock operating mode (OC= "1") or when the serial data transfer is the simple mode transfer, these control data bits become invalid.

| Control data |     |     |     | PWM output waveform frame frequency fp[Hz]                                                         |                                                                                                            |
|--------------|-----|-----|-----|----------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| PF0          | PF1 | PF2 | PF3 | Internal oscillator operating mode<br>(The control data OC is 0,<br>$f_{osc}=300[\text{kHz}]$ typ) | External clock operating mode<br>(The control data OC is 1 and EXF is 0,<br>$f_{CK1}=300[\text{kHz}]$ typ) |
| 0            | 0   | 0   | 0   | $f_{osc}/1536$                                                                                     | $f_{CK1}/1536$                                                                                             |
| 1            | 0   | 0   | 0   | $f_{osc}/1408$                                                                                     | $f_{CK1}/1408$                                                                                             |
| 0            | 1   | 0   | 0   | $f_{osc}/1280$                                                                                     | $f_{CK1}/1280$                                                                                             |
| 1            | 1   | 0   | 0   | $f_{osc}/1152$                                                                                     | $f_{CK1}/1152$                                                                                             |
| 0            | 0   | 1   | 0   | $f_{osc}/1024$                                                                                     | $f_{CK1}/1024$                                                                                             |
| 1            | 0   | 1   | 0   | $f_{osc}/896$                                                                                      | $f_{CK1}/896$                                                                                              |
| 0            | 1   | 1   | 0   | $f_{osc}/768$                                                                                      | $f_{CK1}/768$                                                                                              |
| 1            | 1   | 1   | 0   | $f_{osc}/640$                                                                                      | $f_{CK1}/640$                                                                                              |
| 0            | 0   | 0   | 1   | $f_{osc}/512$                                                                                      | $f_{CK1}/512$                                                                                              |
| 1            | 0   | 0   | 1   | $f_{osc}/384$                                                                                      | $f_{CK1}/384$                                                                                              |
| 0            | 1   | 0   | 1   | $f_{osc}/256$                                                                                      | $f_{CK1}/256$                                                                                              |

Note : When is setting (PF0,PF1,PF2,PF3)=(1,1,0,1) and (X,X,1,1), the frame frequency is same as frame frequency at the time of the (PF0,PF1,PF2,PF3)=(1,0,1,0) setting ( $f_{osc}/896$ ,  $f_{CK1}/896$ ).

X: don't care

(10) FC0 to FC2 ... Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

| Control data |     |     | Common/segment output waveform frame frequency fo[Hz]                                     |                                                                                                                   |                                                                                                                  |
|--------------|-----|-----|-------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| FC0          | FC1 | FC2 | Internal oscillator<br>operating mode<br>(The control data OC is 0,<br>fosc=300[kHz] typ) | External clock<br>operating mode<br>(The control data OC is 1<br>and EXF is 0,<br>f <sub>CK1</sub> =300[kHz] typ) | External clock<br>operating mode<br>(The control data OC is 1<br>and EXF is 1,<br>f <sub>CK2</sub> =38[kHz] typ) |
| 1            | 1   | 0   | fosc/6144                                                                                 | f <sub>CK1</sub> /6144                                                                                            | f <sub>CK2</sub> /768                                                                                            |
| 1            | 1   | 1   | fosc/4608                                                                                 | f <sub>CK1</sub> /4608                                                                                            | f <sub>CK2</sub> /576                                                                                            |
| 0            | 0   | 0   | fosc/3072                                                                                 | f <sub>CK1</sub> /3072                                                                                            | f <sub>CK2</sub> /384                                                                                            |
| 0            | 0   | 1   | fosc/2304                                                                                 | f <sub>CK1</sub> /2304                                                                                            | f <sub>CK2</sub> /288                                                                                            |
| 0            | 1   | 0   | fosc/1536                                                                                 | f <sub>CK1</sub> /1536                                                                                            | f <sub>CK2</sub> /192                                                                                            |
| 0            | 1   | 1   | fosc/1152                                                                                 | f <sub>CK1</sub> /1152                                                                                            | f <sub>CK2</sub> /144                                                                                            |
| 1            | 0   | 0   | fosc/768                                                                                  | f <sub>CK1</sub> /768                                                                                             | f <sub>CK2</sub> /96                                                                                             |

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, f<sub>CK1</sub>/3072, f<sub>CK2</sub>/384).

(11) CT0 to CT2 ... Display contrast setting control data

These control data bits set display contrast.

CT0 to CT2: Sets the display contrast (7 steps)

| CT0 | CT1 | CT2 | LCD drive 3/3 bias voltage V <sub>DD0</sub> level              |
|-----|-----|-----|----------------------------------------------------------------|
| 0   | 0   | 0   | 1.00V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×0) |
| 1   | 0   | 0   | 0.95V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×1) |
| 0   | 1   | 0   | 0.90V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×2) |
| 1   | 1   | 0   | 0.85V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×3) |
| 0   | 0   | 1   | 0.80V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×4) |
| 1   | 0   | 1   | 0.75V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×5) |
| 0   | 1   | 1   | 0.70V <sub>DD</sub> =V <sub>DD</sub> -(0.05V <sub>DD</sub> ×6) |

Note: When is setting (CT0,CT1,CT2)=(1,1,1), the LCD drive 3/3 bias voltage V<sub>DD0</sub> level is 1.00V<sub>DD</sub>.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it can also be adjusted by modifying the supply pin V<sub>DD</sub> voltage level.

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(12) W10 to W15, W20 to W25, W30 to W35 ..... PWM data of the PWM output

These control data bits set the pulse width of the PWM output P1 to P4. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the  $f_{CK2}=38[\text{kHz}]$  typ (EXF="1") in external clock operating mode (OC= "1") or when the serial data transfer is the simple mode transfer, these control data bits become invalid.

| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | Pulse width of PWM output |
|-----|-----|-----|-----|-----|-----|---------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | $(1/64) \times T_p$       |
| 1   | 0   | 0   | 0   | 0   | 0   | $(2/64) \times T_p$       |
| 0   | 1   | 0   | 0   | 0   | 0   | $(3/64) \times T_p$       |
| 1   | 1   | 0   | 0   | 0   | 0   | $(4/64) \times T_p$       |
| 0   | 0   | 1   | 0   | 0   | 0   | $(5/64) \times T_p$       |
| 1   | 0   | 1   | 0   | 0   | 0   | $(6/64) \times T_p$       |
| 0   | 1   | 1   | 0   | 0   | 0   | $(7/64) \times T_p$       |
| 1   | 1   | 1   | 0   | 0   | 0   | $(8/64) \times T_p$       |
| 0   | 0   | 0   | 1   | 0   | 0   | $(9/64) \times T_p$       |
| 1   | 0   | 0   | 1   | 0   | 0   | $(10/64) \times T_p$      |
| 0   | 1   | 0   | 1   | 0   | 0   | $(11/64) \times T_p$      |
| 1   | 1   | 0   | 1   | 0   | 0   | $(12/64) \times T_p$      |
| 0   | 0   | 1   | 1   | 0   | 0   | $(13/64) \times T_p$      |
| 1   | 0   | 1   | 1   | 0   | 0   | $(14/64) \times T_p$      |
| 0   | 1   | 1   | 1   | 0   | 0   | $(15/64) \times T_p$      |
| 1   | 1   | 1   | 1   | 0   | 0   | $(16/64) \times T_p$      |
| 0   | 0   | 0   | 0   | 1   | 0   | $(17/64) \times T_p$      |
| 1   | 0   | 0   | 0   | 1   | 0   | $(18/64) \times T_p$      |
| 0   | 1   | 0   | 0   | 1   | 0   | $(19/64) \times T_p$      |
| 1   | 1   | 0   | 0   | 1   | 0   | $(20/64) \times T_p$      |
| 0   | 0   | 1   | 0   | 1   | 0   | $(21/64) \times T_p$      |
| 1   | 0   | 1   | 0   | 1   | 0   | $(22/64) \times T_p$      |
| 0   | 1   | 1   | 0   | 1   | 0   | $(23/64) \times T_p$      |
| 1   | 1   | 1   | 0   | 1   | 0   | $(24/64) \times T_p$      |
| 0   | 0   | 0   | 1   | 1   | 0   | $(25/64) \times T_p$      |
| 1   | 0   | 0   | 1   | 1   | 0   | $(26/64) \times T_p$      |
| 0   | 1   | 0   | 1   | 1   | 0   | $(27/64) \times T_p$      |
| 1   | 1   | 0   | 1   | 1   | 0   | $(28/64) \times T_p$      |
| 0   | 0   | 1   | 1   | 1   | 0   | $(29/64) \times T_p$      |
| 1   | 0   | 1   | 1   | 1   | 0   | $(30/64) \times T_p$      |
| 0   | 1   | 1   | 1   | 1   | 0   | $(31/64) \times T_p$      |
| 1   | 1   | 1   | 1   | 1   | 0   | $(32/64) \times T_p$      |

| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | Pulse width of PWM output |
|-----|-----|-----|-----|-----|-----|---------------------------|
| 0   | 0   | 0   | 0   | 0   | 1   | $(33/64) \times T_p$      |
| 1   | 0   | 0   | 0   | 0   | 1   | $(34/64) \times T_p$      |
| 0   | 1   | 0   | 0   | 0   | 1   | $(35/64) \times T_p$      |
| 1   | 1   | 0   | 0   | 0   | 1   | $(36/64) \times T_p$      |
| 0   | 0   | 1   | 0   | 0   | 1   | $(37/64) \times T_p$      |
| 1   | 0   | 1   | 0   | 0   | 1   | $(38/64) \times T_p$      |
| 0   | 1   | 1   | 0   | 0   | 1   | $(39/64) \times T_p$      |
| 1   | 1   | 1   | 0   | 0   | 1   | $(40/64) \times T_p$      |
| 0   | 0   | 0   | 1   | 0   | 1   | $(41/64) \times T_p$      |
| 1   | 0   | 0   | 1   | 0   | 1   | $(42/64) \times T_p$      |
| 0   | 1   | 0   | 1   | 0   | 1   | $(43/64) \times T_p$      |
| 1   | 1   | 0   | 1   | 0   | 1   | $(44/64) \times T_p$      |
| 0   | 0   | 1   | 1   | 0   | 1   | $(45/64) \times T_p$      |
| 1   | 0   | 1   | 1   | 0   | 1   | $(46/64) \times T_p$      |
| 0   | 1   | 1   | 1   | 0   | 1   | $(47/64) \times T_p$      |
| 1   | 1   | 1   | 1   | 0   | 1   | $(48/64) \times T_p$      |
| 0   | 0   | 0   | 0   | 1   | 1   | $(49/64) \times T_p$      |
| 1   | 0   | 0   | 0   | 1   | 1   | $(50/64) \times T_p$      |
| 0   | 1   | 0   | 0   | 1   | 1   | $(51/64) \times T_p$      |
| 1   | 1   | 0   | 0   | 1   | 1   | $(52/64) \times T_p$      |
| 0   | 0   | 1   | 0   | 1   | 1   | $(53/64) \times T_p$      |
| 1   | 0   | 1   | 0   | 1   | 1   | $(54/64) \times T_p$      |
| 0   | 1   | 1   | 0   | 1   | 1   | $(55/64) \times T_p$      |
| 1   | 1   | 1   | 0   | 1   | 1   | $(56/64) \times T_p$      |
| 0   | 0   | 0   | 1   | 1   | 1   | $(57/64) \times T_p$      |
| 1   | 0   | 0   | 1   | 1   | 1   | $(58/64) \times T_p$      |
| 0   | 1   | 0   | 1   | 1   | 1   | $(59/64) \times T_p$      |
| 1   | 1   | 0   | 1   | 1   | 1   | $(60/64) \times T_p$      |
| 0   | 0   | 1   | 1   | 1   | 1   | $(61/64) \times T_p$      |
| 1   | 0   | 1   | 1   | 1   | 1   | $(62/64) \times T_p$      |
| 0   | 1   | 1   | 1   | 1   | 1   | $(63/64) \times T_p$      |
| 1   | 1   | 1   | 1   | 1   | 1   | $(64/64) \times T_p$      |

Note: W10 to W15 ... PWM data of the output pin S1/P1 and S4/P4

W20 to W25 ... PWM data of the output pin S2/P2

W30 to W35 ... PWM data of the output pin S3/P3

$$T_p = \frac{1}{f_p}$$

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## Display Data and Output Pin Correspondence (1/4 Duty)

| Output pin | COM1 | COM2 | COM3 | COM4 | Output pin | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|------------|------|------|------|------|
| S1/P1      | D1   | D2   | D3   | D4   | S35        | D137 | D138 | D139 | D140 |
| S2/P2      | D5   | D6   | D7   | D8   | S36        | D141 | D142 | D143 | D144 |
| S3/P3      | D9   | D10  | D11  | D12  | S37        | D145 | D146 | D147 | D148 |
| S4/P4      | D13  | D14  | D15  | D16  | S38        | D149 | D150 | D151 | D152 |
| S5/P5      | D17  | D18  | D19  | D20  | S39        | D153 | D154 | D155 | D156 |
| S6/P6      | D21  | D22  | D23  | D24  | S40        | D157 | D158 | D159 | D160 |
| S7/P7      | D25  | D26  | D27  | D28  | S41        | D161 | D162 | D163 | D164 |
| S8/P8      | D29  | D30  | D31  | D32  | S42        | D165 | D166 | D167 | D168 |
| S9         | D33  | D34  | D35  | D36  | S43        | D169 | D170 | D171 | D172 |
| S10        | D37  | D38  | D39  | D40  | S44        | D173 | D174 | D175 | D176 |
| S11        | D41  | D42  | D43  | D44  | S45        | D177 | D178 | D179 | D180 |
| S12        | D45  | D46  | D47  | D48  | S46        | D181 | D182 | D183 | D184 |
| S13        | D49  | D50  | D51  | D52  | S47        | D185 | D186 | D187 | D188 |
| S14        | D53  | D54  | D55  | D56  | S48        | D189 | D190 | D191 | D192 |
| S15        | D57  | D58  | D59  | D60  | S49        | D193 | D194 | D195 | D196 |
| S16        | D61  | D62  | D63  | D64  | S50        | D197 | D198 | D199 | D200 |
| S17        | D65  | D66  | D67  | D68  | S51        | D201 | D202 | D203 | D204 |
| S18        | D69  | D70  | D71  | D72  | S52        | D205 | D206 | D207 | D208 |
| S19        | D73  | D74  | D75  | D76  | S53        | D209 | D210 | D211 | D212 |
| S20        | D77  | D78  | D79  | D80  | S54        | D213 | D214 | D215 | D216 |
| S21        | D81  | D82  | D83  | D84  | S55        | D217 | D218 | D219 | D220 |
| S22        | D85  | D86  | D87  | D88  | S56        | D221 | D222 | D223 | D224 |
| S23        | D89  | D90  | D91  | D92  | S57        | D225 | D226 | D227 | D228 |
| S24        | D93  | D94  | D95  | D96  | S58        | D229 | D230 | D231 | D232 |
| S25        | D97  | D98  | D99  | D100 | S59        | D233 | D234 | D235 | D236 |
| S26        | D101 | D102 | D103 | D104 | S60        | D237 | D238 | D239 | D240 |
| S27        | D105 | D106 | D107 | D108 | S61        | D241 | D242 | D243 | D244 |
| S28        | D109 | D110 | D111 | D112 | S62        | D245 | D246 | D247 | D248 |
| S29        | D113 | D114 | D115 | D116 | S63        | D249 | D250 | D251 | D252 |
| S30        | D117 | D118 | D119 | D120 | S64        | D253 | D254 | D255 | D256 |
| S31        | D121 | D122 | D123 | D124 | S65        | D257 | D258 | D259 | D260 |
| S32        | D125 | D126 | D127 | D128 | S66        | D261 | D262 | D263 | D264 |
| S33        | D129 | D130 | D131 | D132 | S68        | D265 | D266 | D267 | D268 |
| S34        | D133 | D134 | D135 | D136 | S69/OSCI   | D269 | D270 | D271 | D272 |

Note: This table assumes that pins S1/P1 to S8/P8 and S69/OSCI are configured for segment output.

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For example, the table below lists the output states for the S21 output pin.

| Display data |     |     |     | Output pin (S21) state                                                |
|--------------|-----|-----|-----|-----------------------------------------------------------------------|
| D81          | D82 | D83 | D84 |                                                                       |
| 0            | 0   | 0   | 0   | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off. |
| 0            | 0   | 0   | 1   | The LCD segment corresponding to COM4 is on.                          |
| 0            | 0   | 1   | 0   | The LCD segment corresponding to COM3 is on.                          |
| 0            | 0   | 1   | 1   | The LCD segment corresponding to COM3 and COM4 are on.                |
| 0            | 1   | 0   | 0   | The LCD segment corresponding to COM2 is on.                          |
| 0            | 1   | 0   | 1   | The LCD segment corresponding to COM2 and COM4 are on.                |
| 0            | 1   | 1   | 0   | The LCD segment corresponding to COM2 and COM3 are on.                |
| 0            | 1   | 1   | 1   | The LCD segments corresponding to COM2, COM3, and COM4 are on.        |
| 1            | 0   | 0   | 0   | The LCD segment corresponding to COM1 is on.                          |
| 1            | 0   | 0   | 1   | The LCD segment corresponding to COM1 and COM4 are on.                |
| 1            | 0   | 1   | 0   | The LCD segment corresponding to COM1 and COM3 are on.                |
| 1            | 0   | 1   | 1   | The LCD segments corresponding to COM1, COM3, and COM4 are on.        |
| 1            | 1   | 0   | 0   | The LCD segment corresponding to COM1 and COM2 are on.                |
| 1            | 1   | 0   | 1   | The LCD segments corresponding to COM1, COM2, and COM4 are on.        |
| 1            | 1   | 1   | 0   | The LCD segments corresponding to COM1, COM2, and COM3 are on.        |
| 1            | 1   | 1   | 1   | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.  |



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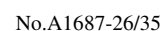
Display Data and Output Pin Correspondence (1/3 Duty)

| Output pin | COM1 | COM2 | COM3 | Output pin | COM1 | COM2 | COM3 |
|------------|------|------|------|------------|------|------|------|
| S1/P1      | D1   | D2   | D3   | S36        | D106 | D107 | D108 |
| S2/P2      | D4   | D5   | D6   | S37        | D109 | D110 | D111 |
| S3/P3      | D7   | D8   | D9   | S38        | D112 | D113 | D114 |
| S4/P4      | D10  | D11  | D12  | S39        | D115 | D116 | D117 |
| S5/P5      | D13  | D14  | D15  | S40        | D118 | D119 | D120 |
| S6/P6      | D16  | D17  | D18  | S41        | D121 | D122 | D123 |
| S7/P7      | D19  | D20  | D21  | S42        | D124 | D125 | D126 |
| S8/P8      | D22  | D23  | D24  | S43        | D127 | D128 | D129 |
| S9         | D25  | D26  | D27  | S44        | D130 | D131 | D132 |
| S10        | D28  | D29  | D30  | S45        | D133 | D134 | D135 |
| S11        | D31  | D32  | D33  | S46        | D136 | D137 | D138 |
| S12        | D34  | D35  | D36  | S47        | D139 | D140 | D141 |
| S13        | D37  | D38  | D39  | S48        | D142 | D143 | D144 |
| S14        | D40  | D41  | D42  | S49        | D145 | D146 | D147 |
| S15        | D43  | D44  | D45  | S50        | D148 | D149 | D150 |
| S16        | D46  | D47  | D48  | S51        | D151 | D152 | D153 |
| S17        | D49  | D50  | D51  | S52        | D154 | D155 | D156 |
| S18        | D52  | D53  | D54  | S53        | D157 | D158 | D159 |
| S19        | D55  | D56  | D57  | S54        | D160 | D161 | D162 |
| S20        | D58  | D59  | D60  | S55        | D163 | D164 | D165 |
| S21        | D61  | D62  | D63  | S56        | D166 | D167 | D168 |
| S22        | D64  | D65  | D66  | S57        | D169 | D170 | D171 |
| S23        | D67  | D68  | D69  | S58        | D172 | D173 | D174 |
| S24        | D70  | D71  | D72  | S59        | D175 | D176 | D177 |
| S25        | D73  | D74  | D75  | S60        | D178 | D179 | D180 |
| S26        | D76  | D77  | D78  | S61        | D181 | D182 | D183 |
| S27        | D79  | D80  | D81  | S62        | D184 | D185 | D186 |
| S28        | D82  | D83  | D84  | S63        | D187 | D188 | D189 |
| S29        | D85  | D86  | D87  | S64        | D190 | D191 | D192 |
| S30        | D88  | D89  | D90  | S65        | D193 | D194 | D195 |
| S31        | D91  | D92  | D93  | S66        | D196 | D197 | D198 |
| S32        | D94  | D95  | D96  | S67/COM4   | D199 | D200 | D201 |
| S33        | D97  | D98  | D99  | S68        | D202 | D203 | D204 |
| S34        | D100 | D101 | D102 | S69/OSCI   | D205 | D206 | D207 |
| S35        | D103 | D104 | D105 |            |      |      |      |

Note: This table assumes that pins S1/P1 to S8/P8, S67/COM4 and S69/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

| Display data |     |     | Output pin (S21) state                                          |
|--------------|-----|-----|-----------------------------------------------------------------|
| D61          | D62 | D63 |                                                                 |
| 0            | 0   | 0   | The LCD segments corresponding to COM1, COM2, and COM3 are off. |
| 0            | 0   | 1   | The LCD segment corresponding to COM3 is on.                    |
| 0            | 1   | 0   | The LCD segment corresponding to COM2 is on.                    |
| 0            | 1   | 1   | The LCD segment corresponding to COM2 and COM3 are on.          |
| 1            | 0   | 0   | The LCD segment corresponding to COM1 is on.                    |
| 1            | 0   | 1   | The LCD segment corresponding to COM1 and COM3 are on.          |
| 1            | 1   | 0   | The LCD segment corresponding to COM1 and COM2 are on.          |
| 1            | 1   | 1   | The LCD segments corresponding to COM1, COM2, and COM3 are on.  |

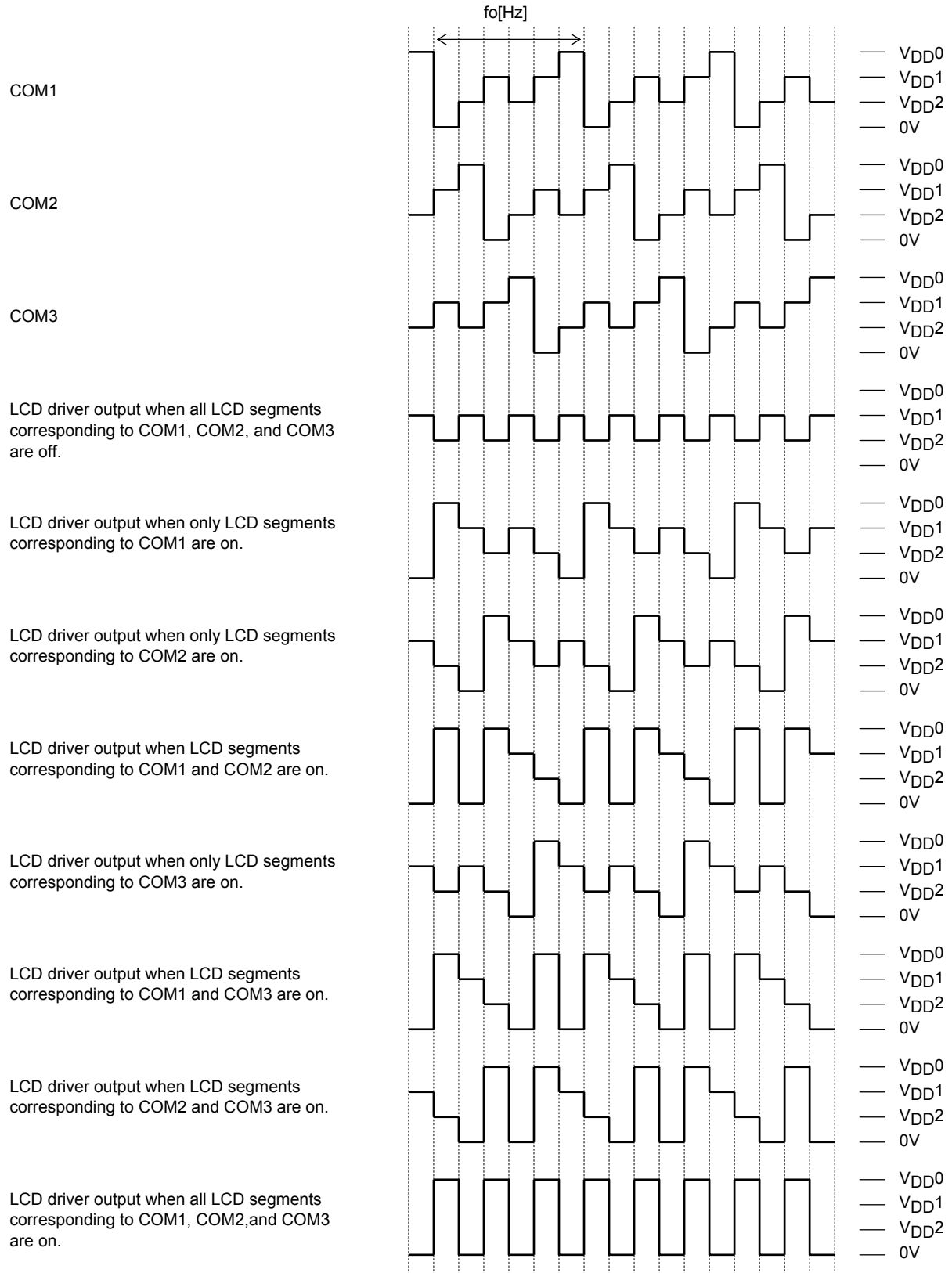


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| Control data |     |     | Common/segment output waveform frame frequency fo[Hz]                                  |                                                                                                |                                                                                               |
|--------------|-----|-----|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| FC0          | FC1 | FC2 | Internal oscillator operating mode<br>(The control data OC is 0,<br>fosc=300[kHz] typ) | External clock operating mode<br>(The control data OC is 1<br>and EXF is 0, fCK1=300[kHz] typ) | External clock operating mode<br>(The control data OC is 1<br>and EXF is 1, fCK2=38[kHz] typ) |
| 1            | 1   | 0   | fosc/6144                                                                              | fCK1/6144                                                                                      | fCK2/768                                                                                      |
| 1            | 1   | 1   | fosc/4608                                                                              | fCK1/4608                                                                                      | fCK2/576                                                                                      |
| 0            | 0   | 0   | fosc/3072                                                                              | fCK1/3072                                                                                      | fCK2/384                                                                                      |
| 0            | 0   | 1   | fosc/2304                                                                              | fCK1/2304                                                                                      | fCK2/288                                                                                      |
| 0            | 1   | 0   | fosc/1536                                                                              | fCK1/1536                                                                                      | fCK2/192                                                                                      |
| 0            | 1   | 1   | fosc/1152                                                                              | fCK1/1152                                                                                      | fCK2/144                                                                                      |
| 1            | 0   | 0   | fosc/768                                                                               | fCK1/768                                                                                       | fCK2/96                                                                                       |

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, fCK1/3072, fCK2/384).

## Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)

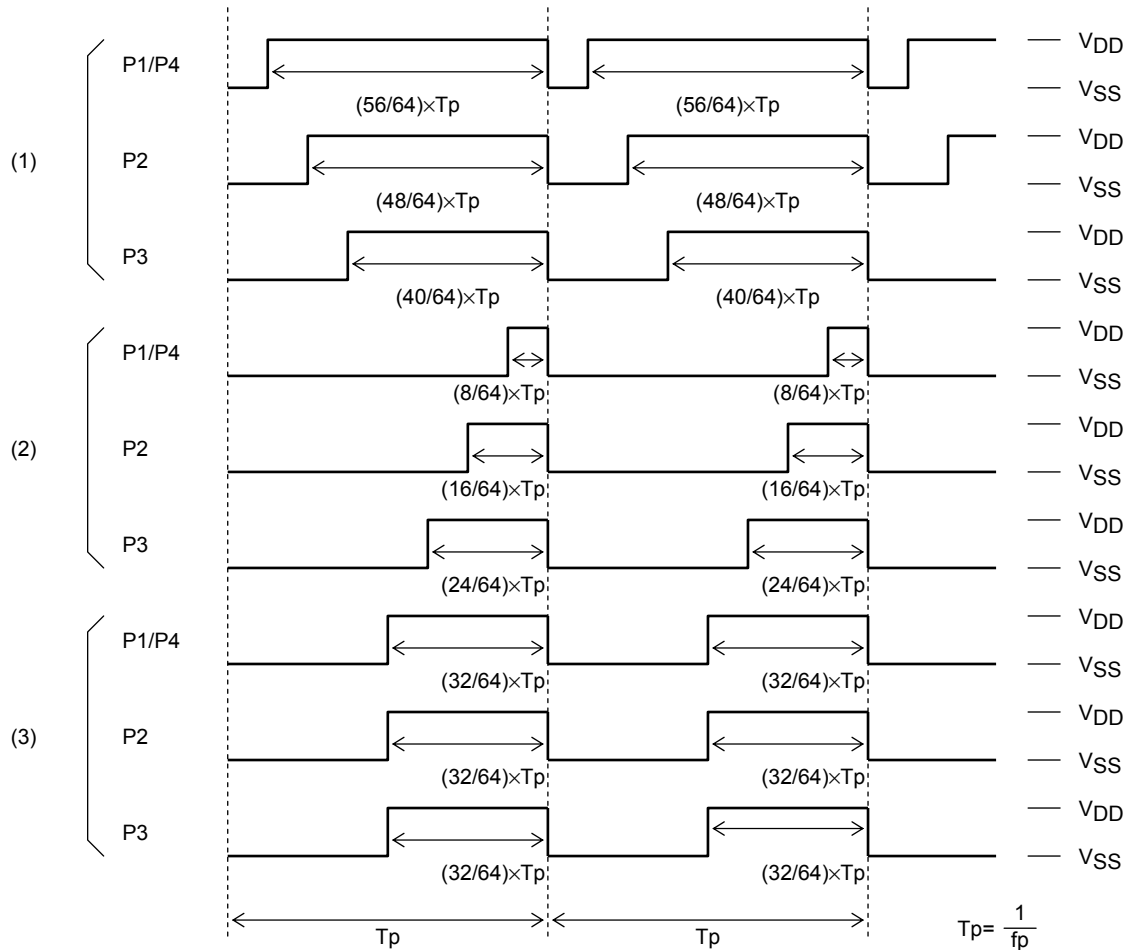


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| Control data |     |     | Common/segment output waveform frame frequency fo[Hz]                                  |                                                                                                |                                                                                               |
|--------------|-----|-----|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| FC0          | FC1 | FC2 | Internal oscillator operating mode<br>(The control data OC is 0,<br>fosc=300[kHz] typ) | External clock operating mode<br>(The control data OC is 1<br>and EXF is 0, fCK1=300[kHz] typ) | External clock operating mode<br>(The control data OC is 1<br>and EXF is 1, fCK2=38[kHz] typ) |
| 1            | 1   | 0   | fosc/6144                                                                              | fCK1/6144                                                                                      | fCK2/768                                                                                      |
| 1            | 1   | 1   | fosc/4608                                                                              | fCK1/4608                                                                                      | fCK2/576                                                                                      |
| 0            | 0   | 0   | fosc/3072                                                                              | fCK1/3072                                                                                      | fCK2/384                                                                                      |
| 0            | 0   | 1   | fosc/2304                                                                              | fCK1/2304                                                                                      | fCK2/288                                                                                      |
| 0            | 1   | 0   | fosc/1536                                                                              | fCK1/1536                                                                                      | fCK2/192                                                                                      |
| 0            | 1   | 1   | fosc/1152                                                                              | fCK1/1152                                                                                      | fCK2/144                                                                                      |
| 1            | 0   | 0   | fosc/768                                                                               | fCK1/768                                                                                       | fCK2/96                                                                                       |

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, fCK1/3072, fCK2/384).

## PWM output port waveforms



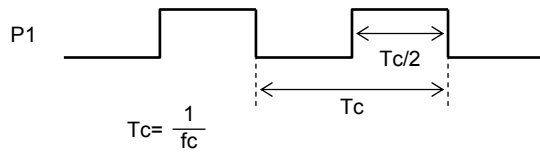
| Control data |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | PWM output waveforms |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------|
| W10          | W11 | W12 | W13 | W14 | W15 | W20 | W21 | W22 | W23 | W24 | W25 | W30 | W31 | W32 | W33 | W34 | W35 |                      |
| 1            | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 0   | 0   | 1   | (1)                  |
| 1            | 1   | 1   | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 0   | 1   | 1   | 1   | 0   | 1   | 0   | (2)                  |
| 1            | 1   | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 1   | 0   | (3)                  |

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| Control data |     |     |     | PWM output waveform frame frequency fp[Hz]                                             |                                                                                                |
|--------------|-----|-----|-----|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| PF0          | PF1 | PF2 | PF3 | Internal oscillator operating mode<br>(The control data OC is 0,<br>fosc=300[kHz] typ) | External clock operating mode<br>(The control data OC is 1 and<br>EXF is 0, fCK1=300[kHz] typ) |
| 0            | 0   | 0   | 0   | fosc/1536                                                                              | fCK1/1536                                                                                      |
| 1            | 0   | 0   | 0   | fosc/1408                                                                              | fCK1/1408                                                                                      |
| 0            | 1   | 0   | 0   | fosc/1280                                                                              | fCK1/1280                                                                                      |
| 1            | 1   | 0   | 0   | fosc/1152                                                                              | fCK1/1152                                                                                      |
| 0            | 0   | 1   | 0   | fosc/1024                                                                              | fCK1/1024                                                                                      |
| 1            | 0   | 1   | 0   | fosc/896                                                                               | fCK1/896                                                                                       |
| 0            | 1   | 1   | 0   | fosc/768                                                                               | fCK1/768                                                                                       |
| 1            | 1   | 1   | 0   | fosc/640                                                                               | fCK1/640                                                                                       |
| 0            | 0   | 0   | 1   | fosc/512                                                                               | fCK1/512                                                                                       |
| 1            | 0   | 0   | 1   | fosc/384                                                                               | fCK1/384                                                                                       |
| 0            | 1   | 0   | 1   | fosc/256                                                                               | fCK1/256                                                                                       |

Note: When is setting (PF0,PF1,PF2,PF3)=(1,1,0,1) and (X,X,1,1), the frame frequency is same as frame frequency at the time of the (PF0,PF1,PF2,PF3)=(1,0,1,0) setting (fosc/896, fCK1/896). X: don't care

Clock output waveforms

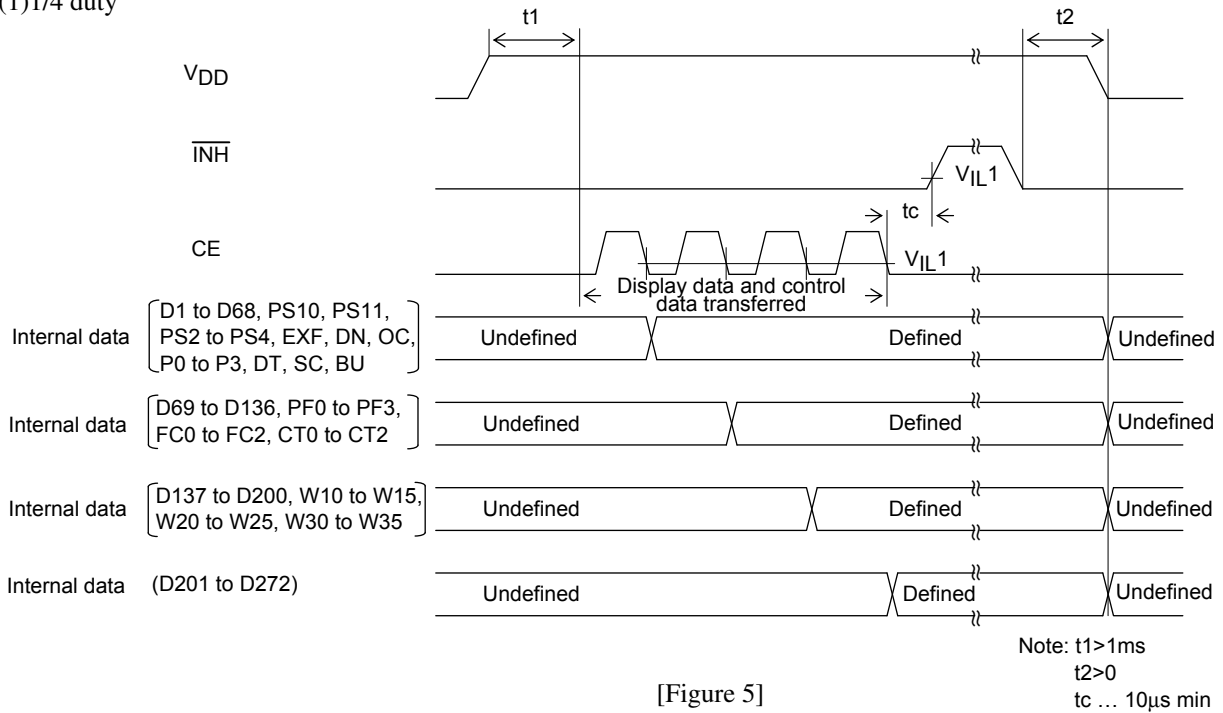


| Control data |      | Clock frequency of clock output P1<br>$f_c (=1/T_c)$ [Hz] |
|--------------|------|-----------------------------------------------------------|
| PS10         | PS11 |                                                           |
| 1            | 0    | Clock output function (fosc/2, fCK/2)                     |
| 0            | 1    | Clock output function (fosc/8, fCK/8)                     |

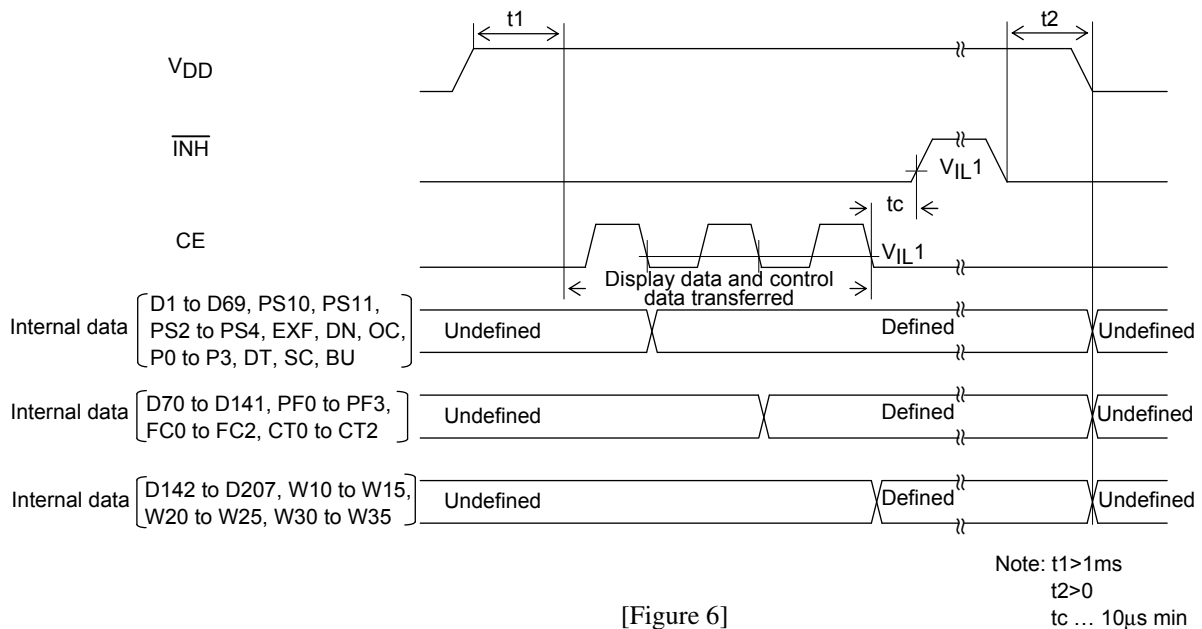
## Display Control and the $\overline{\text{INH}}$ Pin

Since the LSI internal data (1/4 duty : the display data D1 to D272 and the control data, 1/3 duty : the display data D1 to D207 and the control data) is undefined when power is first applied, applications should set the  $\overline{\text{INH}}$  pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S8/P8, S9 to S66, COM1 to COM3, COM4/S67, S68, and S69/OSCI pins to the  $V_{SS}$  level.) and during this period send serial data from the controller. The controller should then set the  $\overline{\text{INH}}$  pin high after the data transfer has completed. This procedure prevents meaningless display at power on (See Figure 5, Figure 6, Figure 7 and Figure 8.)

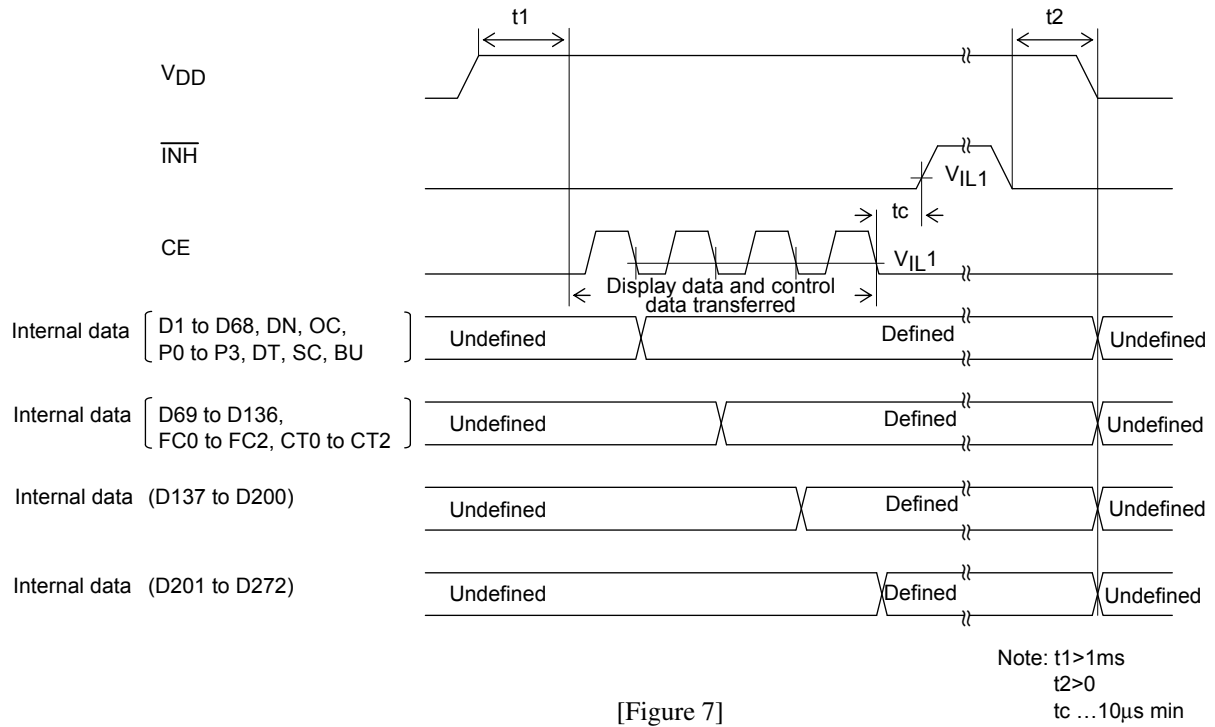
### (1) 1/4 duty



### (2) 1/3 duty

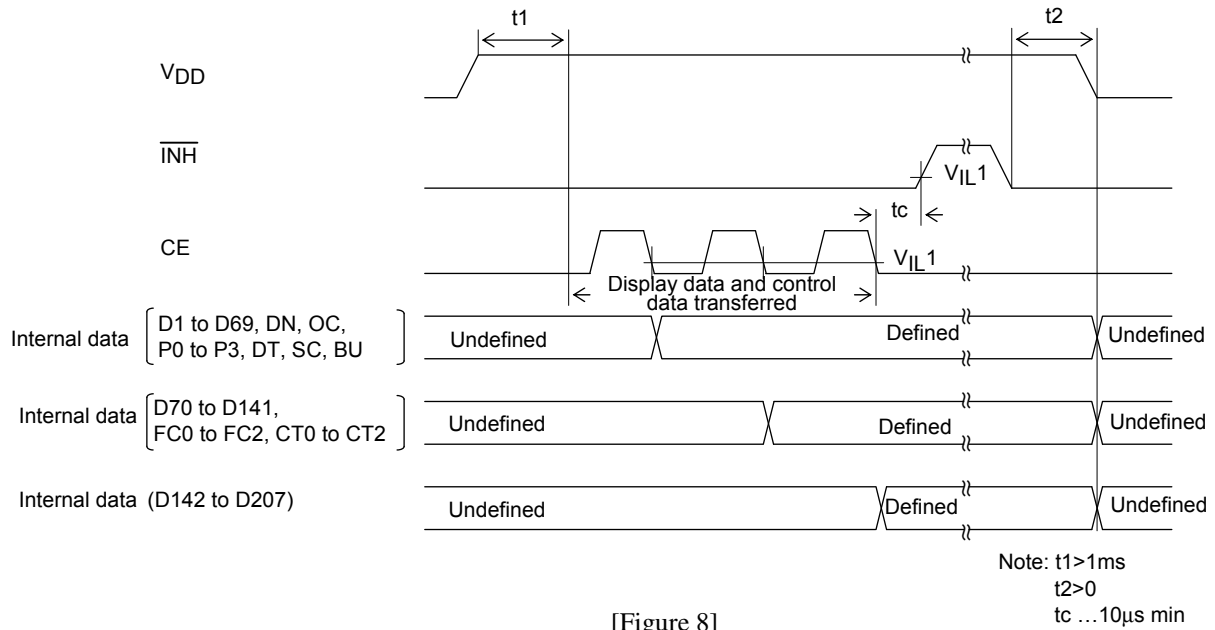


(3) 1/4 duty (Simple mode transfer)



[Figure 7]

(4) 1/3 duty (Simple mode transfer)



[Figure 8]



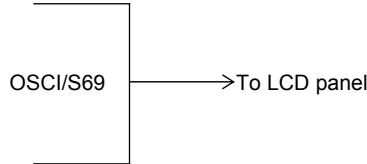
## Notes on Controller Transfer of Display Data

When using the LC75879PT in 1/4 duty, applications transfer the display data (D1 to D272) in four operations, and in 1/3 duty, they transfer the display data (D1 to D207) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

## S69/OSCI Pin Peripheral Circuit

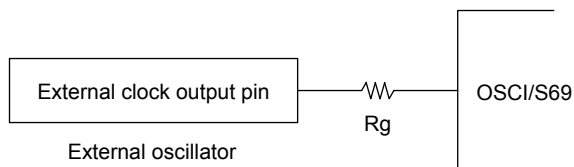
### (1) Internal oscillator operating mode (control data OC=0)

Connect the S69/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.



### (2) External clock operating mode (control data OC=1)

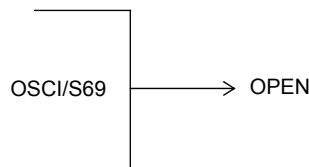
When the external clock operating mode is selected, insert a current protection resistor  $R_g$  (2.2 to 22k $\Omega$ ) between the S69/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



Note: Allowable current value at external clock output pin >  $\frac{V_{DD}}{R_g}$

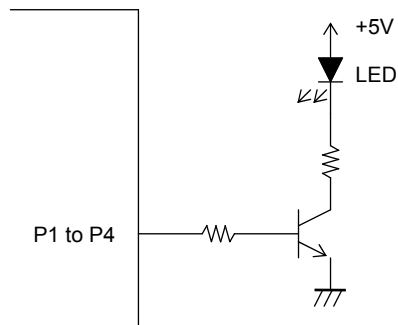
### (3) Unused pin treatment

When the S69/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



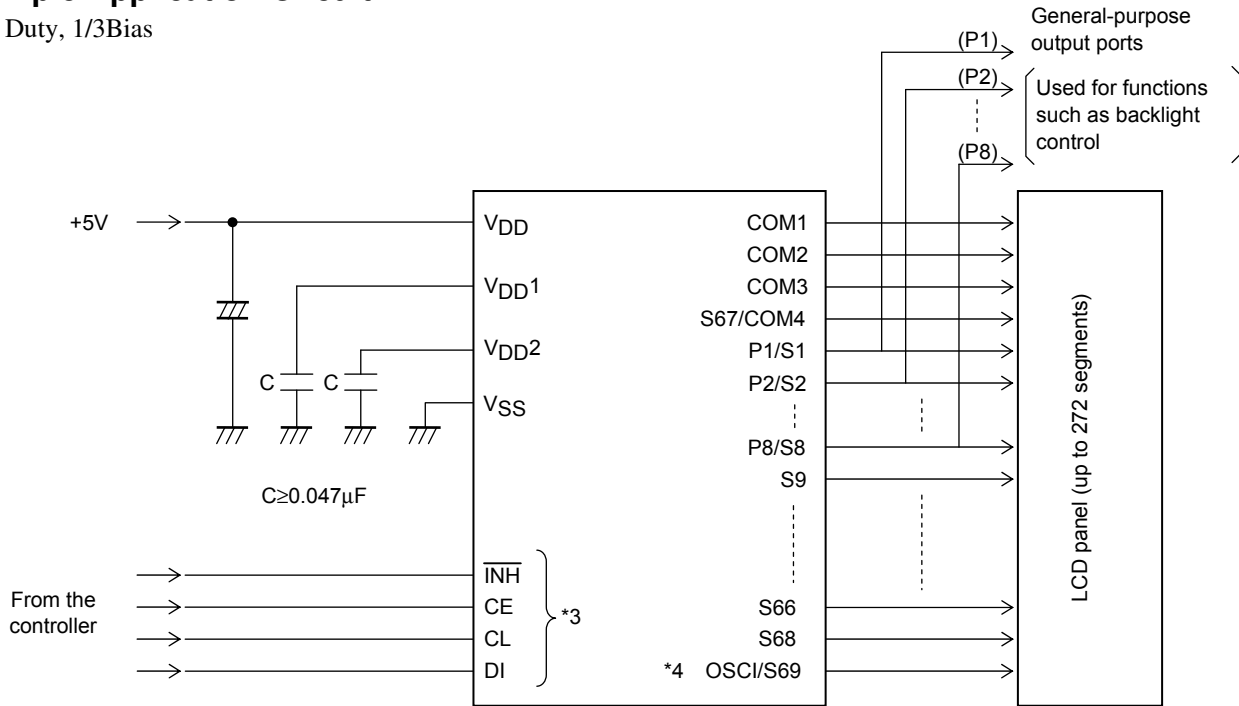
## P1 to P4 pin peripheral circuit

It is recommended the circuit shown below be used to adjust the brightness of the LED backlight using the PWM output P1 to P4



## Sample Application Circuit 1

1/4 Duty, 1/3Bias

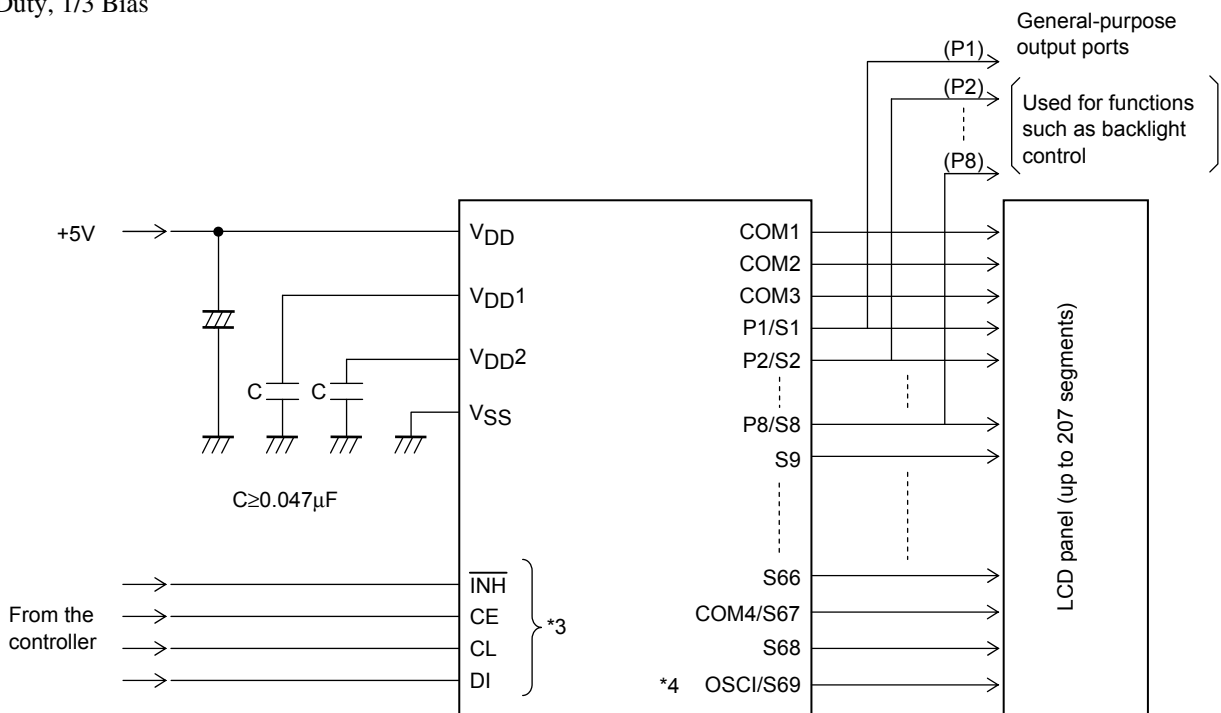


\*3 The pins to be connected to the controller (CE, CL, DI,  $\overline{\text{INH}}$ ) can handle 3.3V or 5V.

\*4 Connect the S69/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor  $R_g$  (2.2 to 22k $\Omega$ ) between the S69/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see “S69/OSCI Pin Peripheral Circuit”).

## Sample Application Circuit 2

1/3 Duty, 1/3 Bias



\*3 The pins to be connected to the controller (CE, CL, DI,  $\overline{\text{INH}}$ ) can handle 3.3V or 5V.

\*4 Connect the S69/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor  $R_g$  (2.2 to 22k $\Omega$ ) between the S69/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see “S69/OSCI Pin Peripheral Circuit”).

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