



**SANYO Semiconductors**

**DATA SHEET**

# LV5233H — Bi-CMOS IC 24ch LED Driver

## Overview

The LV5233H is a semiconductor integrated circuit that incorporates a serial input and serial or parallel output 24-stage shift register that features a CMOS structure based on Bi-CMOS process technology. The LV5233H also contains an n-channel CMOS construction high-withstand-voltage, large-current drive 24-stage parallel output driver. The protection circuit of the output malfunction is built into.

## Features

- Serial input and serial or parallel output
- Enable input for output control
- Serial output enables cascade connection
- Low supply current (0.45mA typ. during standby  $ICC \leq 0.6mA$ )
- Serial input/output levels compatible with typical CMOS devices
- High-withstand-voltage LED driver with open drain output
- High withstand voltage ( $VDS < 42V$ )
- High-current drive ( $I_O$  max = 100mA)
- Operating temperature range  $T_a = -25$  to  $75^{\circ}C$
- Output malfunction protection circuit
- Reset input pin
- Thermal protection circuit
- $V_{CC}$  decrease voltage confirmation

## Specifications

### Maximum Ratings at $T_a = 25^{\circ}C$

| Parameter                   | Symbol       | Conditions               | Ratings     | Unit |
|-----------------------------|--------------|--------------------------|-------------|------|
| Maximum supply voltage      | $V_{CC}$ max | $SV_{CC}$                | 6           | V    |
| Output voltage              | $V_O$ max    | LEDO1 to LEDO24 off      | 42          | V    |
| Output current              | $I_O$ max    |                          | 100         | mA   |
| Allowable power dissipation | $P_d$ max    | $T_a \leq 25^{\circ}C$ * | 1750        | mW   |
| Operating temperature       | $T_{opr}$    |                          | -25 to +75  | °C   |
| Storage temperature         | $T_{stg}$    |                          | -40 to +125 | °C   |

\* Specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

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LV5233H

### Operating Conditions at $T_a = 25^\circ\text{C}$

| Parameter                      | Symbol       | Conditions        | Ratings    | Unit |
|--------------------------------|--------------|-------------------|------------|------|
| Recommended supply voltage     | $V_{CC}$     | $SV_{CC}$         | 5.0        | V    |
| Operating supply voltage range | $V_{CC\ op}$ | $SV_{CC}$         | 3.0 to 5.5 | V    |
| Output applied voltage         | $V_O$        |                   | 42         | V    |
| Output current                 | $I_O$        | Duty = 45% to 55% | 100        | mA   |

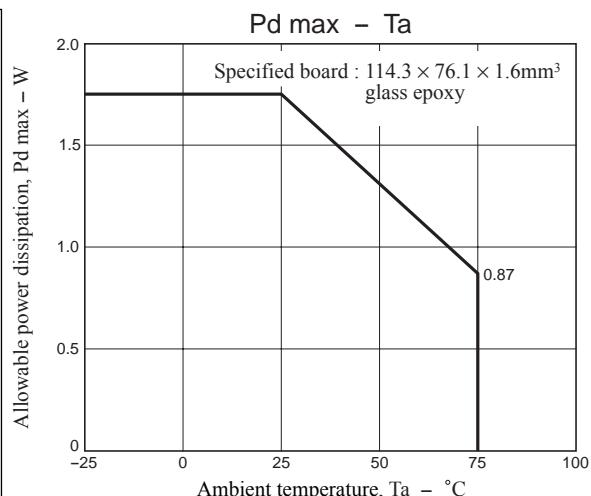
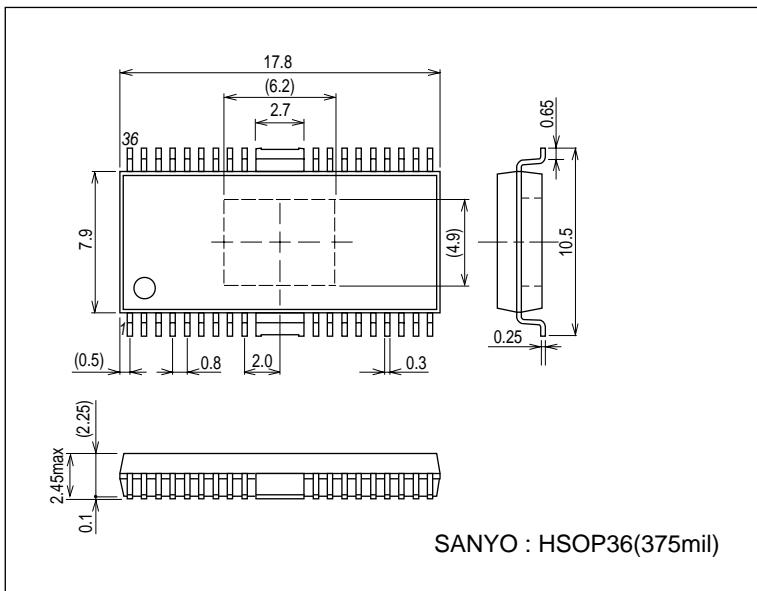
### **Electrical Characteristics** at $T_a = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$

| Parameter                                    | Symbol     | Conditions                | Ratings |      |      | Unit          |
|--|------------|---------------------------|---------|------|------|---------------|
|  |            |                           | min     | typ  | max  |               |
| Quiescent current drain                      | $I_{CC1}$  | LEDO driver off (standby) |         | 0.45 | 0.6  | mA            |
| LEDO output on resistance                    | $R_{on}$   | $I_O = 30\text{mA}$       |         | 3    |      | $\Omega$      |
| OFF leak current                             | $I_{leak}$ | $V_O = 42\text{V}$        |         | 0    | 10   | $\mu\text{A}$ |
| Driver output malfunction prevention voltage | $V_t$      |                           | 2.58    | 2.70 | 2.82 | V             |

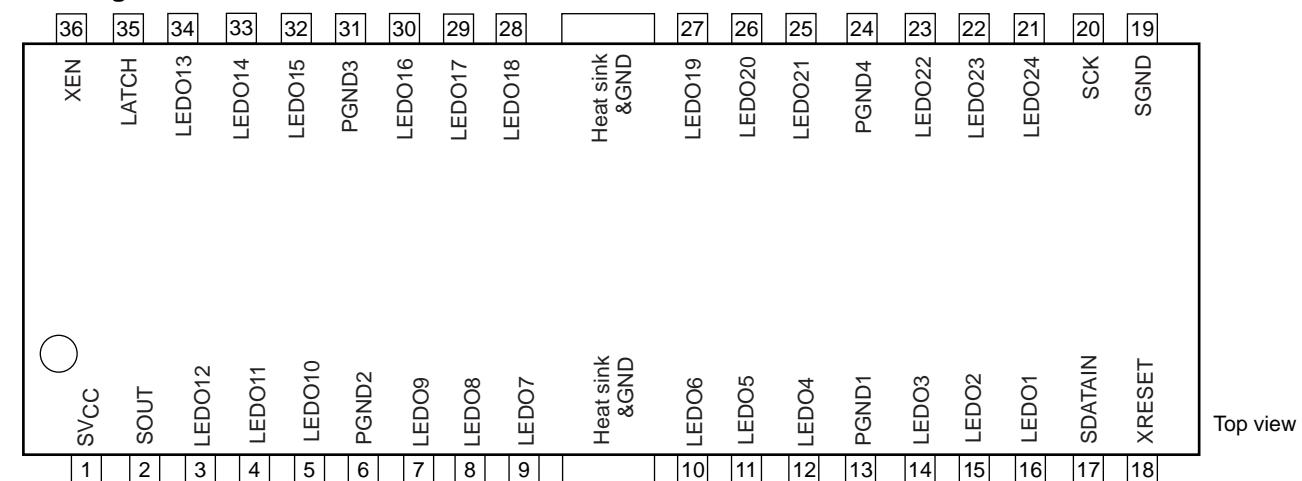
## Package Dimensions

unit : mm (typ)

3235A



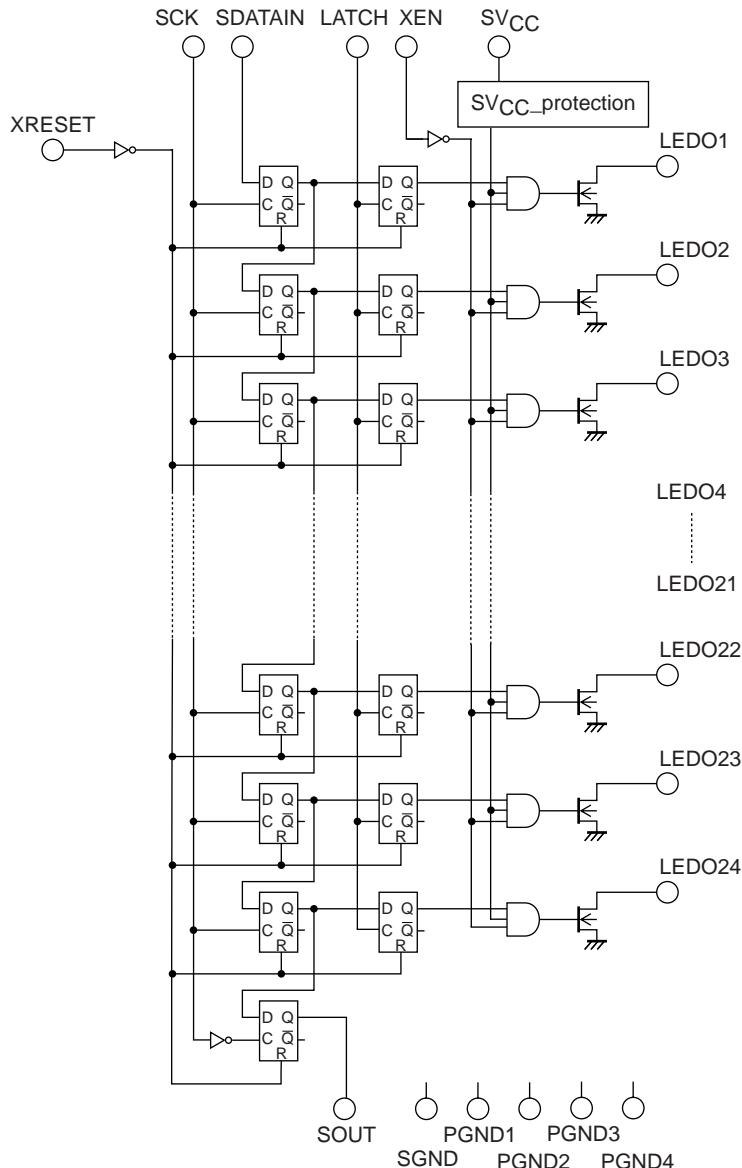
## Pin Assignment



## Pin Descriptions

| Pin No.   | Pin name | I/O | Description   |
|-----------|----------|-----|---|
| 1         | SVCC     |     | Power supply  |
| 2         | SOUT     | O   | shift register output (final-stage shift register)  |
| 3         | LEDO12   | O   | LEDO12 Latch output (LEDO12 of shift register)  |
| 4         | LEDO11   | O   | LEDO11 Latch output (LEDO11 of shift register)  |
| 5         | LEDO10   | O   | LEDO10 Latch output (LEDO10 of shift register)  |
| 6         | PGND2    |     | GND   |
| 7         | LEDO9    | O   | LEDO9 Latch output (LEDO9 of shift register)  |
| 8         | LEDO8    | O   | LEDO8 Latch output (LEDO8 of shift register)  |
| 9         | LEDO7    | O   | LEDO7 Latch output (LEDO7 of shift register)  |
| Heat sink |          |     |   |
| 10        | LEDO6    | O   | LEDO6 Latch output (LEDO6 of shift register)  |
| 11        | LEDO5    | O   | LEDO5 Latch output (LEDO5 of shift register)  |
| 12        | LEDO4    | O   | LEDO4 Latch output (LEDO4 of shift register)  |
| 13        | PGND1    |     | GND   |
| 14        | LEDO3    | O   | LEDO3 Latch output (LEDO3 of shift register)  |
| 15        | LEDO2    | O   | LEDO2 Latch output (LEDO2 of shift register)  |
| 16        | LEDO1    | O   | LEDO1 Latch output (LEDO1 of shift register)  |
| 17        | SDATAIN  | I   | Serial Input  |
| 18        | XRESET   | I   | Reset input (shift register and latch)  |
| 19        | SGND     |     | GND   |
| 20        | SCK      | I   | Clock input (for shift register)  |
| 21        | LEDO24   | O   | LEDO24 Latch output (LEDO24 of shift register)  |
| 22        | LEDO23   | O   | LEDO23 Latch output (LEDO23 of shift register)  |
| 23        | LEDO22   | O   | LEDO22 Latch output (LEDO22 of shift register)  |
| 24        | PGND4    |     | GND   |
| 25        | LEDO21   | O   | LEDO21 Latch output (LEDO21 of shift register)  |
| 26        | LEDO20   | O   | LEDO20 Latch output (LEDO20 of shift register)  |
| 27        | LEDO19   | O   | LEDO19 Latch output (LEDO19 of shift register)  |
| Heat sink |          |     |   |
| 28        | LEDO18   | O   | LEDO18 Latch output (LEDO18 of shift register)  |
| 29        | LEDO17   | O   | LEDO17 Latch output (LEDO17 of shift register)  |
| 30        | LEDO16   | O   | LEDO16 Latch output (LEDO16 of shift register)  |
| 31        | PGND3    |     | GND   |
| 32        | LEDO15   | O   | LEDO15 Latch output (LEDO15 of shift register)  |
| 33        | LEDO14   | O   | LEDO14 Latch output (LEDO14 of shift register)  |
| 34        | LEDO13   | O   | LEDO13 Latch output (LEDO13 of shift register)  |
| 35        | LATCH    | I   | <p>Latch input</p> <p>When the latch input is held low, the LED0 output status is retained.</p> <p>When a high-level is input, the LED0 outputs change when the status of the shift register changes.</p> |
| 36        | XEN      | I   | <p>Enable inputs (LEDO1 to LEDO24)</p> <p>When a high-level is input, all the LED0 outputs are turned off.</p> <p>When a low-level is input, the shift register data is output to LED0.</p>               |

## Block Diagram



## Function

The LV5233H consists of 1) an 8-stage D-type flip-flop and 2) an 8-stage D-type flip-flop connected to the output of 1). When data is supplied to the serial data input (SDATAIN) and the clock pulse is supplied to the clock input (SCK), the serial data input signal is input to the internal shift register and the data already in the shift register shifted sequentially when the clock changes from low to high.

The serial output (SOUT) is used to connect multiple LV5233H to expand the number of bits and is connected to the SDATAIN of the next stage. (Cascade connection supported.)

For parallel output, when the output control enable input (XEN) is low, the latch input (LATCH) changes from low to high and the clock pulse input changes from low to high, the serial data input signal is output to LED01, and the output is shifted sequentially. For parallel outputs (LED2 to LED24), the signals whose polarities inverted from those of the serial data input (SDATAIN) are output.

When the EN input is high, outputs LED01 through LED04 all turn off.

When the reset input is low, outputs LED01 through LED24 and SOUT outputs all turn off. The power must be turned on after checking that the reset input is low.

To prevent the malfunction, the output load protection circuit is built into. The output of LED01 to LED024 is compulsorily turned off when becoming below the voltage with a constant there is  $V_{CC}$ .

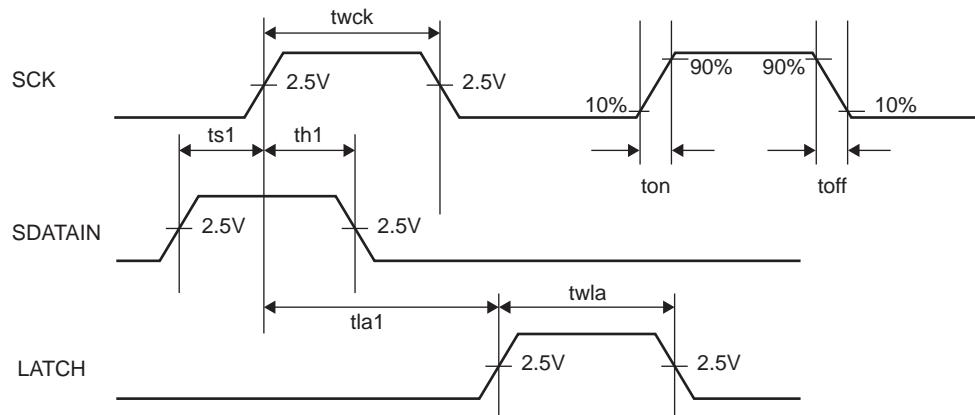
Moreover, a thermal circuit is built into, and the output of LED01 to LED024 is turned off compulsorily when becoming it at the temperature that exceeds the temperature of the junction in IC.

## Pin Functions

| Pin No.  | Pin Name  | Pin function                    | Equivalent Circuit |
|--|---|---------------------------------|--------------------|
| 17<br>20   | SDATAIN<br>SCK  | Pull-down input                 |                    |
| 18<br>35<br>36   | XRESET<br>LATCH<br>XEN  | Pull-up input                   |                    |
| 2  | SOUT  | SOUT output                     |                    |
| 3<br>4<br>5<br>7<br>8<br>9<br>10<br>11<br>12<br>14<br>15<br>16<br>21<br>22<br>23<br>25<br>26<br>27<br>28<br>29<br>30<br>32<br>33<br>34 | LEDO12<br>LEDO11<br>LEDO10<br>LEDO9<br>LEDO8<br>LEDO7<br>LEDO6<br>LEDO5<br>LEDO4<br>LEDO3<br>LEDO2<br>LEDO1<br>LEDO24<br>LEDO23<br>LEDO22<br>LEDO21<br>LEDO20<br>LEDO19<br>LEDO18<br>LEDO17<br>LEDO16<br>LEDO15<br>LEDO14<br>LEDO13 | LEDO outputs<br>LEDO1 to LEDO24 |                    |

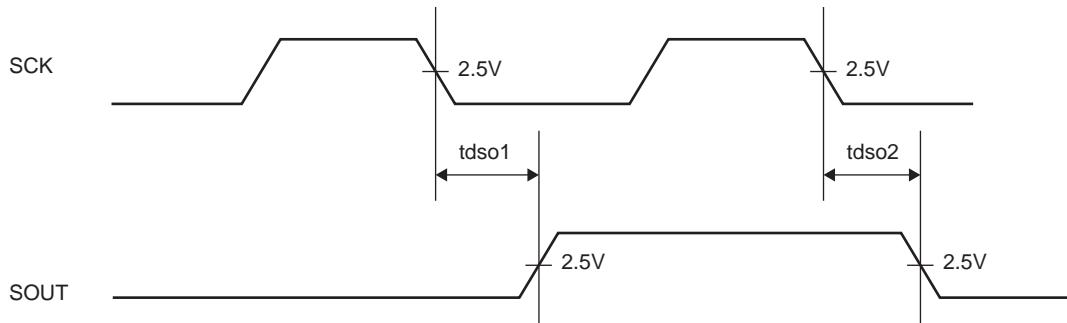
## Timing conditions

| Parameter          | symbol | Conditions   | min | typ | max | unit |
|--------------------|--------|--|-----|-----|-----|------|
| Clock frequency    | fs1    | SCK Duty = 50%                                     |     |     | 10  | MHz  |
| Clock pulse width  | twck   | SCK  | 50  |     |     | ns   |
| Latch pulse width  | twla   | LATCH  | 50  |     |     | ns   |
| Data set up time   | ts1    | SDATAIN setup time relative to the rise of SCK     | 25  |     |     | ns   |
| Data hold time     | th1    | SDATAIN data hold time relative to the rise of SCK | 25  |     |     | ns   |
| Clock latch time   | tla1   |  | 100 |     |     | ns   |
| Input conditions 1 | ton    | SCK and SDATAIN rise time                          |     |     | 100 | ns   |
| Input conditions 2 | toff   | SCL and SDATAIN fall time                          |     |     | 100 | ns   |



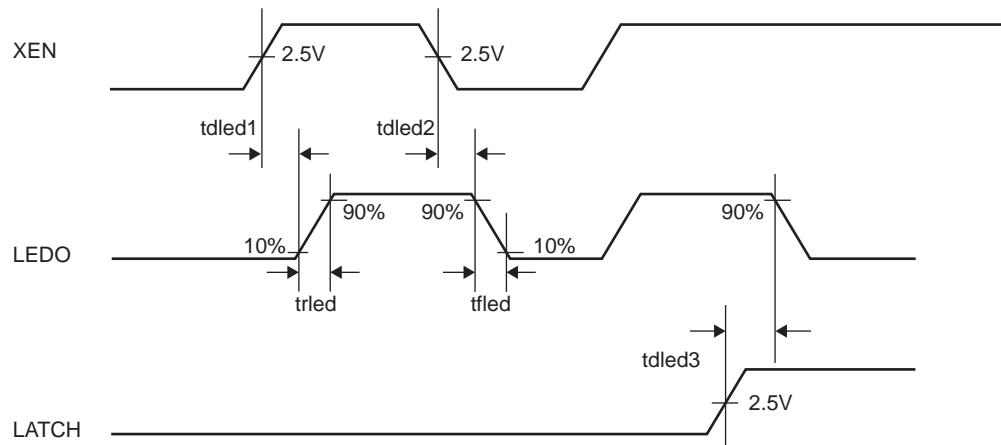
## SOUT output timings

| Parameter         | symbol | Conditions  | min | typ | max | unit |
|-------------------|--------|---|-----|-----|-----|------|
| SOUT delay time 1 | tdso1  | The time from a SCK falling edge to SOUT rising edge  |     |     | 50  | ns   |
| SOUT delay time 2 | tdso2  | The time from a SCK falling edge to SOUT falling edge |     |     | 50  | ns   |

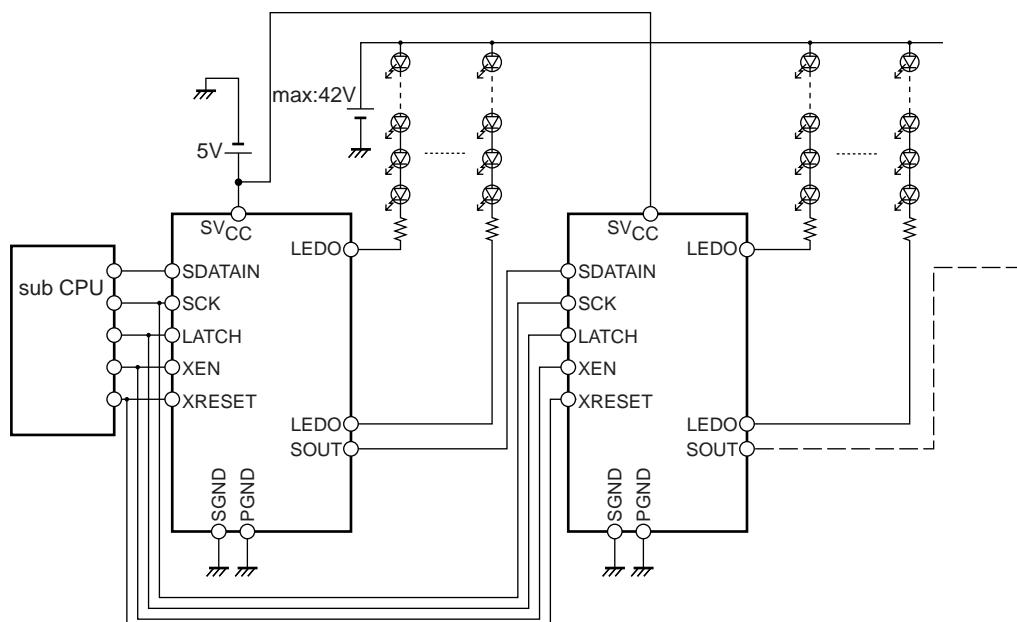


## LEDO output timings

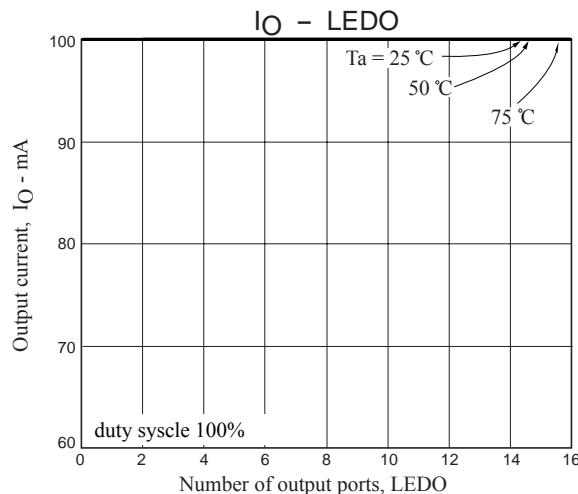
| Parameter         | symbol | Conditions  | min | typ | max | unit |
|-------------------|--------|---|-----|-----|-----|------|
| LEDO delay time 1 | tdled1 | The time from an XEN rising edge to LEDO rising edge<br>CL = 30pF, IO = 100mA, VO = 42V   |     | 100 |     | ns   |
| LEDO delay time 2 | tdled2 | The time from an XEN falling edge to LEDO falling edge<br>CL = 30pF, IO = 100mA, VO = 42V |     | 100 |     | ns   |
| LEDO rise time    | trled  | LEDO rise time<br>CL = 30pF, IO = 100mA, VO = 42V   |     | 200 |     | ns   |
| LEDO fall time    | tfled  | LEDO fall time<br>CL = 30pF, IO = 100mA, VO = 42V   |     | 200 |     | ns   |
| LEDO delay time 3 | tdled3 | The time from a LATCH rising edge to LEDO falling edge<br>CL = 30pF, IO = 100mA, VO = 42V |     | 200 |     | ns   |



## Application Circuit Example



## Allowable output current characteristics



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