



SANYO Semiconductors

DATA SHEET

LV5655VB — Bi-CMOS LSI 3-channel Switching Regulator Controller

Overview

The LV5655VB is a 3-channel switching regulator controller.

Features

- Low-voltage (3V) operation
- Reference voltage precision : $\pm 1\%$
- Standby circuit (CTL : Controls operation of all channels)
- Synchronous rectification: channel 1 and channel 2 (selected by SYN voltage)
- Independent soft start function for each channel

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		-0.3 to 16	V
Allowable power dissipation	$P_d\text{ max}$	Mounted on a specified board*	0.72	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

* Specified board: 114.3mm \times 76.1mm \times 1.6mm, glass epoxy board.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		3 to 15	V
Supply voltage	V_{BIAS}		3 to 15	V
Oscillation frequency	f_{OSC}		0.2 to 1.3	MHz

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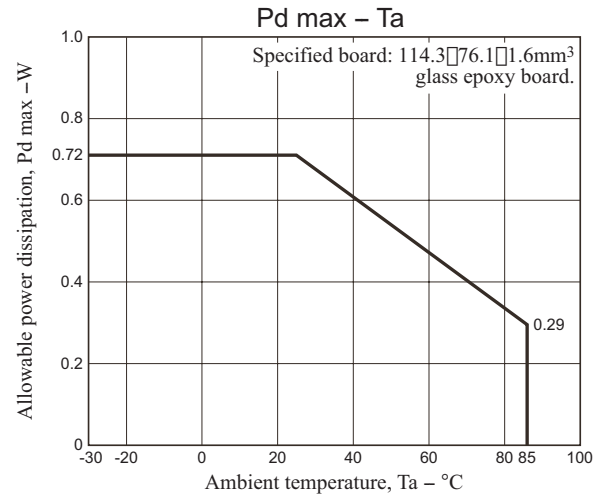
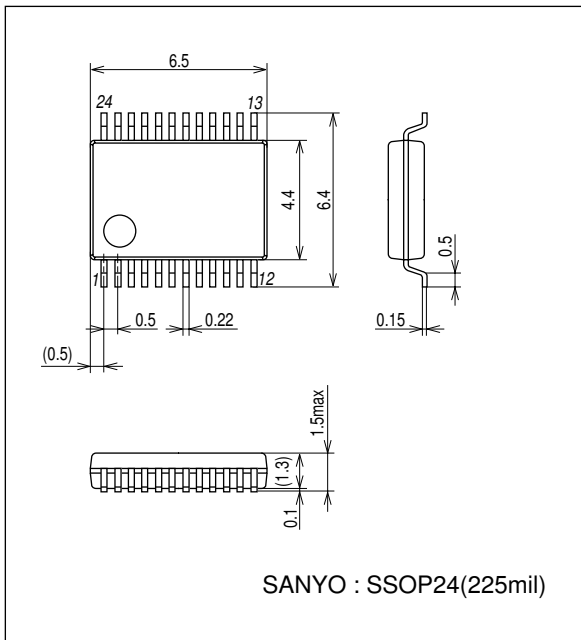
Electrical Characteristics at Ta = 25°C, VCC = VBIAS = 3.6V, SCP = 0V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Error amplifier 1							
IN ⁺ pin internal bias voltage		VB	Value added to the error amplifier offset at the error amplifier + side voltage	0.504	0.51	0.516	V
Output low voltage	ch1 to ch3	V _{Low} FB	IN ⁻ = 2.0V, IFB = 20μA			0.2	V
Output high voltage	ch1 to ch3	V _{Hi} FB	IN ⁻ = 0V, IFB1 = -20μA	2.0			V
Protection circuit							
Threshold voltage		V _{SCP}		1.1	1.25	1.4	V
SCP pin current		I _{SCP}			4		μA
Software start block							
Soft start current	ch1 to ch3	I _{SF}	CSOFT* = 0V	3.2	4	4.8	μA
Soft start resistance	ch1 to ch3	R _{SF}		160	200	240	kΩ
Fixed duty							
Maximum on duty 1	ch1	Duty MAX 1	IN ⁻ = 0V	100			%
Maximum on duty 2	ch2	Duty MAX 2	IN ⁻ = 0V	100			%
Maximum on duty 3	ch3	Duty MAX 3	IN ⁻ = 0V	80	85	90	%
Output block							
OUT pin high side on resistance		R _{OUT} SOUR	I _O = -10mA		28	50	Ω
OUT pin low side on resistance		R _{OUT} SINK	I _O = 10mA		18	35	Ω
Triangle wave oscillator block							
Current setting pin voltage		VT RT	RT = 20kΩ		0.56		V
Oscillation frequency		f _{OSC}	RT = 20kΩ	460	600	730	kHz
Reference voltage block							
Reference voltage		VREF			1.240		V
Line regulation		V _{LN} REF	V _{CC} = 3V to 15V			10	mV
SYN circuit							
On state voltage		V _{ON} SYN		2.0			V
OFF state voltage		V _{OFF} SYN				0.6	V
Pin input current		I _{IN} SYN	SYN* = 2V			60	μA
Control circuit							
On state voltage		V _{ON} CTL		2.0			V
OFF state voltage		V _{OFF} CTL				0.6	V
Pin input current		I _{IN} STBY	CTL = 2V			60	μA
All circuits							
V _{CC} current consumption		I _{CC}	IN1 ⁻ to IN3 ⁻ = 1V		4.5	6	mA
Standby mode current consumption		I _{OFF}	CTL = 0V, I _{OFF} = I _{CC} + I _{BIAS}			1	μA

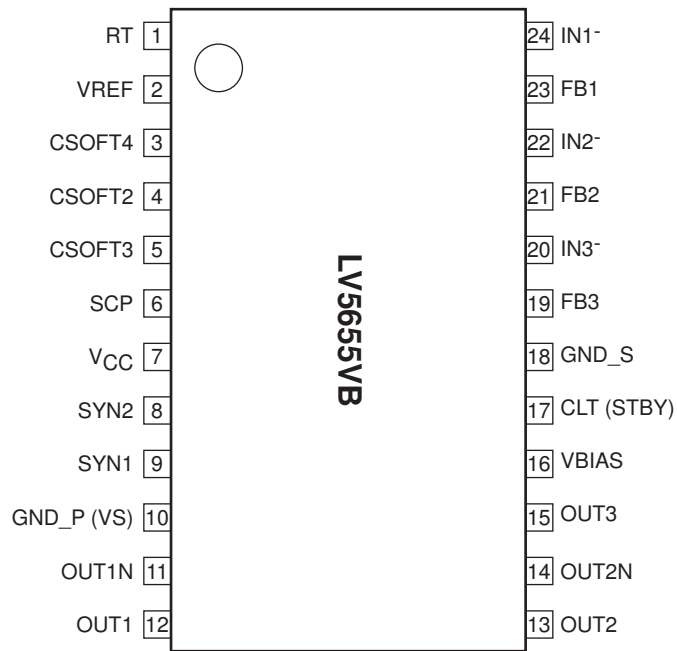
Package Dimensions

unit : mm (typ)

3287

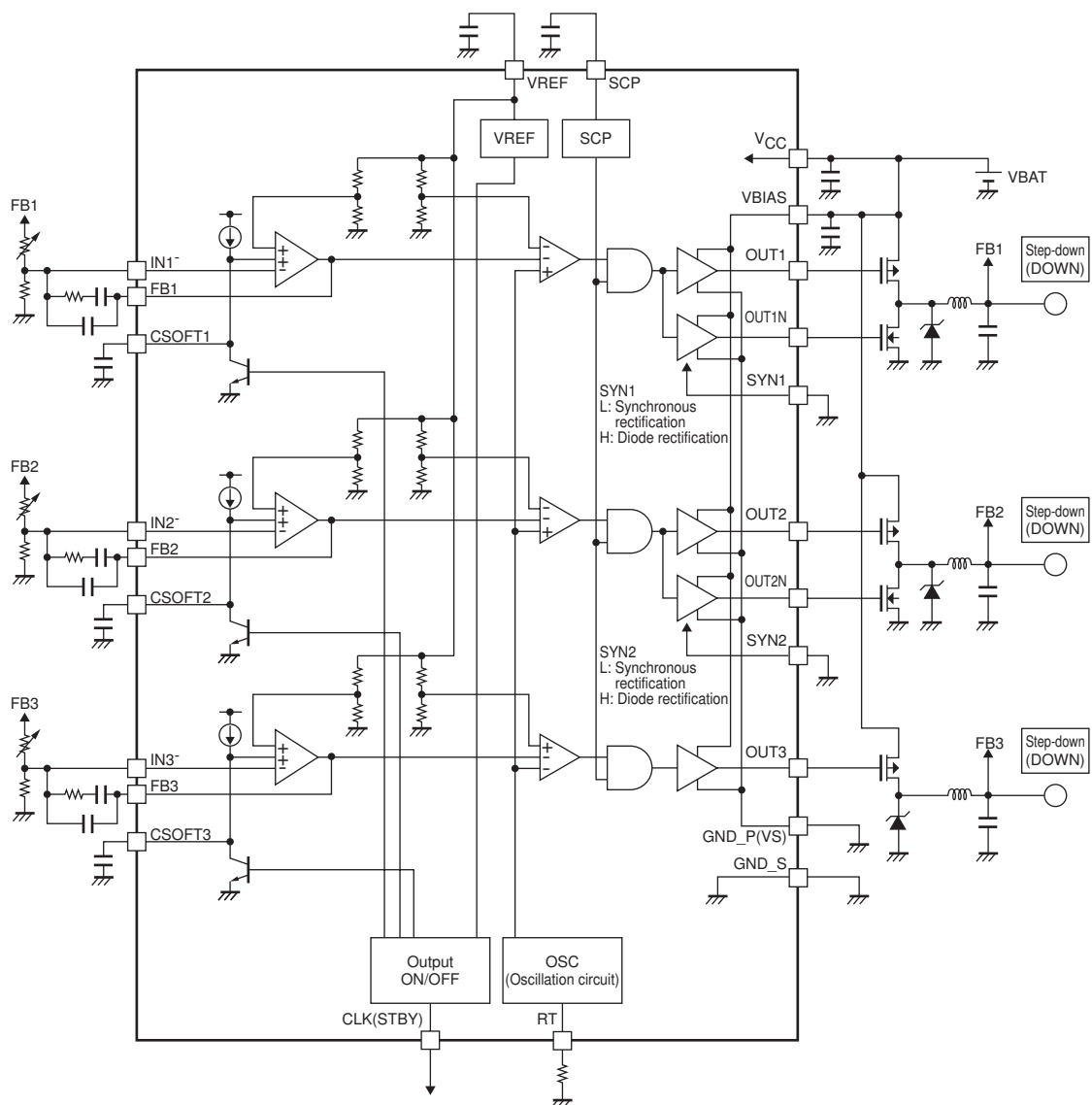


Pin Assignment



Top view

Block Diagram and Sample Application Circuit



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Pin Function

Block	Pin No.	Pin Name	Functions
ch1 (Step-down)	24	IN1 ⁻	Error amplifier, - (Inverting) input.
	23	FB1	Error amplifier output.
	3	CSOFT1	Soft start setting capacitor connection. Connect to GND through a capacitor.
	12	OUT1	Output. External transistor P-channel gate connect.
	11	OUT1N	Output. External transistor N-channel gate connection.
	9	SYN1	Synchronous rectification/diode rectification switching, L : synchronous rectification H : diode rectification.
ch2 (Step-down)	22	IN2 ⁻	Error amplifier, - (Inverting) input.
	21	FB2	Error amplifier output.
	4	CSOFT2	Soft start setting capacitor connection. Connect to GND through a capacitor.
	13	OUT2	Output. External transistor P-channel gate connect.
	14	OUT2N	Output. External transistor N-channel gate connection.
	8	SYN2	Synchronous rectification/diode rectification switching, L : synchronous rectification H : diode rectification.
ch3 (Step-down)	20	IN3 ⁻	Error amplifier, - (Inverting) input.
	19	FB3	Error amplifier output.
	5	CSOFT3	Soft start setting capacitor connection. Connect to GND through a capacitor.
	15	OUT3	Output. External transistor P-channel gate connect.
POWER	7	V _{CC}	Power supply input (signal system).
	16	VBIAS	Power supply input (pre-output stage).
	18	GND_S	Ground (signal system).
	10	GND_P (VS)	Ground (pre-output stage).
CONTROL	2	VREF	Reference voltage output. Connect to GND through a capacitor.
	17	CTL (STBY)	Output control, H : all outputs ON, L : all outputs off.
	6	SCP	Connection pin for the delay time setting capacitor of short-circuit detection circuit (connect to GND).
OSC	1	RT	Oscillation frequency setting resistor connection (connect to GND).

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Equivalent Circuits

Pin No.	Pin Name	Description	Equivalent Circuit
17	CTL	CTL: Controls operation of all circuits. Controls operation of all channels. High : ON Low : OFF	
24 22 20	IN1 ⁻ IN2 ⁻ IN3 ⁻	Error amplifier inverting input. The regulator output is divided by a resistor and connected to IN ⁺	
23 21 19	FB1 FB2 FB3	Error amplifier output. These pins, in combination with IN ⁺ , configure the error amplifier filters	
3 4 5	CSOFT1 CSOFT2 CSOFT3	Soft start. Connect to GND via a capacitor to set the soft start time.	
12 13 15	OUT1 OUT2 OUT3	Output. Connect external PchFET.	
11 14	OUT1N OUT2N	Output. Connect external NchFET.	

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Pin No.	Pin Name	Description	Equivalent Circuit
1	RT	Sets the oscillation frequency. Connect to GND through a resistor. Constant voltage output (0.56V typ.)	
6	SCP	Connect to GND via a capacitor to set the short circuit detection circuit delay time.	
9 8	SYN1 SYN2	Channel 1 and channel 2 synchronous/diode rectification switching. Low : Synchronous rectification High : Diode rectification Switching operates independently for the corresponding channel.	<p>SYN* L : Synchronous rectification H : Diode rectification</p>
23	VREF	Internal constant voltage circuit output. Connect a stabilizing capacitor.	
7	V _{CC}	Signal system power supply	V _{CC} ○ ———
16	VBIAS	Power system power supply (Output stage)	VBIAS ○ ———
18	GND_S	Signal system GND	GND_S ○ ———
10	GND_P (VS1)	Output stage GND (pre-stage)	GND_P (VS) ○ ———

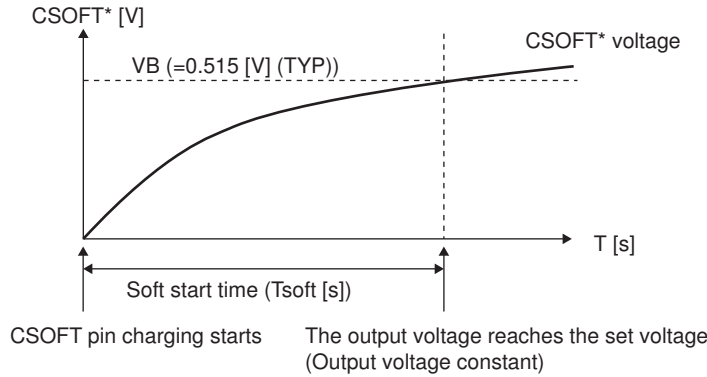
Notes

(1) Soft start time setting method

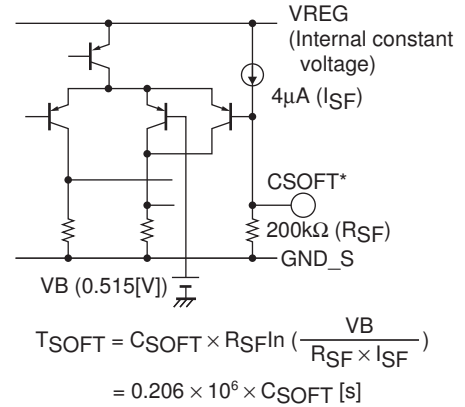
The soft start time is set with the capacitor connected between CSOFT* and GND_S.

This IC has an independent soft start function for each channel, so a capacitor must be connected for each CSOFT to set the soft start time.

(Description of soft start operation)



(Outline of soft start pin)



(2) Setting the oscillation frequency

The oscillation frequency is set by the resistor (RT resistor) connected to the RT pin.

The RT pin is a constant voltage (0.56 [V] typ.) output, and the oscillation frequency is determined by the current run through the RT resistor and charging/discharging of the internal capacitor.

$$f_{OSC} \text{ [kHz]} = \frac{12 \times 1E3}{RT \text{ [k}\Omega\text{]}} \quad (\text{Reference calculation formula})$$

The internal oscillation frequency deviates from the calculated value due to overshoot, undershoot and other factors, so the frequency should be confirmed in an actual set.

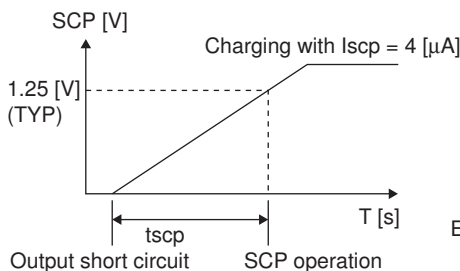
(3) SCP (short circuit protection) function

• Description of operation

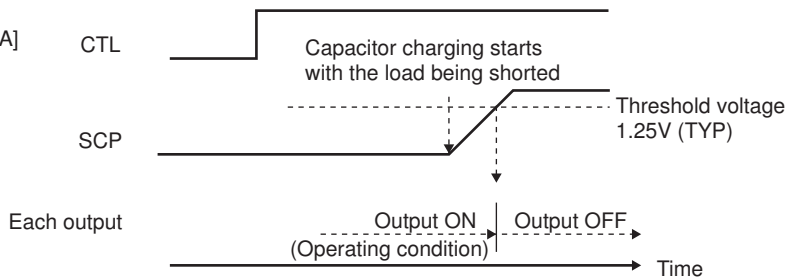
When any one of FB1 to FB4 goes High due to the load being shorted or other reason, charging to the SCP pin starts. If output does not recover during the set time T_{scp} and SCP pin voltage exceeds the threshold voltage, the protective circuit (SCP) operates and all channel outputs are turned OFF. All outputs are latched off by the protection circuit (SCP). This latched state (output OFF) is canceled by setting the CTL pin Low or by turning the power supply OFF. When not using the protection function (SCP), the SCP pin must be shorted to GND_S with a line that is as short as possible.

The SCP operation time is set by the capacitor connected to the SCP pin.

(SCP charging operation)



(SCP function)



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