



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV5604TA — Bi-CMOS LSI Eight-Channel Switching Regulator Controller

Overview

The LV5604TA is a eight-channel switching regulator controller.

Features

- Low-voltage (3V) operation
- Independent standby functions for each of the eight channels
- Synchronous rectification : channel 1 and channel 2
- Reference voltage precision : $\pm 1\%$
- Is capable of driving MOS transistors
- Supports inverting step-up operation.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		16	V
Allowable power dissipation	$P_d\text{ max}$		1	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		3 to 15	V
Supply voltage	V_{BIAS}		3 to 15	V
Timing resistor	RT		7 to 30	$k\Omega$
Timing capacitor	CT		100 to 1000	pF
Triangle wave frequency	f_{OSC}		0.1 to 1.3	MHz

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment. The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for new introduction or other application different from current conditions on the usage of automotive device, communication device, office equipment, industrial equipment etc. , please consult with us about usage condition (temperature, operation time etc.) prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

<http://semicon.sanyo.com/en/network>

LV5604TA

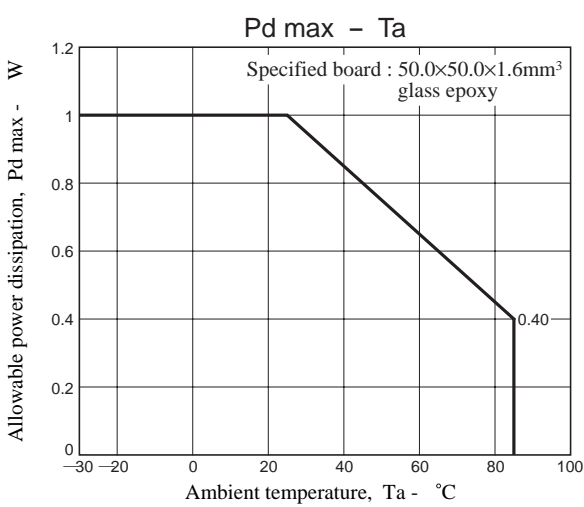
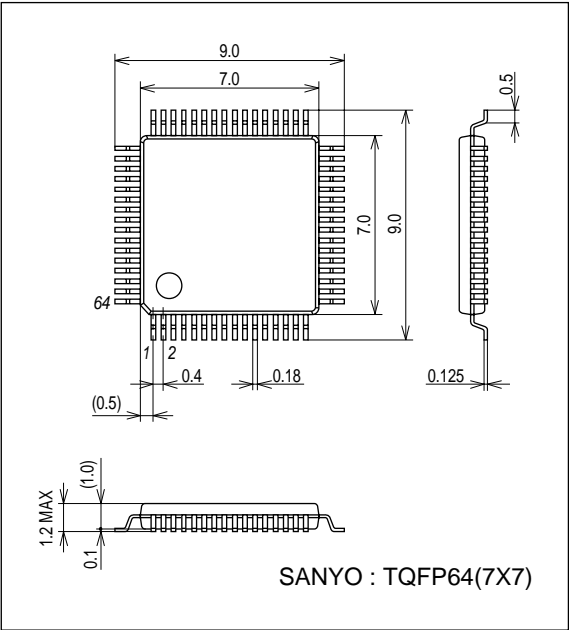
Electrical Characteristics at $T_a = 25^{\circ}\text{C}$, $V_{CC} = V_{BIAS} = 3.6\text{V}$, $SCP = 0\text{V}$

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Error amplifier 1							
IN ⁺ pin internal bias voltage		V _B	Value added to the error amplifier offset at the error amplifier + side voltage	0.509	0.515	0.521	V
Output low voltage	ch1 to ch8	V _{Low} FB	IN ⁻ = 2.0V, IFB = 20μA			0.2	V
Output high voltage	ch1 to ch8	V _{Hi} FB	IN ⁻ = 0V IFB1 = -20μA	2.0			V
Error amplifier 2							
IN5 ⁻ RE pin offset voltage		VOF		-6		6	mV
Output low voltage		V _{Low} FB5RE	IN5 ⁻ RE = 2.0V, IFB = 20μA			0.2	V
Output high voltage		V _{Hi} FB5RE	FB5RE ; H, IFB = 500μA	1.95			V
Protection circuit							
Threshold voltage		V _{SCP}		1.1	1.25	1.4	V
SCP pin current		I _{SCP}			4		μA
Short circuit detection signal pin		VSCPOUT	Open collector ISCPOUT = 100μA			0.2	V
Software start block (ch1 to ch8)							
Soft start current	ch1 to ch8	I _{SF}	CSOFT1 to 8 = 0V	3.2	4	4.8	μA
Soft start resistance	ch1 to ch8	R _{SF}		160	200	240	kΩ
Fixed duty							
Maximum on duty 1	ch1 to ch4	Duty MAX 1 to 4	Out monitor, IN ⁻ = 0V	100			%
Maximum on duty 2	ch5	Duty MAX 5	Out monitor, IN ⁻ = 0V	80	85	90	%
Maximum on duty 3	ch6 to ch8	Duty MAX 6 to 8	Out monitor, IN ⁻ = 0V	80	85	90	%
Output block 1 to 6							
OUT pin high side on resistance		R _{OUT} SOUR	I _O = 10mA		25		Ω
OUT pin high side on resistance		R _{OUT} SINK	I _O = 10mA		10		Ω
Triangle wave oscillator block							
Current setting pin voltage		V _T RT	RT = 10kΩ		0.57		V
Output current		I _{OH} CT			220		μA
Output current ratio		ΔI _O CT	CT pin, ISOURCE/ISINK		2.5		
Oscillation frequency		f _{OSC1}	RT = 10kΩ, CT = 270pF	390	490	570	kHz
Reference voltage block							
Reference voltage		V _{REF}			1.230		V
Line regulation		V _{LN} REF	V _{CC} = 3V to 15V			10	mV
Control circuit							
On state voltage		V _{ON} CTL		2.0			V
OFF state voltage		V _{OFF} CTL				0.6	V
Pin input current		I _{IN} CTL	VCTL = 2V			60	μA
Standby circuit							
On voltage		V _{ON} STBY		2.0			V
Off voltage		V _{OFF} STBY				0.6	V
Pin input current		I _{IN} STBY	VSTBY = 2V			60	μA
All circuits							
V _{CC} current consumption		I _{CC}	IN1 ⁻ to IN8 ⁻ = 1V		6	7.5	mA
Standby mode current consumption		I _{OFF}	VSTBY = VCTL = 0V I _{OFF} = I _{CC} + I _{BIAS}			1	μA

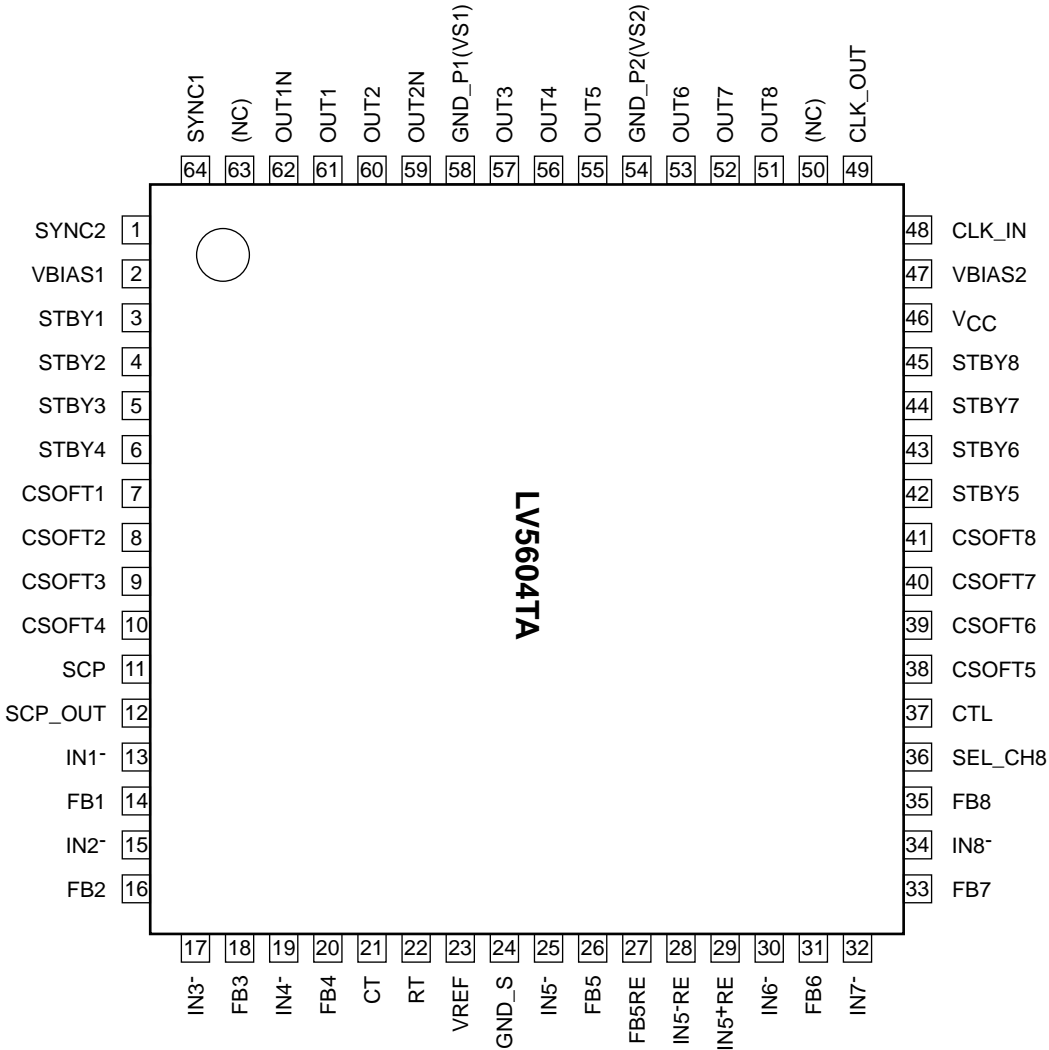
Package Dimensions

unit : mm (typ)

3425

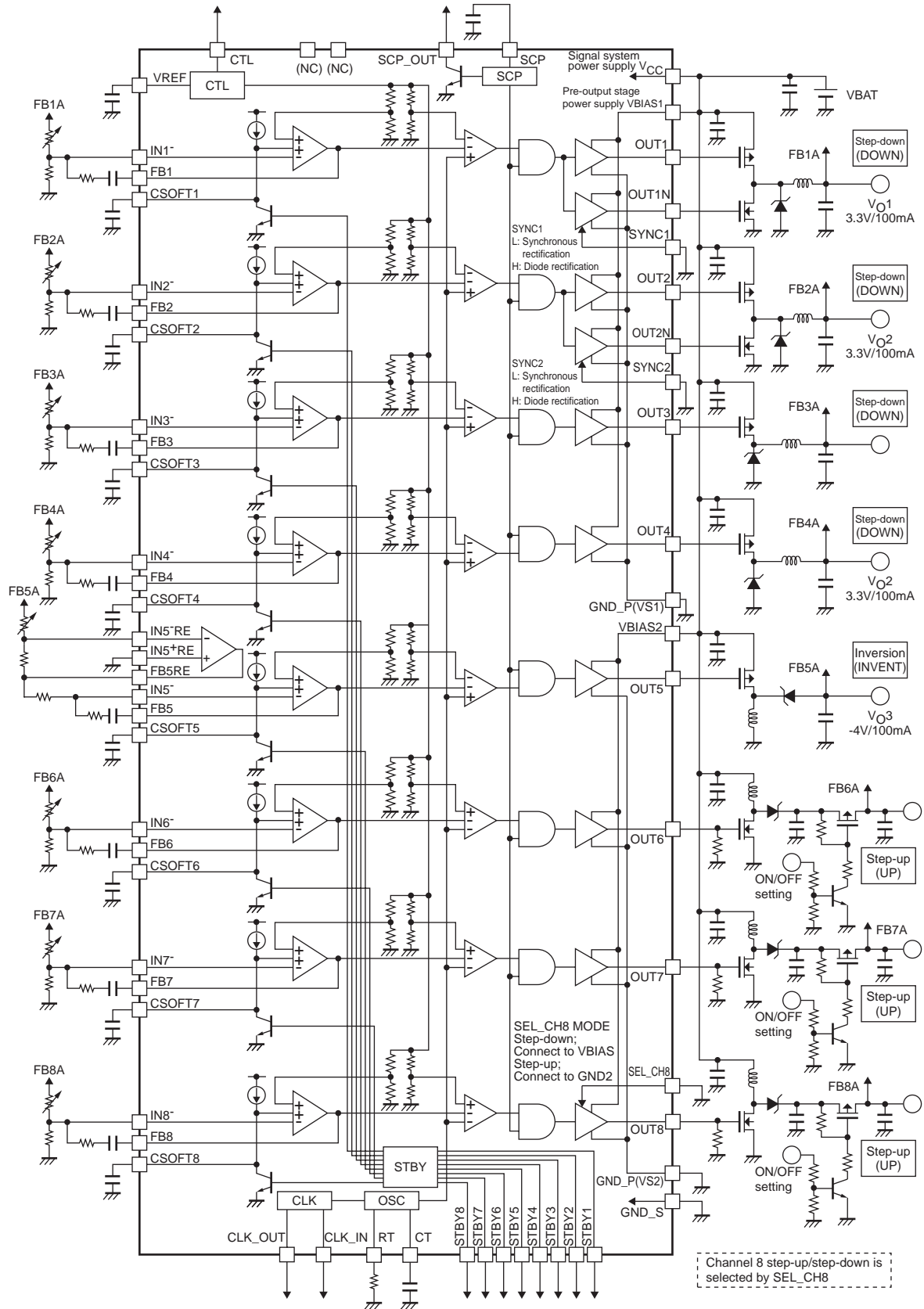


Pin Assignment



Top view

Block Diagram and Sample Application Circuit



LV5604TA

Pin Function

Block	Pin No.	Pin Name	Functions
ch1 (Step-down)	3	STBY1	Standby input. H/ch1 ; ON, L/ch1 ; OFF
	13	IN1 ⁻	Error amplifier Inverting input
	14	FB1	Error amplifier output
	61	OUT1	Output. External transistor P-channel gate connect
	62	OUT1N	Output. External transistor N-channel gate connection
	7	CSOFT1	Soft start setting capacitor connection. Connect to GND through a capacitor.
ch2 (Step-down)	4	STBY2	Standby input. H/ch2 ; ON, L/ch2 ; OFF
	15	IN2 ⁻	Error amplifier Inverting input
	16	FB2	Error amplifier output
	60	OUT2	Output. External transistor P-channel gate connection
	59	OUT2N	Output. External transistor N-channel gate connection
	8	CSOFT2	Soft start setting capacitor connection. Connect to GND through a capacitor.
ch3 (Step-down)	5	STBY3	Standby input. H/ch3 ; ON, L/ch3 ; OFF
	17	IN3 ⁻	Error amplifier Inverting input
	18	FB3	Error amplifier output
	9	CSOFT3	Soft start setting capacitor connection. Connect to GND through a capacitor.
	57	OUT3	Output. External transistor P-channel gate connection
ch4 (Step-down)	6	STBY4	Standby input. H/ch4 ; ON, L/ch4 ; OFF
	19	IN4 ⁻	Error amplifier Inverting input
	20	FB4	Error amplifier output
	10	CSOFT4	Soft start setting capacitor connection. Connect to GND through a capacitor.
	56	OUT4	Output. External transistor P-channel gate connection
ch5 (Inversion)	42	STBY5	Standby input. H/ch5 ; ON, L/ch5 ; OFF
	28	IN5 ⁻ RE	Inversion step-up error amplifier, - (Inverting) input
	29	IN5 ⁺ RE	Inversion step-up error amplifier, + (noninverting) input
	27	FB5RE	Inversion step-up error amplifier output
	25	IN5 ⁻	Error amplifier Inverting input
	26	FB5	Error amplifier output
	38	CSOFT5	Soft start setting capacitor connection. Connect to GND through a capacitor.
	55	OUT5	Output. External transistor P-channel gate connection
ch6 (Step-up)	43	STBY6	Standby input. H/ch6 ; ON, L/ch6 ; OFF
	30	IN6 ⁻	Error amplifier Inverting input
	31	FB6	Error amplifier output
	39	CSOFT6	Soft start setting capacitor connection. Connect to GND through a capacitor.
	53	OUT6	Output. External transistor N-channel gate connection
ch7 (Step-up)	44	STBY7	Standby input. H/ch7 ; ON, L/ch7 ; OFF
	32	IN7 ⁻	Error amplifier Inverting input
	33	FB7	Error amplifier output
	40	CSOFT7	Soft start setting capacitor connection. Connect to GND through a capacitor.
	52	OUT7	Output. External transistor N-channel gate connection
ch8 (Step-down) (Step-up)	45	STBY8	Standby input. H/ch8 ; ON, L/ch8 ; OFF
	34	IN8 ⁻	Error amplifier Inverting input
	35	FB8	Error amplifier output
	41	CSOFT8	Soft start setting capacitor connection. Connect to GND through a capacitor.
	51	OUT8	Output. External transistor (Step-up / N-channel, Step-down / P-channel) gate connection

Continued on next page.

LV5604TA

Continued from preceding page.

Block	Pin No.	Pin Name	Functions
MODE	64	SYNC1	Synchronous rectification/diode rectification switching, L : synchronous rectification H : diode rectification
	1	SYNC2	Synchronous rectification/diode rectification switching, L : synchronous rectification H : diode rectification
	36	SEL_CH8	Channel 8 step-up/step-down switching, L (GND) : step-up H (VBIAS2) : step-down
POWER	46	V _{CC}	Power supply input (signal system)
	2	VBIAS1	Power supply input (ch1 to ch4, pre-output stage)
	47	VBIAS2	Power supply input (ch5 to ch8, pre-output stage)
	24	GND_S	Ground (signal system)
	58	GND_P1 (VS1)	Ground (ch1 to ch4, pre-output stage)
	54	GND_P2 (VS2)	Ground (ch5 to ch8, pre-output stage)
	23	VREF	Reference voltage output
CONTROL	37	CTL	Power supply control
	11	SCP	Connection pin for the delay time setting capacitor of short circuit detection circuit
	12	SCP_OUT	Short circuit detection circuit output
OSC	21	CT	Triangle wave oscillation frequency setting capacitor connection
	22	RT	Triangle wave oscillation frequency setting resistor connection
	48	CLKIN	External clock input
	49	CLKOUT	Clock output
OTHER	63	(NC)	No connection
	50	(NC)	No connection

LV5604TA

Equivalent Circuits

Pin No.	Pin Name	Description	Equivalent Circuit
37 3 4 5 6 42 43 44 45	CTL STBY1 STBY2 STBY3 STBY4 STBY5 STBY6 STBY7 STBY8	CTL : Controls operation of all channels. STBY* : Independently controls operation of the corresponding channel. Operation is high active. High : Circuit operation ON Low : Circuit operation OFF	
13 15 17 19 25 30 32 34	IN1- IN2- IN3- IN4- IN5- IN6- IN7- IN8-	Error amplifier inverting input. The regulator output is divided by a resistor and connected to IN*-	
14 16 18 20 26 31 33 35	FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8	Error amplifier output. These pins, in combination with IN*-, configure the error amplifier filters	
29 28	IN5+RE IN5-RE	Inversion step-up (Channel 5) error amplifier input. These pins, in combination with FB5R, configure the operational amplifier (independent)	
27	FB5RE	Inversion step-up (Channel5) error amplifier output. This pin, in combination with IN5+RE and IN5-RE, configures the operational amplifier (independent).	
7 8 9 10 38 39 40 41	CSOFT1 CSOFT2 CSOFT3 CSOFT4 CSOFT5 CSOFT6 CSOFT7 CSOFT8	Soft start. Connect to GND via a capacitor to set the soft start time.	

Continued on next page.

LV5604TA

Continued from preceding page.

Pin No.	Pin Name	Description	Equivalent Circuit
61 62 60 59 57 56 55 53 52 51	OUT1 OUT1N OUT2 OUT2N OUT3 OUT4 OUT5 OUT6 OUT7 OUT8	Output. Connect external FET.	
22	RT	Connect to GND through a resistor. This pin, together with CT, sets the oscillation frequency.	
21	CT	Connect to GND through a capacitor. This pin, together with RT, sets the oscillation frequency.	
11	SCP	Connect to GND via a capacitor to set the short circuit detection circuit delay time.	
12	SCP_OUT	Short circuit detection circuit output. When SCP exceeds the threshold voltage, the open collector goes OFF and this pin goes High.	

Continued on next page.

LV5604TA

Continued from preceding page.

Pin No.	Pin Name	Description	Equivalent Circuit
23	VREF	Internal constant voltage circuit output. Connect a stabilizing capacitor.	<p>VREF (Internal constant voltage)</p> <p>GND_S</p>
48	CLK_IN	External clock input. Apply an external clock of the internal oscillation frequency or higher.	<p>VREG (Internal constant voltage)</p> <p>CLKIN</p> <p>300Ω</p> <p>GND_S</p>
49	CLK_OUT	Clock output. This outputs the internal or external clock frequency pulse.	<p>VREG (Internal constant voltage)</p> <p>CLKOUT</p> <p>300Ω</p> <p>300Ω</p> <p>GND_S</p>
64 1	SYNC1 SYNC2	Channel 1 and channel 2 synchronous/diode rectification switching. Low : Synchronous rectification High : Diode rectification Switching operates independently for the corresponding channel.	<p>VREG (Internal constant voltage)</p> <p>SYNC*</p> <p>120kΩ</p> <p>30kΩ</p> <p>GND_S</p> <p>SYNC* L : Synchronous rectification H : Diode rectification</p>
36	SEL_CH8	Channel 8 step-up/step-down switching. High : Sets step-down Low : Sets step-up	<p>VBIAS2</p> <p>SEL_CH8</p> <p>GND_P2 (VS2)</p> <p>Channel 8 step-up/step-down switching H (VBIAS2) : step-down, L (GND) : step-up</p>

Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Description	Equivalent Circuit
46	V _{CC}	Signal system power supply	V _{CC} ○ —
2 47	VBIAS1 VBIAS2	Power system power supply (Output stage)	VBIAS* ○ —
24	GND_S	Signal system GND	GND_S ○ —
58 54	GND_P1 (VS1) GND_P2 (VS2)	Output stage GND (Output stage GND)	GND_P*(VS*) ○ —
50 63	(NC) (NC)	Use prohibited (Not connected pins)	(NC) ○

Notes

(1) Channel 8 step-up/step-down selection function

The channel 8 step-up or step-down converter selection is made by the SEL_8CH pin connection.

Step-up/step-down is selected by SEL_CH8, but this selection cannot be switched during use, and is fixed to either step-up or step-down in the design stage. In addition, unlike other channels, channel 8 is not connected internally to a pull-up/pull-down resistor, so an external resistor must be connected instead.

(Mode selection using SEL_CH8)

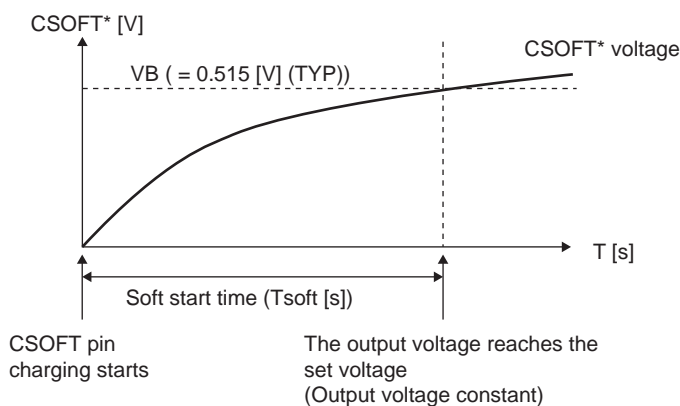
Selected mode	SEL_CH8 connection	OUT8 resistor connection
Step-down (DOWN converter)	VBIAS2	Connect to VBIAS2 via a resistor (between the PchTr gate and VBIAS2)
Step-up (UP converter)	GND_P2 (VS2)	Connect to GND_P2 (VS2) via a resistor (between the NchTr gate and GND_P2 (VS2))

(2) Soft start time setting method

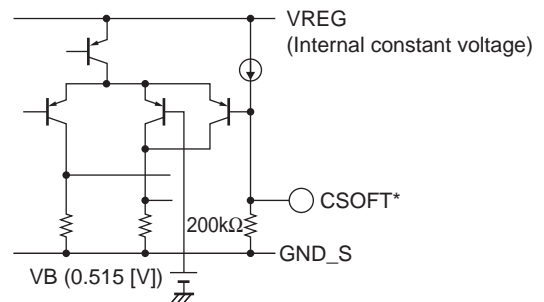
The soft start time is set with the capacitor connected between CSOFT* and GND_S.

This IC has an independent soft start function for each channel, so a capacitor must be connected for each channel to set the soft start (time).

(Description of soft start operation)



(Outline of soft start pin)



(3) Setting the oscillation frequency

The internal oscillation frequency is set by the resistor connected to the RT pin and the capacitor connected to the CT pin. The waveform generated on CT is a triangular wave with the charging/discharging waveform determined by RT and CT.

$$f_{OSC} = \frac{1}{CT \times RT} \text{ [Hz]}$$

The actual internal oscillation frequency deviates from the calculated value due to overshoot, undershoot and other factors, so the frequency should be confirmed in an actual set.

(4) External input CLK function (CLK_IN)

Switching operation can be synchronized with external clock input (CLK_IN) by using the CLK_IN pin.

- External clock (CLK_IN) frequency and input level

When using external clock (CLK_IN) input, input a frequency equal to the internal oscillation frequency +20% or more to CLK_IN. In addition, the CLK_IN configuration is shown in the figure “CLK_IN (input) equivalent circuit (outline)” below.

The 0.8V reference voltage and CLK_IN are compared to determine the edges, so input a signal of 0.8V or more (V_{CC} voltage or less) as the external clock (CLK_IN).

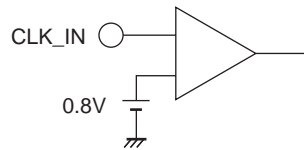
- External/internal clock switching

Set the CTL pin Low before switching between the external clock and the internal clock.

- Maximum ON duty

The maximum ON duty (Duty_MAX*) of channel 1 to channel 4 is the 85% (typ.) setting. When using the external clock (CLK_IN), the maximum ON duty (Duty_MAX*) becomes smaller, so care must be taken for the set output voltage.

(CLK_IN (input) equivalent circuit (outline))



(5) SCP function

- Description of operation

When FB1 to FB8 go High due to the load being shorted or other reason, charging to the SCP pin starts, and if output does not recover during the set time T_{scp} , the protective circuit (SCP) operates. When the protection circuit (SCP) operates, all channel outputs are turned OFF. When not using the protection function (SCP), the SCP pin must be shorted to GND_S with a line that is as short as possible.

When the SCP function operates and SCP_OUT goes High, all outputs are latched OFF. This latched state is canceled by setting the CTL pin Low or by turning the power supply off.

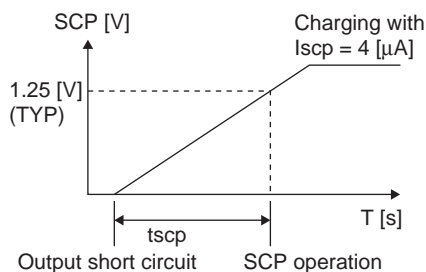
- SCP_OUT

The SCP_OUT pin functions to notify an external microcontroller or other component of the SCP (short circuit protection) and CTL status. The output configuration is an open drain output, and a pull-up resistor is used. When not used, leave this pin open.

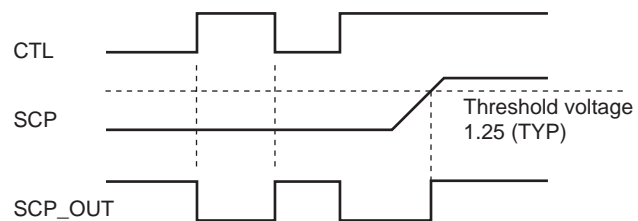
- Switching time

The SCP_OUT switching time is set by the capacitor connected to the SCP pin.

(SCP charging operation)



(SCP and SCP_OUT operation)



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of March, 2012. Specifications and information herein are subject to change without notice.