



SANYO Semiconductors

## DATA SHEET

# LV5749NV — Bi-CMOS LSI 1-channel Step-down Switching Regulator

## Application

The LV5749NV is a 1-channel step-down switching regulator.

## Functions

- 1 channel step-down switching regulator controller.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Synchronous rectification.
- Current mode control.
- Synchronous drive by external signal.

## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	$V_{IN\ max}$		45	V
Allowable Power dissipation	$P_d\ max$	Mounted on a specified board. *	0.74	W
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\* : When mounted on the specified printed circuit board (114.3mm x 76.1mm x 1.6mm), glass epoxy

### Recommended Operating Range at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	$V_{IN}$		8.5 to 42	V
Error amplifier input voltage			0 to 1.6	V

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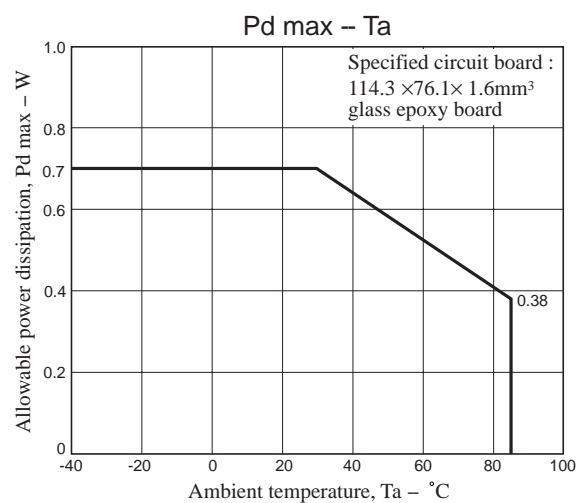
# LV5749NV

## Electrical Characteristics at Ta = 25°C, VIN = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A	0.654	0.67	0.686	V
5V power supply	VDD	IOUT = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	FOSC	RT = 220kΩ	110	125	140	kHz
Frequency variation	FOSC DV	VIN = 8.5 to 42V		1		%
ON/OFF circuit block						
IC start-up voltage	VEN on		2.5	3.0	3.5	V
IC off voltage	VEN off		1.1	1.3	1.5	V
Soft start circuit block						
Soft start source current	ISS SC	EN > 3.5V	4	5	6	μA
Soft start sink current	ISS SK	EN < 1V, VDD=5V		2		mA
UVLO circuit block						
UVLO lock release voltage	VUVLO		7.5	8.0	8.5	V
UVLO hysteresis	VUVLO H			0.7		V
OCP circuit block						
OCP charge current	I <sub>OCP</sub>			5		μA
Error amplifier						
Input bias current	I <sub>EA IN</sub>				100	nA
Error amplifier transconductance	G <sub>EA</sub>		1000	1400	1800	μA/V
Sink output current	I <sub>EA OSK</sub>	FB = 1.0V		-100		μA
Source output current	I <sub>EA OSC</sub>	FB = 0V		100		μA
Current detection amplifier gain	G <sub>ISNS</sub>			1.5		
Over current limiter circuit block						
Reference current 1	I <sub>LIM1</sub>	MODE = L (GND)	-10%	18.5	+10%	μA
Reference current 2	I <sub>LIM2</sub>	MODE = H (VIN)	-10%	37.0	+10%	μA
Over current detection comparator offset voltage	V <sub>LIM OFS</sub>		-5		+5	mV
Over current detection comparator common mode input range			V <sub>IN</sub> -0.45		V <sub>IN</sub>	V
PWM comparator						
Input threshold voltage (fosc = 125kHz)	Vt max	Duty cycle = DMAX	0.9	1.0	1.1	V
	Vt0	Duty cycle = 0%	0.4	0.5	0.6	V
Maximum ON duty	DMAX		80	85	90	%
Output block						
Output stage ON resistance (the upper side)	R <sub>ONH</sub>			5		Ω
Output stage ON resistance (the under side)	R <sub>ONL</sub>			5		Ω
Output stage ON current (the upper side)	I <sub>ONH</sub>		240			mA
Output stage ON current (the under side)	I <sub>ONL</sub>		240			mA
The whole device						
Standby current	I <sub>CCS</sub>	EN < 1V			10	μA
Mean consumption current	I <sub>CCA</sub>	EN > 3.5V		3		mA

## Package Dimensions

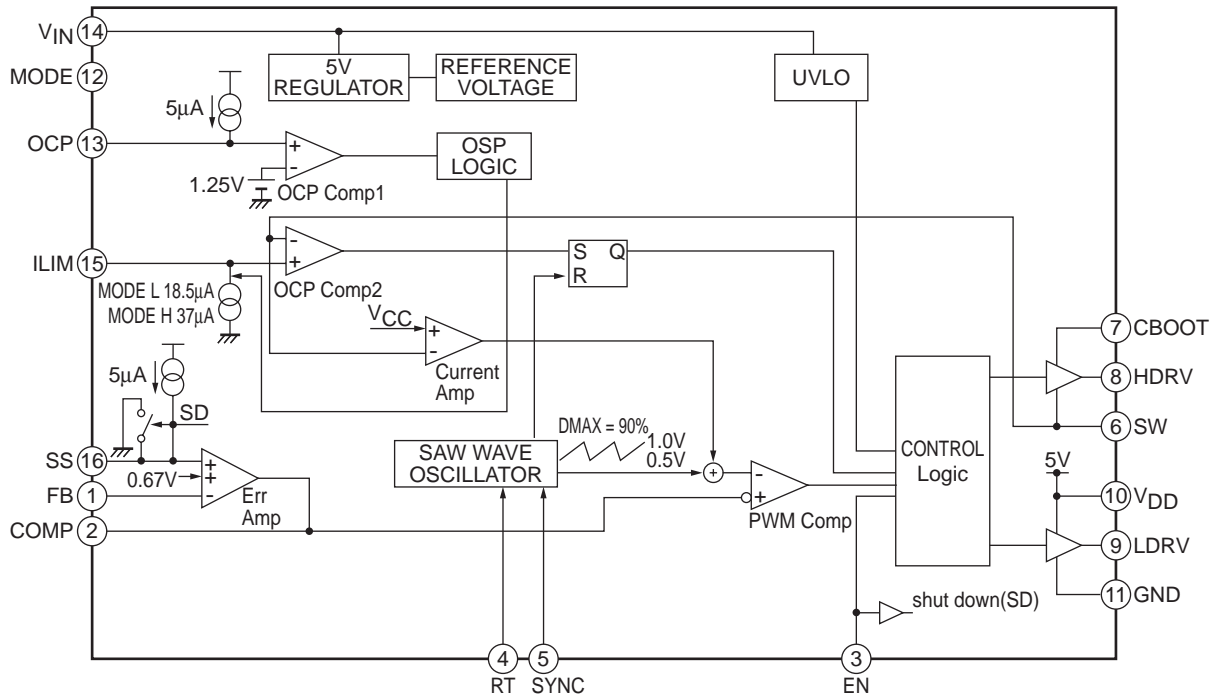
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Pin diagram of the LV5749NV IC. The chip is a square package with 16 pins. The pin numbers and functions are as follows:

Pin Number	Function
1	FB
2	COMP
3	EN
4	RT
5	SYNC
6	SW
7	CBOOT
8	HDRV
9	LDRV
10	V <sub>DD</sub>
11	GND
12	MODE
13	OCP
14	V <sub>IN</sub>
15	ILIM
16	SS

## Block Diagram



## Pin Function

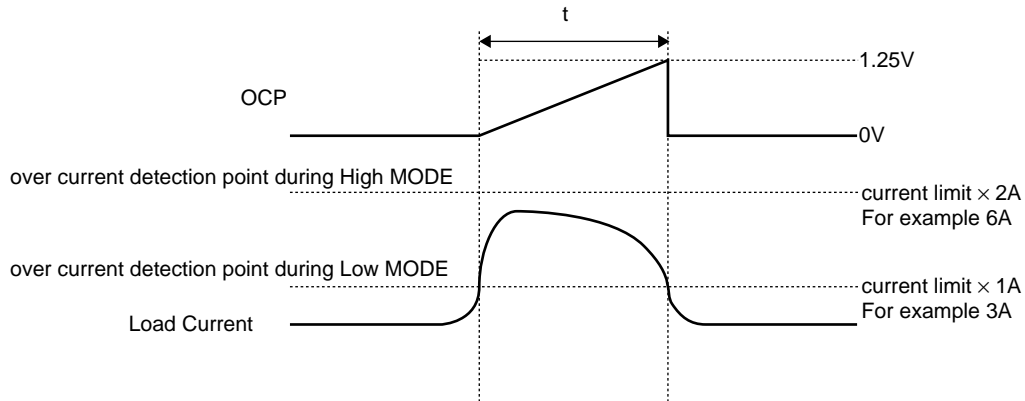
Pin No.	Pin name	Description
14	$V_{IN}$	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.7V or more by UVLO function, The IC starts and the soft start function operates.
11	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
10	$V_{DD}$	Power supply pin for an external the lower MOS-FET gate drive.
7	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypass capacitor between CBOOT and SW.
6	SW	Pin to connect with switching node. The source of NchMOSFET connects to this pin.
5	SYNC	External synchronous signal input pin.
9	LDRV	An external the lower MOSFET gate drive pin.
8	HDRV	An external the upper MOSFET gate drive pin.
1	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.67V. The voltage in which the output voltage is divided by an external resistance is applied to this pin.
2	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
16	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5μA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active.
15	ILIM	Reference current pin for current detection. The sink current of about 20μA flows to this pin when Low level (GND) is set to the MODE pin. Also, the sink current of about 40μA flows to this pin when High level ( $V_{IN}$ ) is set to the MODE pin. When a resistance is connected between this pin and $V_{IN}$ outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse.
3	EN	ON/OFF pin.
13	OCP	Pin to set the time of the timer (during double the over current detection point) Connect a capacitor between this pin and GND. OCP charge current : 5μA
4	RT	Pin to set the oscillation frequency. Connect a resistance between this pin and GND.
12	MODE	Pin to switch the over current detection point. Set by the low level (GND) of the ILIM pin. Set by the high level ( $V_{IN}$ ) of the OCP pin. When this MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value. Also, when the MODE pin is set to the low level, the point of the over current detection remains an original value.

### Timing Chart

When the MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value.

Also, when the MODE pin is set to the low level, the point of over current detection remains an original value.

Timing chart of the over current detection point switching is as below.



### Setting Chart

#### 1. Output voltage setting

- Setting of the output voltage VOUT is as follows.

$$V_{OUT} = 1 + \frac{R4}{R3} \times V_{REF} = 1 + \frac{R4}{R3} \times 0.67(\text{typ}) [\text{V}]$$

#### 2. Soft Start setting

- Setting of capacitor C5 is as follows.

$$C5 = \frac{I_{ss} \times T_{ss}}{V_{REF}} = \frac{5\mu \times T_{ss}}{0.67} [\text{F}]$$

I<sub>ss</sub> : Charge current value.

T<sub>ss</sub> : Soft Start time

#### 3. OCP Timer setting

- Setting of OCP timer capacitor C11 is as follows.

$$C11 = \frac{I_{ocp} \times T_{ocp}}{V_{ocp \text{ comp1}}} = \frac{5\mu \times T_{ocp}}{1.3} [\text{F}]$$

I<sub>ocp</sub> : Charge current value.

T<sub>ocp</sub> : OCP time

#### 4. Current limiter setting

- Setting of the current limiter set resistance R5 is as follows.

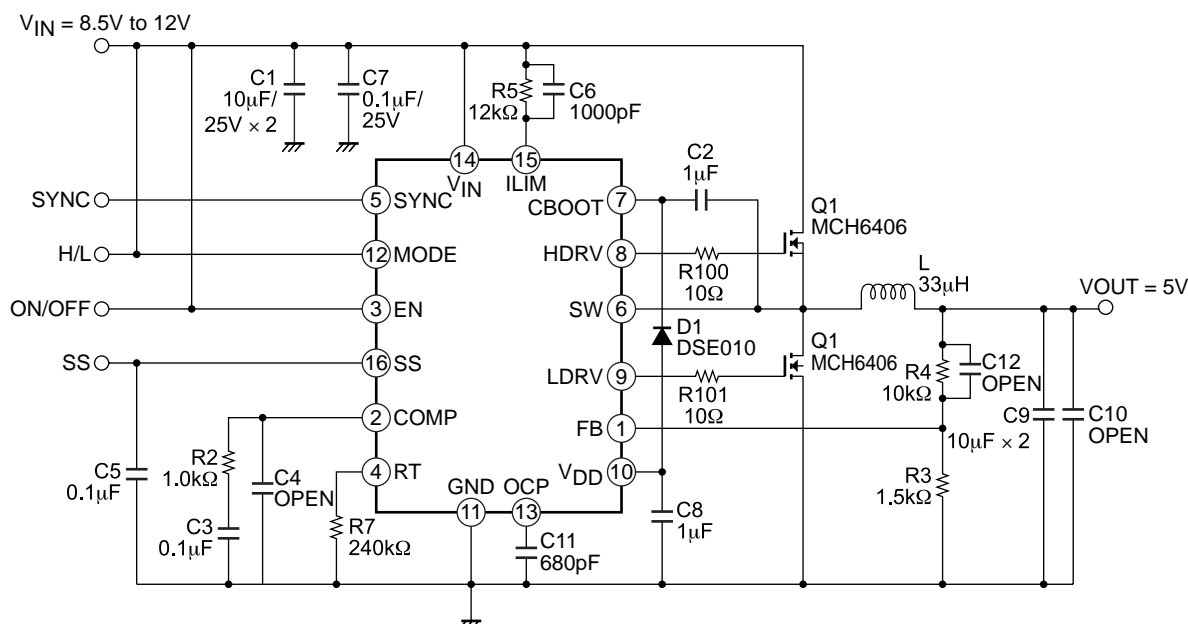
$$R5 = \frac{R_{dson} \times I_{out}}{I_{lim}} = \frac{R_{dson} \times I_{L \text{ max}}}{18.5\mu} [\Omega]$$

I<sub>lim</sub> : ILIM current value.

I<sub>L</sub> : inductance current value

R<sub>dson</sub> : ON resistance value between Q1 drain-sources.

## Sample Application Circuit



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