



SANYO Semiconductors

## DATA SHEET

An ON Semiconductor Company

Bi-CMOS LSI

# LV5725JA — Step-down Switching Regulator

## Overview

The LV5725JA is a step-down voltage switching regulator.

## Functions

- Wide input dynamic range: 4.5V to 50V.
- Built-in pulse-by-pulse OCP circuit: detection is on resistance of an external MOS.
- Over current protection: HICCUP mode.
- Load-independent soft start circuit
- Synchronous operation by external signal.
- External voltage is usable when output voltage is high.
- Current mode type.
- Thermal shutdown.
- ON/OFF pin
- Power good pin

## Specifications

**Absolute Maximum Ratings** at Ta = 25°C

| Parameter                   | Symbol                           | Conditions                      | Ratings              | Unit |
|-----------------------------|----------------------------------|---------------------------------|----------------------|------|
| Supply voltage              | V <sub>IN</sub> max              |                                 | 55                   | V    |
| Allowable pin voltage       | V <sub>IN</sub> , SW, OUT, PGOOD |                                 | 55                   | V    |
|                             | HDRV, CBOOT                      |                                 | 61                   | V    |
|                             | LDRV                             |                                 | 6.0                  | V    |
|                             | Between CBOOT to SW              |                                 | 6.0                  | V    |
|                             | Between CBOOT to HDRV            |                                 |                      |      |
|                             | EN, ILIM                         |                                 | V <sub>IN</sub> +0.3 | V    |
|                             | Between V <sub>IN</sub> to ILIM  |                                 | 1.0                  | V    |
|                             | V <sub>DD</sub>                  |                                 | 6.0                  | V    |
|                             | SS, FB, COMP, RT, SYNC           |                                 | V <sub>DD</sub> +0.3 | V    |
| Allowable Power dissipation | Pd max                           | Mounted on a specified board. * | 1.45                 | W    |
| Operating temperature       | T <sub>opr</sub>                 |                                 | -40 to +85           | °C   |
| Storage temperature         | T <sub>stg</sub>                 |                                 | -55 to +150          | °C   |

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| Parameter                    | Symbol             | Conditions | Ratings | Unit |
|------------------------------|--------------------|------------|---------|------|
| Maximum junction temperature | T <sub>j</sub> max |            | 150     | °C   |

\* Specified board : 58.0mm × 78.0mm × 1.6mm, fiberglass epoxy printed board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

## Recommended Operating Range at T<sub>a</sub> = 25°C

| Parameter                     | Symbol           | Conditions | Ratings   | Unit |
|-------------------------------|------------------|------------|-----------|------|
| Supply voltage range          | V <sub>IN</sub>  |            | 4.5 to 50 | V    |
| Error amplifier input voltage | V <sub>FB</sub>  |            | 0 to 1.6  | V    |
| Oscillatory frequency         | F <sub>OSC</sub> |            | 50 to 500 | kHz  |

## Electrical Characteristics at T<sub>a</sub> = 25°C, V<sub>IN</sub> = 12V

| Parameter                                                    | Symbol               | Conditions                                             | Ratings               |       |                 | Unit |
|--------------------------------------------------------------|----------------------|--------------------------------------------------------|-----------------------|-------|-----------------|------|
|                                                              |                      |                                                        | min                   | typ   | max             |      |
| <b>Reference voltage block</b>                               |                      |                                                        |                       |       |                 |      |
| Internal reference voltage                                   | V <sub>ref</sub>     | Including offset of E/A                                | 0.698                 | 0.708 | 0.718           | V    |
| 5V power supply                                              | V <sub>DD</sub>      | I <sub>OUT</sub> = 0 to 5mA                            | 4.7                   | 5.2   | 5.7             | V    |
| <b>Triangular waveform oscillator block</b>                  |                      |                                                        |                       |       |                 |      |
| Oscillation frequency                                        | F <sub>OSC</sub>     | RT = 56kΩ                                              | 317                   | 365   | 412             | kHz  |
| Frequency variation                                          | F <sub>OSC</sub> DV  | V <sub>IN</sub> = 4.5 to 50V                           |                       | 1     |                 | %    |
| Fold back detection voltage                                  | V <sub>OSC</sub> FB  | After power is supplied to SS, voltage is detected FB. |                       | 0.5   |                 | V    |
| Fold back oscillation frequency                              | F <sub>OSC</sub> FB  | RT = 56kΩ, V <sub>FB</sub> = 0V                        | 100                   | 130   | 160             | kHz  |
| <b>ON/OFF circuit block</b>                                  |                      |                                                        |                       |       |                 |      |
| IC start-up voltage                                          | V <sub>EN</sub> on   |                                                        | -                     | 2.5   | 3.0             | V    |
| Hysteresis of startup voltage                                | V <sub>EN</sub> hys  |                                                        | 0.3                   | 0.6   | -               | V    |
| <b>Soft start circuit block</b>                              |                      |                                                        |                       |       |                 |      |
| Soft start source current                                    | I <sub>SS</sub> SC   | EN > 3.0V                                              | 4                     | 5     | 6               | μA   |
| Soft start sink current                                      | I <sub>SS</sub> SK   | EN < 1V, V <sub>DD</sub> = 5V                          |                       | 2     |                 | mA   |
| Soft start end voltage                                       | V <sub>SS</sub> END  |                                                        | 0.7                   | 0.9   | 1.1             | V    |
| <b>UVLO circuit block</b>                                    |                      |                                                        |                       |       |                 |      |
| UVLO voltage                                                 | V <sub>UVLO</sub>    |                                                        | 3.7                   | 4.0   | 4.3             | V    |
| Hysteresis of UVLO                                           | V <sub>UVLO</sub> H  |                                                        |                       | 0.3   |                 | V    |
| <b>Error amplifier</b>                                       |                      |                                                        |                       |       |                 |      |
| Input bias current                                           | I <sub>EA</sub> IN   |                                                        |                       |       | 100             | nA   |
| Error amplifier gain                                         | G <sub>EA</sub>      |                                                        | 1000                  | 1400  | 1800            | μA/V |
| Range of common-mode input voltage                           | V <sub>EA</sub> R    | V <sub>IN</sub> = 4.5 to 50V                           | 0                     |       | 1.6             | V    |
| Output sink current                                          | I <sub>EA</sub> OSK  | FB = 1.0V                                              |                       | -100  |                 | μA   |
| Output source current                                        | I <sub>EA</sub> OSC  | FB = 0V                                                |                       | 100   |                 | μA   |
| Current detection amplifier gain                             | G <sub>ISNS</sub>    |                                                        |                       | 2.4   |                 |      |
| <b>Over current limiter circuit block</b>                    |                      |                                                        |                       |       |                 |      |
| Reference current                                            | I <sub>LIM</sub>     |                                                        | -10%                  | 20    | +10%            | μA   |
| Over current detection comparator offset voltage             | V <sub>LIM</sub> OFS |                                                        | -5                    |       | +5              | mV   |
| Range of over current detection comparator common mode input | V <sub>LIM</sub> CM  |                                                        | V <sub>IN</sub> -0.45 |       | V <sub>IN</sub> | V    |
| <b>PWM comparator</b>                                        |                      |                                                        |                       |       |                 |      |
| Input threshold voltage                                      | V <sub>t</sub> max   | Duty cycle = D <sub>MAX</sub> , SW = V <sub>IN</sub>   | 1.15                  | 1.25  | 1.35            | V    |
|                                                              | V <sub>t0</sub>      | Duty cycle = 0%, SW = V <sub>IN</sub>                  | 0.5                   | 0.6   | 0.7             | V    |
| Maximum ON duty                                              | D <sub>MAX</sub>     |                                                        | 92                    |       |                 | %    |

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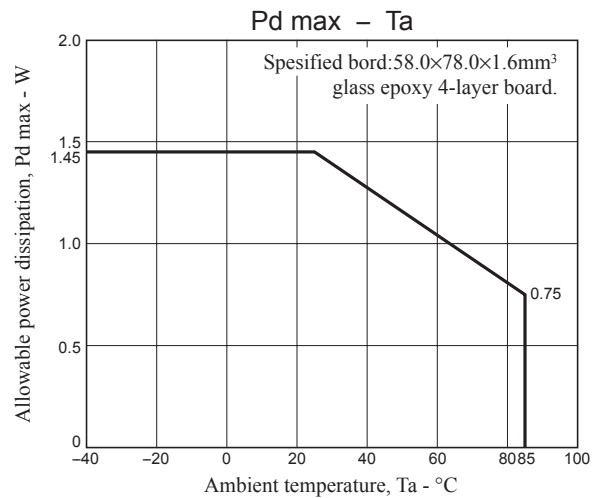
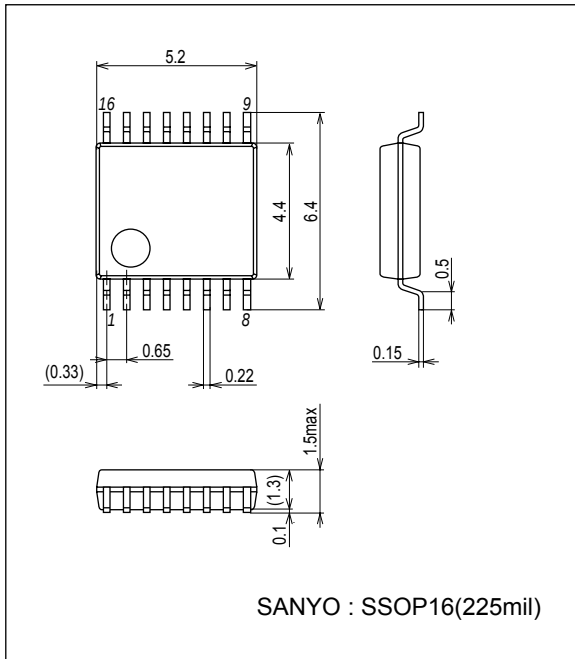
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| Parameter                              | Symbol                | Conditions                     | Ratings |       |     | Unit |
|----------------------------------------|-----------------------|--------------------------------|---------|-------|-----|------|
|                                        |                       |                                | min     | typ   | max |      |
| Power good                             |                       |                                |         |       |     |      |
| Power good “L” sink current            | I <sub>PGL</sub>      | PGOOD = 5V                     |         | 5     |     | mA   |
| Power good “H” sink current            | I <sub>PGH</sub>      | PGOOD = 5V                     |         |       | 1   | μA   |
| Power good voltage                     | P <sub>G</sub> thresh | When FB voltage rises          |         | 0.612 |     | V    |
| Hysteresis of power good               | P <sub>G</sub> hys    |                                |         | 12    |     | mV   |
| Output block                           |                       |                                |         |       |     |      |
| High side output ON resistance (upper) | R <sub>ONH_HIGH</sub> | CBOOT – HDRV = -0.1V           |         | 12    |     | Ω    |
| High side output ON resistance (lower) | R <sub>ONL_HIGH</sub> | HDRV – SW = +0.1V              |         | 3.3   |     | Ω    |
| Low side output ON resistance (upper)  | R <sub>ONH_LOW</sub>  | V <sub>DD</sub> – LDRV = -0.1V |         | 7.9   |     | Ω    |
| Low side output ON resistance (lower)  | R <sub>ONL_LOW</sub>  | LDRV – GND = +0.1V             |         | 3.8   |     | Ω    |
| High side output ON current (upper)    | I <sub>ONH_HIGH</sub> | CBOOT – HDRV = -4.5V           | 160     |       |     | mA   |
| High side output ON current (lower)    | I <sub>ONL_HIGH</sub> | HDRV – SW = +4.5V              | 330     |       |     | mA   |
| Low side output ON current (upper)     | I <sub>ONH_LOW</sub>  | V <sub>DD</sub> – LDRV = -5.2V | 190     |       |     | mA   |
| Low side output ON current (lower)     | I <sub>ONL_LOW</sub>  | LDRV – GND = +5.2V             | 250     |       |     | mA   |
| Entire device                          |                       |                                |         |       |     |      |
| Standby current                        | I <sub>CCS</sub>      | EN < 1V                        |         |       | 1   | μA   |
| Average current consumption            | I <sub>CCA</sub>      | EN > 3.0V                      |         | 2.5   |     | mA   |

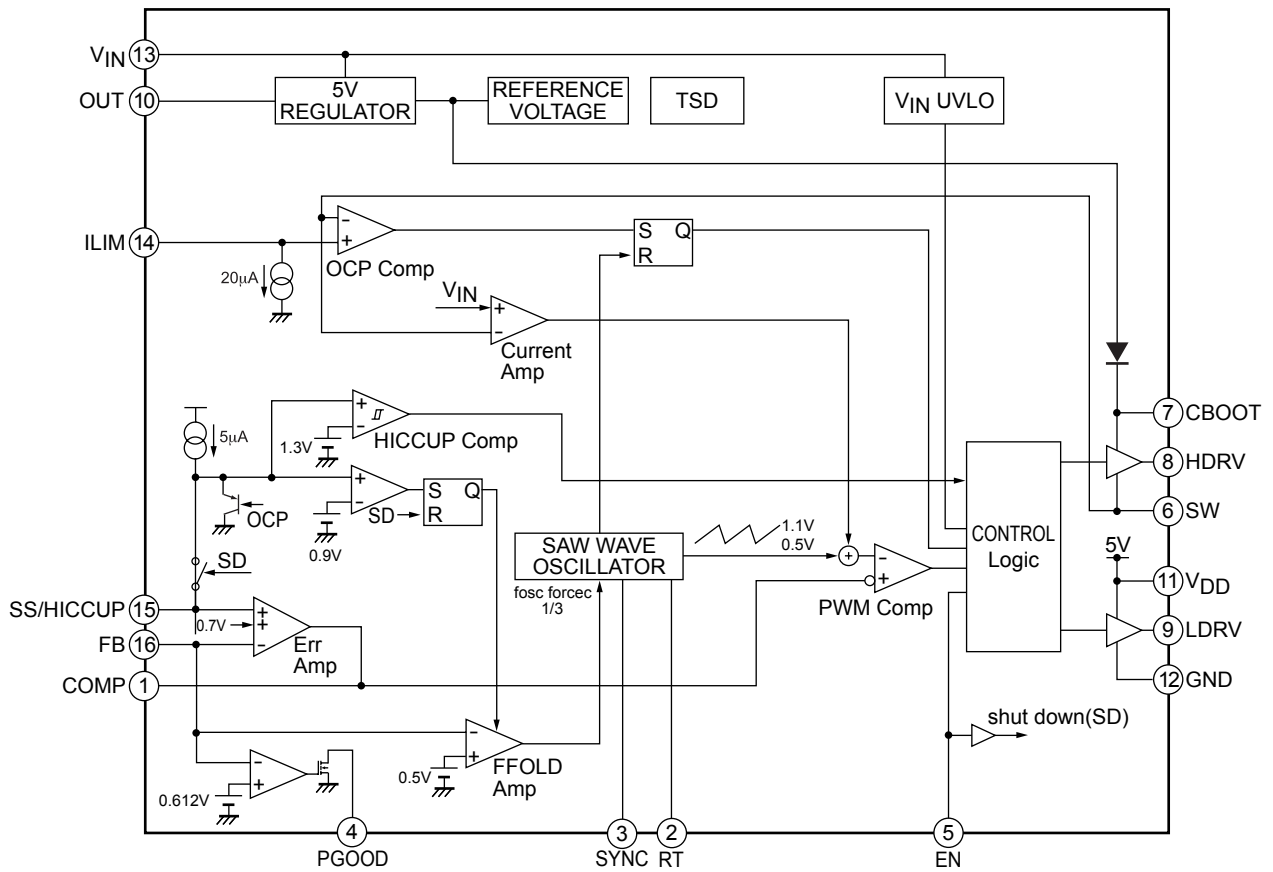
## Package Dimensions

unit : mm (typ)

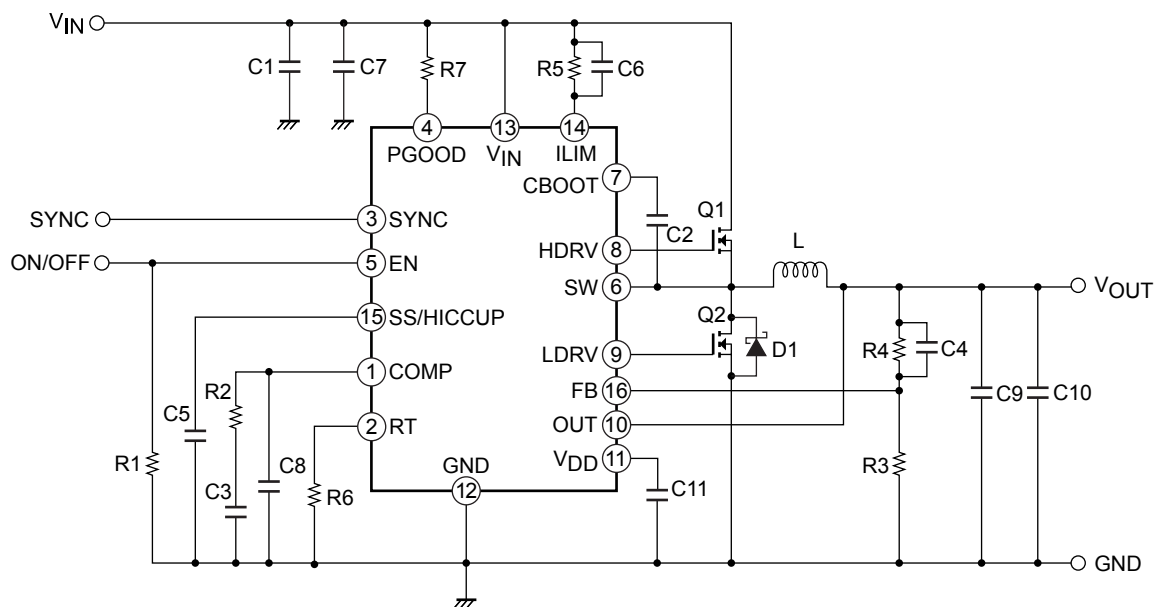
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## Block Diagram

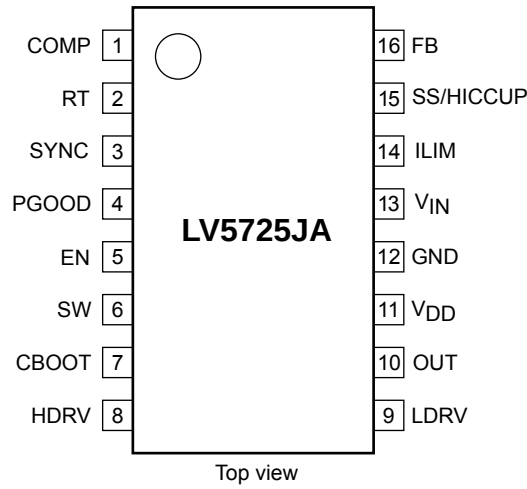


## Sample application circuit



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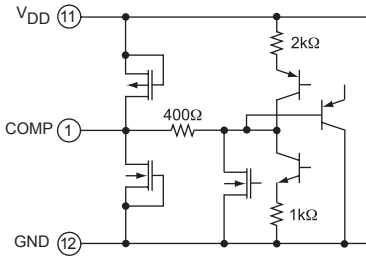
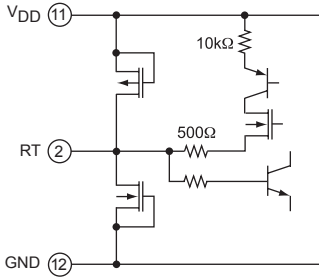
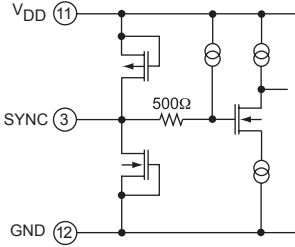
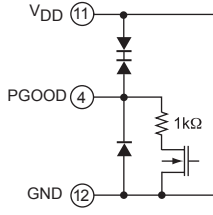
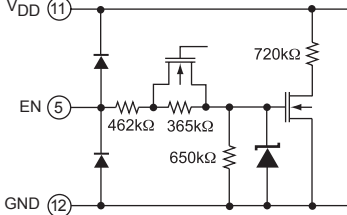
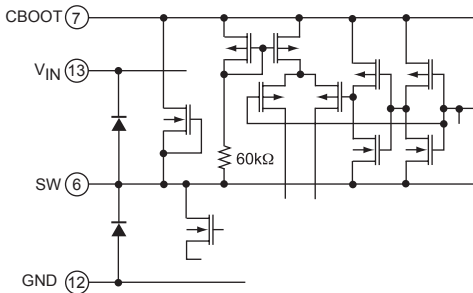
## Pin Assignment



## Pin Function

| Pin No. | Pin name        | Description                                                                                                                                                                                                                                                                                                                                                                  |
|---------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | COMP            | Error amplifier output pin. Make sure to connect a phase compensation network between COMP and GND.                                                                                                                                                                                                                                                                          |
| 2       | RT              | Oscillating frequency setting pin. Make sure to connect a resistor between this pin and GND.                                                                                                                                                                                                                                                                                 |
| 3       | SYNC            | External synchronous signal input pin.                                                                                                                                                                                                                                                                                                                                       |
| 4       | PGOOD           | Power good pin.                                                                                                                                                                                                                                                                                                                                                              |
| 5       | EN              | ON/OFF pin.                                                                                                                                                                                                                                                                                                                                                                  |
| 6       | SW              | This pin is connected to switching node. Connect the source of Nch MOSFET to this pin.                                                                                                                                                                                                                                                                                       |
| 7       | CBOOT           | Bootstrap capacitor connected pin. This pin is used as gate driving power supply for external Nch MOSFET. Make sure to connect a capacitor between CBOOT and SW.                                                                                                                                                                                                             |
| 8       | HDRV            | External upper MOSFET gate driving pin.                                                                                                                                                                                                                                                                                                                                      |
| 9       | LDRV            | External lower MOSFET gate driving pin.                                                                                                                                                                                                                                                                                                                                      |
| 10      | OUT             | Internal regulator power supply pin. This pin is connected to V <sub>OUT</sub> .                                                                                                                                                                                                                                                                                             |
| 11      | V <sub>DD</sub> | Power supply pin for gate drive of the external lower MOS-FET.                                                                                                                                                                                                                                                                                                               |
| 12      | GND             | Ground pin. GND pin voltage is the reference for each reference voltage.                                                                                                                                                                                                                                                                                                     |
| 13      | V <sub>IN</sub> | Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes higher than 4.3V by UVLO function, the IC starts up and mode shifts to soft start operation.                                                                                                                                                                                  |
| 14      | ILIM            | Reference current pin for current detection. The inlet current of approx. 20μA flows into this pin. Connect a resistor externally between this pin and V <sub>IN</sub> and when the voltage supplied to SW pin is lower than the pin voltage of this resistor, the upper Nch MOSFET is turned off by current limiter comparator. This operation is reset at every PWM pulse. |
| 15      | SS/HICCUP       | Capacitor connection pin for soft start. This pin enables to charge the soft start capacitor by 5μA. (approx) When this pin turns approx. 0.9V, soft start period ends and frequency fold back function is activated.                                                                                                                                                        |
| 16      | FB              | Error amplifier reverse input pin. Converter operates to set this pin to 0.708V. The output voltage divided by the external resistance is applied to this pin. After soft start, frequency fold back function operates when the voltage of this pin becomes 0.5V or lower. And oscillating frequency decreases together with FB voltage.                                     |

I/O pin equivalent circuit chart

| Pin No. | Pin No. | Equivalent Circuit                                                                   |
|---------|---------|--------------------------------------------------------------------------------------|
| 1       | COMP    |    |
| 2       | RT      |    |
| 3       | SYNC    |   |
| 4       | PGOOD   |  |
| 5       | EN      |  |
| 6       | SW      |  |

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| Pin No. | Pin No.  | Equivalent Circuit |
|---------|----------|--------------------|
| 7       | CBOOT    |                    |
| 8       | LDRV     |                    |
| 9       | HDRV     |                    |
| 10      | OUT      |                    |
| 11      | VDD      |                    |
| 12, 13  | GND, VIN |                    |
| 14      | ILIM     |                    |

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| Pin No. | Pin No.   | Equivalent Circuit |
|---------|-----------|--------------------|
| 15      | SS/HICCUP |                    |
| 16      | FB        |                    |

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