Ordering number : ENA2157

# LV8133JA

ON Semiconductor®

http://onsemi.com

**Bi-CMOS IC**

## For Brushless Motor Drive

## Sine wave PWM Drive, Pre driver IC

### Overview

The LV8133JA is a PWM system pre driver IC designed for three-phase brushless motors.
This IC reduces motor driving noise by using a high-efficiency, quiet PWM drive (150-degree drive system).
It incorporates a full complement of protection circuits, and is capable of reducing the number of components used and achieving a high level of reliability. This IC is ideally suited for driving various large-sized motors such as those used in ventilators, air purifiers and other such products.

### Features

- Three-phase bipolar drive
- Quiet PWM drive (150-degree current-carrying)
- Drive phase setting function (set in 16 steps from 0 to 28 degrees)
- Supports motor stop mode (when the SS pin is set to the low level, the motor stop mode is turned on, HB pin turned off)
- Supports bootstrap (maximum duty ratio is limited)
- Automatic recovery type constraint protection circuit (constraint protection detection signal output LDA pin provided)
- Forward/reverse switching circuit, Hall bias pin
- Current limiter circuit, low-voltage protection circuit, and thermal shutdown protection circuit
- FG1 output (360-degree electrical angle/1 pulse)

# Specifications

## Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ max | $V_{CC}$ pin | 18 | V |
| Output current | $I_O$ max | | 15 | mA |
| Allowable power dissipation | Pd max1 | Independent IC | 0.35 | W |
| | Pd max2 | Mounted on a specified circuit board.* | 0.95 | W |
| FG pin applied voltage | $V_{FG}$ max | | 18 | V |
| LDA pin applied voltage | $V_{LDA}$ max | | 18 | V |
| Junction temperature | Tj max | | 150 | °C |
| Operating temperature | Topr | | -40 to +105 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Specified circuit board : 114.3mm × 76.1mm × 1.6mm, glass epoxy

Note 1) Absolute maximum ratings represent the values that cannot be exceeded for any length of time.

Note 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Allowable Operating range at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 8.5 to 16.5 | V |
| 5V constant voltage output current | $I_{REG}$ | | 0 to -10 | mA |
| HB pin output current | $I_{HB}$ | | 0 to -30 | mA |
| CTL pin applied voltage | $V_{CTL}$ | | 0 to VREG | V |
| FG pin applied voltage | $V_{FG}$ | | 0 to $V_{CC}$ | V |
| FG pin output current | $I_{FG}$ | | 0 to 10 | mA |
| LDA pin applied voltage | $V_{LDA}$ | | 0 to $V_{CC}$ | V |
| LDA pin output current | $I_{LDA}$ | | 0 to 10 | mA |

## Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 15V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply current | $I_{CC}$ | | | 4.5 | 7.0 | mA |
| **Output Block** (Pin HIN1, HIN2, HIN3, LIN1, LIN2 and LIN3) | | | | | | |
| High level output voltage | $V_{HO}$ | $I_O$ = -10mA | VREG-0.40 | VREG-0.25 | | V |
| Upper output ON resistance | $R_{ON}$ (H1) | $I_O$ = -10mA | | 25 | 40 | Ω |
| Low level output voltage | $V_{LO}$ | $I_O$ = 10mA | | 0.15 | 0.30 | V |
| Lower output ON resistance | $R_{ON}$ (L1) | $I_O$ = 10mA | | 15 | 30 | Ω |
| Output leakage current | $I_O$leak | | | | 10 | μA |
| Maximum duty ratio limit OFF time | Toff | VCTL = 5V | 5 | 7 | 9 | μs |
| **5V Constant Voltage Output** (VREG5 pin) | | | | | | |
| Output voltage | VREG | $I_O$ = -5mA | 4.7 | 5.0 | 5.3 | V |
| Voltage fluctuation | ΔV (REG1) | $V_{CC}$ = 9.5 to 16.5V, $I_O$ = -5mA | | | 100 | mV |
| Load fluctuation | ΔV (REG2) | $I_O$ = -5 to -10mA | | | 100 | mV |
| **Hall Amplifier** (Pin $IN1^+$, $IN1^-$, $IN2^+$, $IN2^-$, $IN3^+$ and $IN3^-$) | | | | | | |
| Input bias current | IB (HA) | | -2 | | 0 | μA |
| Common-mode input voltage range 1 | VICM1 | When a Hall element is used | 0.3 | | VREG-1.7 | V |
| Common-mode input voltage range 2 | VICM2 | Single-sided input bias mode (when a Hall IC is used) | 0 | | VREG | V |
| Hall input sensitivity | VHIN | Sine wave | 120 | | | mVp-p |
| Hysteresis width | $\Delta V_{IN}$ (HA) | | ±10 | ±25 | ±40 | mV |
| Input voltage Low → High | VSLH | | -5 | 0 | +5 | mV |
| Input voltage High → Low | VSHL | | -5 | 0 | +5 | mV |

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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **CSD Oscillator Circuit** | | | | | | |
| High level output voltage | $V_{OH}$ (CSD) | | 2.75 | 2.95 | 3.15 | V |
| Low level output voltage | $V_{OL}$ (CSD) | | 0.85 | 1.05 | 1.25 | V |
| Amplitude | V (CSD) | | 1.7 | 1.9 | 2.1 | Vp-p |
| External capacitor charging current | ICHG1 (CSD) | VCHG1 = 2.0V | -14 | -10 | -6 | μA |
| External capacitor discharging current | ICHG2 (CSD) | VCHG2 = 2.0V | 6 | 10 | 14 | μA |
| **PWM Oscillator** (CPWM pin) | | | | | | |
| High level output voltage | $V_{OH}$ (PWM) | | 3.3 | 3.5 | 3.7 | V |
| Low level output voltage | $V_{OL}$ (PWM) | | 1.35 | 1.5 | 1.65 | V |
| Amplitude | V (PWM) | | 1.8 | 2.0 | 2.2 | Vp-p |
| Oscillation frequency | f (PWM) | C = 2200pF, R = 15kΩ (design target value) | | 17.3 | | kHz |
| **Current Limiter Operation** (RF pin) | | | | | | |
| Limiter voltage | VRF | | 0.225 | 0.25 | 0.275 | V |
| **Thermal Shutdown Protection Operation** | | | | | | |
| Thermal shutdown protection operating temperature | TSD | * Design target value (junction temperature) | 150 | 175 | | °C |
| Hysteresis width | ΔTSD | * Design target value (junction temperature) | | 35 | | °C |
| **HB pin** | | | | | | |
| High output voltage | $V_{HO}$ (HB) | IHB = -10mA | $V_{CC}$-0.2 | $V_{CC}$-0.1 | | V |
| Output ON resistance | $R_{ON}$ (HB) | IHB = -10mA | | 10 | 20 | Ω |
| Output leakage current | $I_L$ (HB) | Stop mode $V_{CC}$ = 15V | | | 10 | μA |
| **Low Voltage Protection Circuit** (detecting VREG5 voltage) | | | | | | |
| Operation voltage (VREG5 voltage) | VSD | | 3.1 | 3.6 | 4.1 | V |
| Hysteresis width | ΔVSD | | 0.2 | 0.4 | 0.6 | V |
| **FG1 LDA Pin** | | | | | | |
| Output ON resistance | $R_{ON}$L (FG)<br>$R_{ON}$L (LDA) | IFG/ILDA = 5mA | | 40 | 60 | Ω |
| Output leakage current | $I_L$ (FG)<br>$I_L$ (LDA) | VFG/VLDA = 18V | | | 10 | μA |
| **CTL Amplifier** (drive mode) | | | | | | |
| Input voltage range | $V_{IN}$ (CTL) | | 0 | | VREG | V |
| High level input voltage | $V_{IH}$ (CTL) | Amplitude modulated signal 100% | 3.3 | 3.5 | 3.7 | V |
| Middle level input voltage | $V_{IM}$ (CTLI) | Amplitude modulated signal 0% | 1.35 | 1.5 | 1.65 | V |
| **F/R Pin** | | | | | | |
| High level input voltage range | $V_{IH}$ (FR) | | 2.5 | | VREG | V |
| Low level input voltage range | $V_{IL}$ (FR) | | 0 | | 0.7 | V |
| Input open voltage | $V_{IO}$ (FR) | | | 0 | 0.3 | V |
| Hysteresis width | $V_{IS}$ (FR) | | 0.15 | 0.30 | 0.45 | V |
| High level input current | $I_{IH}$ (FR) | VF/R = VREG | 25 | 45 | 65 | μA |
| Low level input current | $I_{IL}$ (FR) | VF/R = 0V | -2 | 0 | +2 | μA |
| **SS Pin** | | | | | | |
| Drive start voltage | VON | | 2.9 | | VREG | V |
| Drive stop voltage | VOFF | | 0 | | 0.8 | V |
| **ADP1 Pin** (drive phase adjustment) | | | | | | |
| Minimum lead angle | Vadp01 | VADP1 = 0V | | 0 | 2 | Deg |
| Maximum lead angle | Vadp16 | VADP1 = VREG | 26 | 28 | | Deg |
| Current ratio with the ADP1/ADP2 pin current | IADPR | VCTL = 2.5V, IADP1/IADP2 | 1.8 | 2 | 2.2 | A/A |

* These are design target values and no measurements are made.

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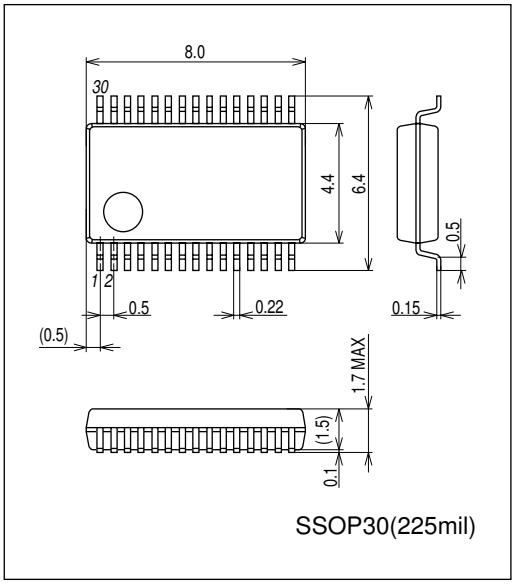
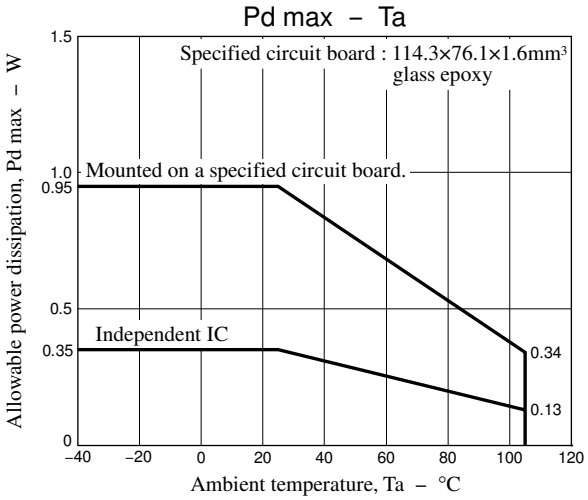
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **ADP2 Pin** (drive phase adjustment) | | | | | | |
| High level output voltage | VADP2H | VCTL = VREG | (VREG/2) -0.2 | (VREG/2) | (VREG/2) +0.2 | V |
| Low level output voltage | VADP2L | VCTL = 0V | 0 | | 0.3 | V |
| **DPL Pin** (drive-phase-adjustment limit setting pin) | | | | | | |
| Lead angle limit high level voltage | VDPLH | | 3.3 | 3.5 | 3.7 | V |
| Lead angle limit low level voltage | VDPLL | | 1.35 | 1.5 | 1.65 | V |

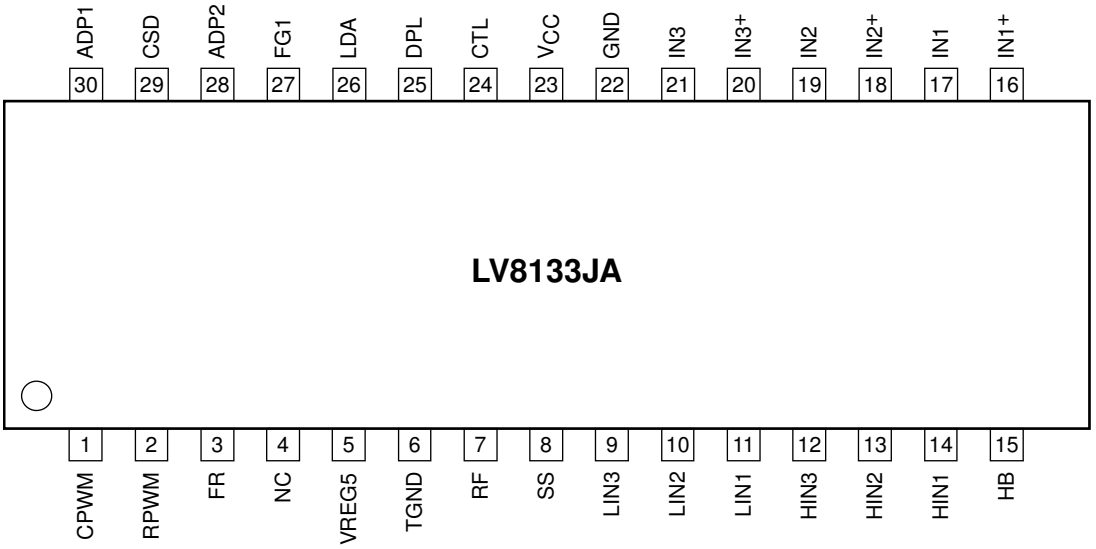
## Package Dimensions

nit : mm (typ)
3421



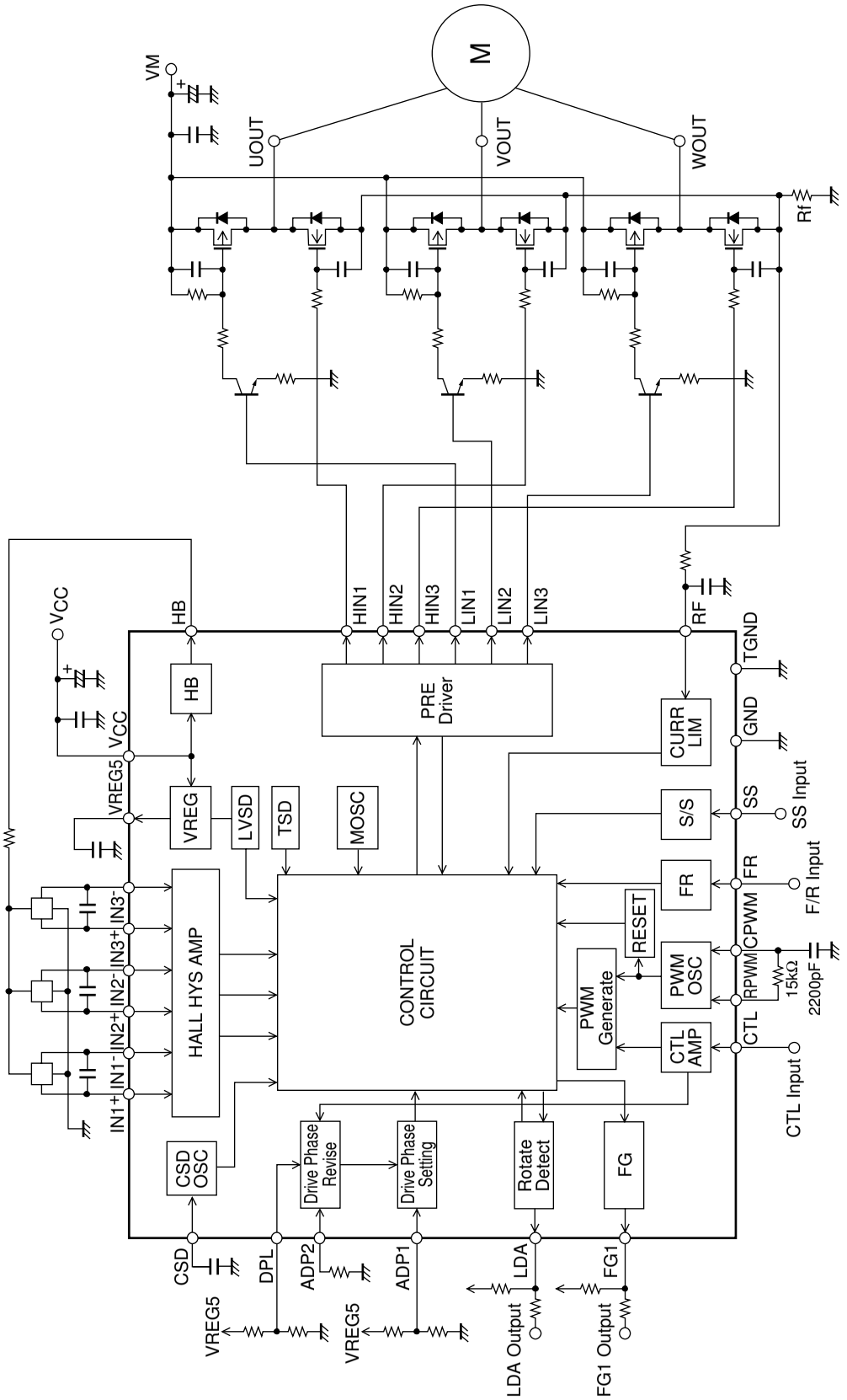




## Pin Assignment

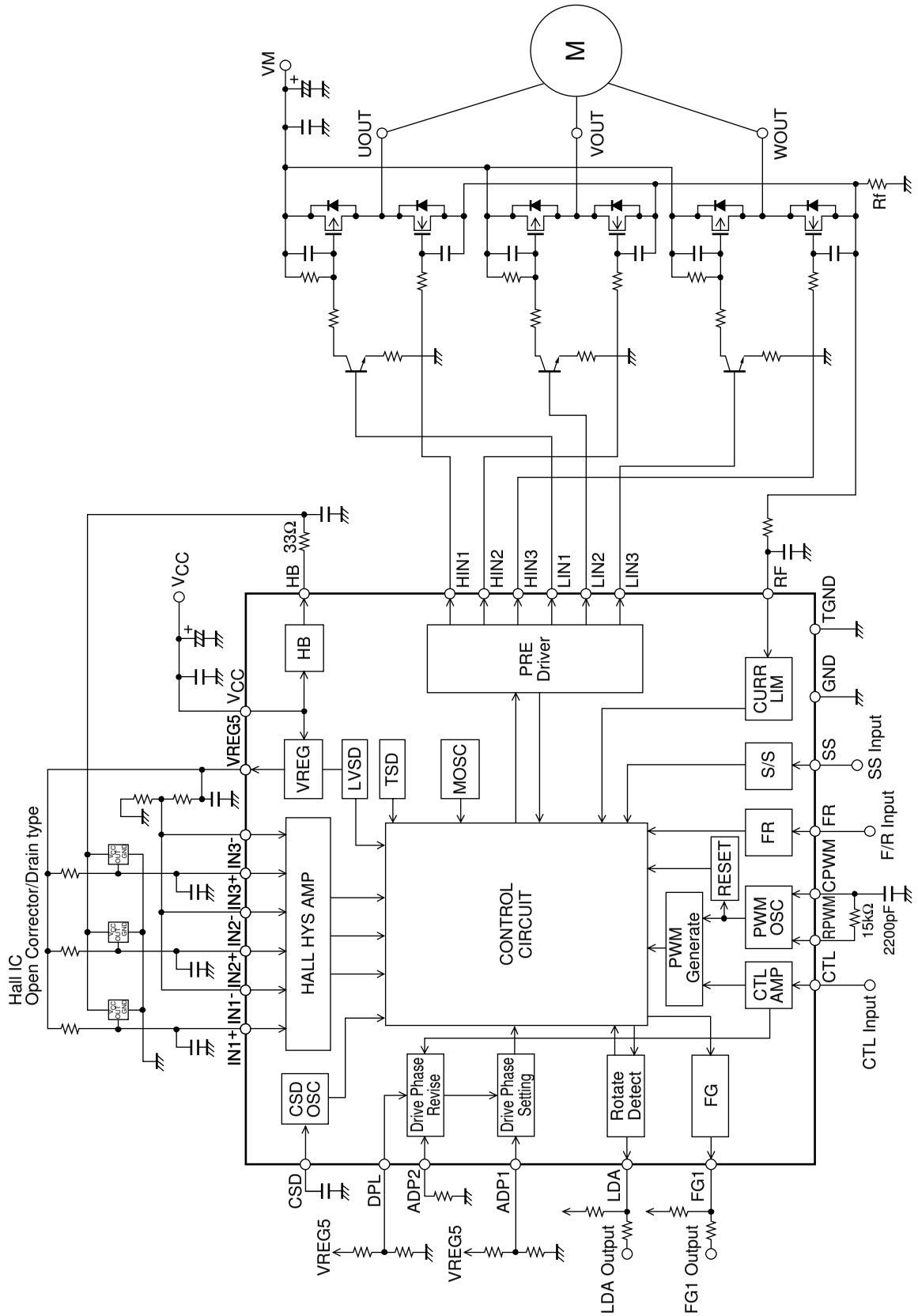



Top view

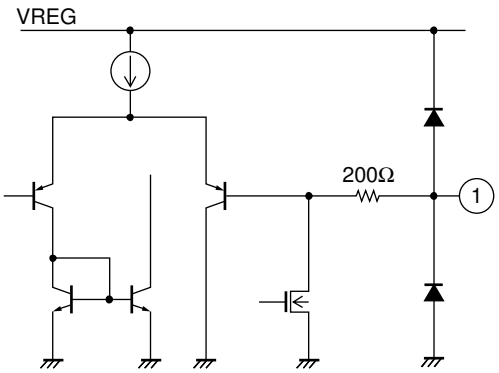
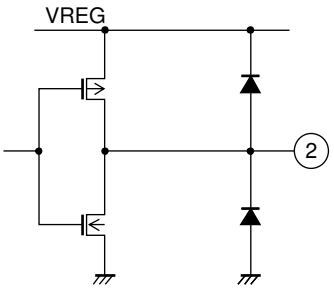
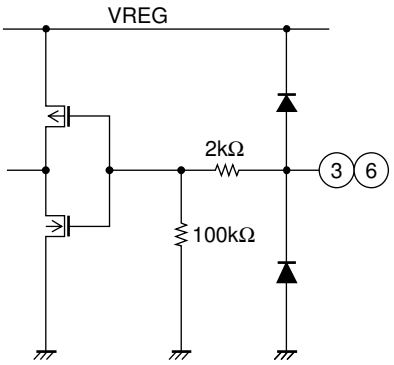
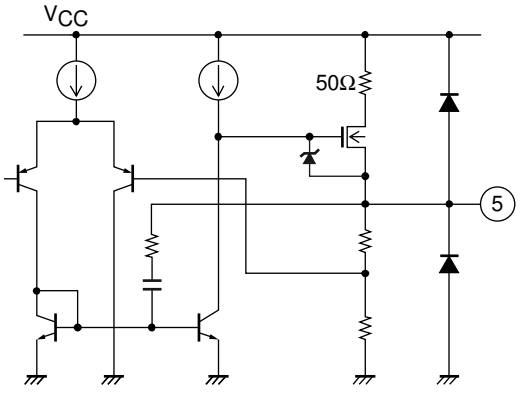
## Sample Application Circuit 1
## (Hall element)



## Sample Application Circuit 2
## (Hall IC)



## Pin Functions

| Pin No. | Pin Name | Pin function | Equivalent Circuit |
|---|---|---|---|
| 1 | CPWM | Triangle wave oscillation pin for PWM generation.<br>Insert a capacitor between this pin and ground and a resistor between this pin and RPWM for triangle wave oscillation. |  |
| 2 | RPWM | Oscillation pin for PWM generation.<br>Insert a resistor between this pin and CPWM. |  |
| 3<br><br><br><br><br>6 | FR<br><br><br><br><br>TGND | FR<br>Forward/reverse rotation setting pin.<br>A low-level specifies forward rotation and a high-level specifies reverse rotation. This pin is held low when open.<br><br>TGND<br>Test pin. Connect this pin to ground. |  |
| 4 | NC | | |
| 5 | VREG5 | 5V regulator output pin<br>(control circuit power supply).<br>Insert a capacitor between this pin and ground for power stabilization.<br>0.1μF or so is desirable. |  |

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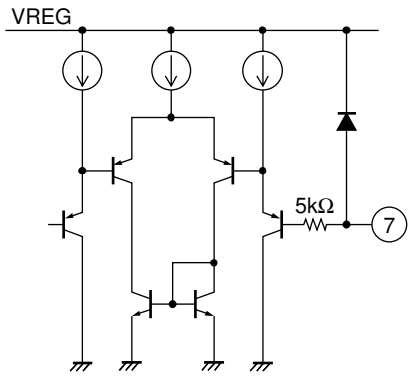
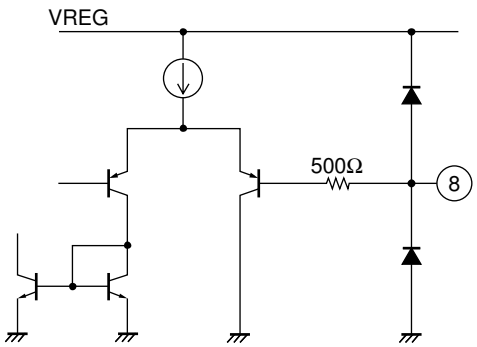
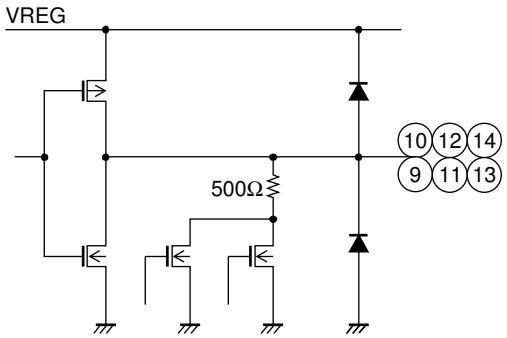
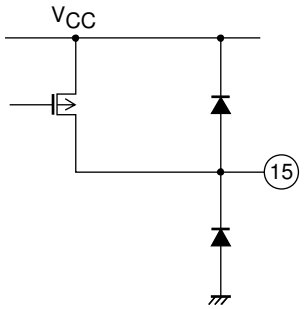
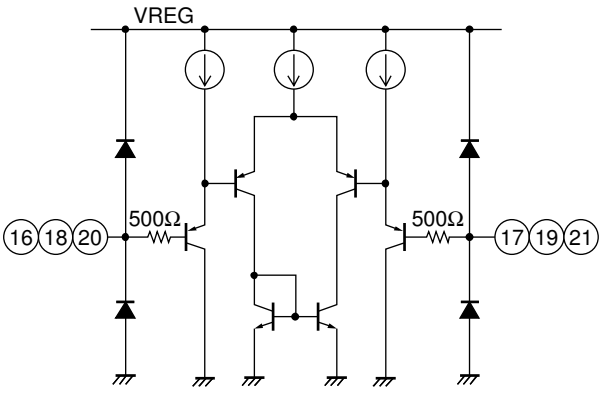
| Pin No. | Pin Name | Pin function | Equivalent Circuit |
|---|---|---|---|
| 7 | RF | Output current detection pin.<br>This pin is used to detect the voltage across the current detection resistor (Rf).<br>The maximum output current is determined by the equation $I_{OUT}$ = 0.25V/Rf. |  |
| 8 | SS | Start/stop pin.<br>When the SS pin is set to the high level, S/S switching circuit enters the start mode. Inversely, when the SS pin is set to the low level, S/S switching circuit enters the stop mode. In the stop mode, the drive output and HB pin are OFF, and the FG signal is output.<br>This pin cannot be used in the open state. |  |
| 9<br>10<br>11<br><br><br>12<br>13<br>14 | LIN3<br>LIN2<br>LIN1<br><br><br>HIN3<br>HIN2<br>HIN1 | LIN1, LIN2, and LIN3 :<br>L-side output pins.<br>Generate 0 to VREG5 push-pull outputs.<br><br>HIN1, HIN2, and HIN3 :<br>H-side output pins.<br>Generate 0 to VREG5 push-pull outputs. |  |
| 15 | HB | Hall bias power supply pin.<br>This pin is set to the high impedance state when in the stop mode. By supplying the Hall bias power from this pin, the power that is consumed by the Hall bias in the stop mode can be reduced to zero. |  |
| 16<br>17<br>18<br>19<br>20<br>21 | $IN1^+$<br>$IN1^-$<br>$IN2^+$<br>$IN2^-$<br>$IN3^+$<br>$IN3^-$ | Hall signal input pins.<br>The high state is when $IN^+$ is greater than $IN^-$, and the low state is the reverse.<br>An amplitude of at least 120mVp-p (differential) is desirable for the Hall signal inputs. If noise on the Hall signals is a problem, insert capacitors between $IN^+$ and $IN^-$ pins.<br>If input is provided from a Hall IC, the common-mode input range can be expanded by biasing either + or -. |  |

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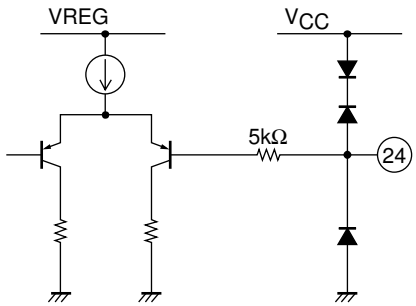
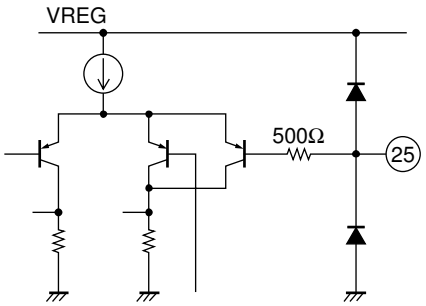
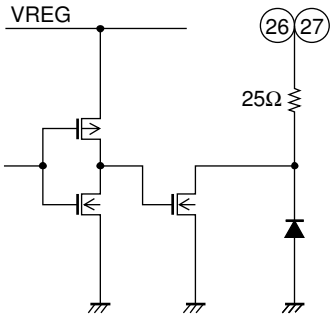
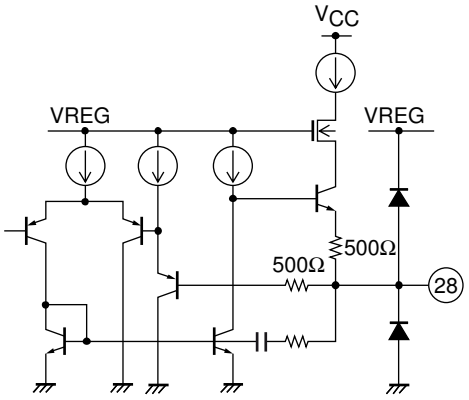
| Pin No. | Pin Name | Pin function | Equivalent Circuit |
|---|---|---|---|
| 22 | GND | Ground pin of the control circuit block. | |
| 23 | $V_{CC}$ | Power supply pin for control.<br>Insert a capacitor between this pin and ground to prevent the influence of noise, etc. | |
| 24 | CTL | Control input pin. When CTL pin voltage rises, the IC changes the output signal PWM duty to increase the torque output. |  |
| 25 | DPL | Setting pin for drive phase adjustment limit.<br>This pin is used to limit the lead angle of the drive phase. The lead angle is limited to zero degrees when the voltage is 1.5V or lower and the limit is released when the voltage is 3.5V or higher. |  |
| 26<br>27 | LDA<br>FG1 | LDA : Constraint protection detection output pin.<br>A low level is output during normal rotation and a high level is output in the constraint protection state.<br><br>FG1 :1-Hall FG signal output pin.<br>8-pole motor outputs 4 pulses per one rotation. |  |
| 28 | ADP2 | Setting pin for phase drive correction.<br>This pin sets the amount of correction made to the lead angle according to the CTL input. Insert a resistor between this pin and ground to adjust the amount of correction. |  |

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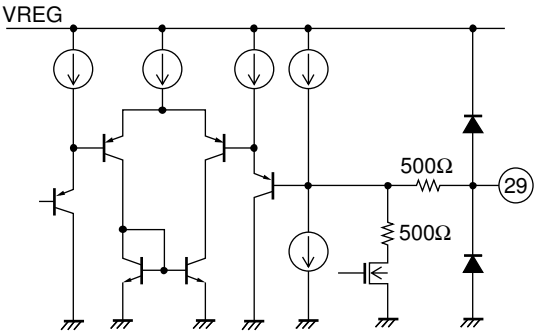
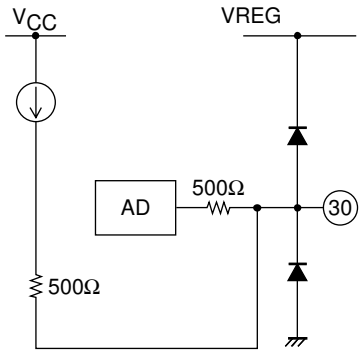
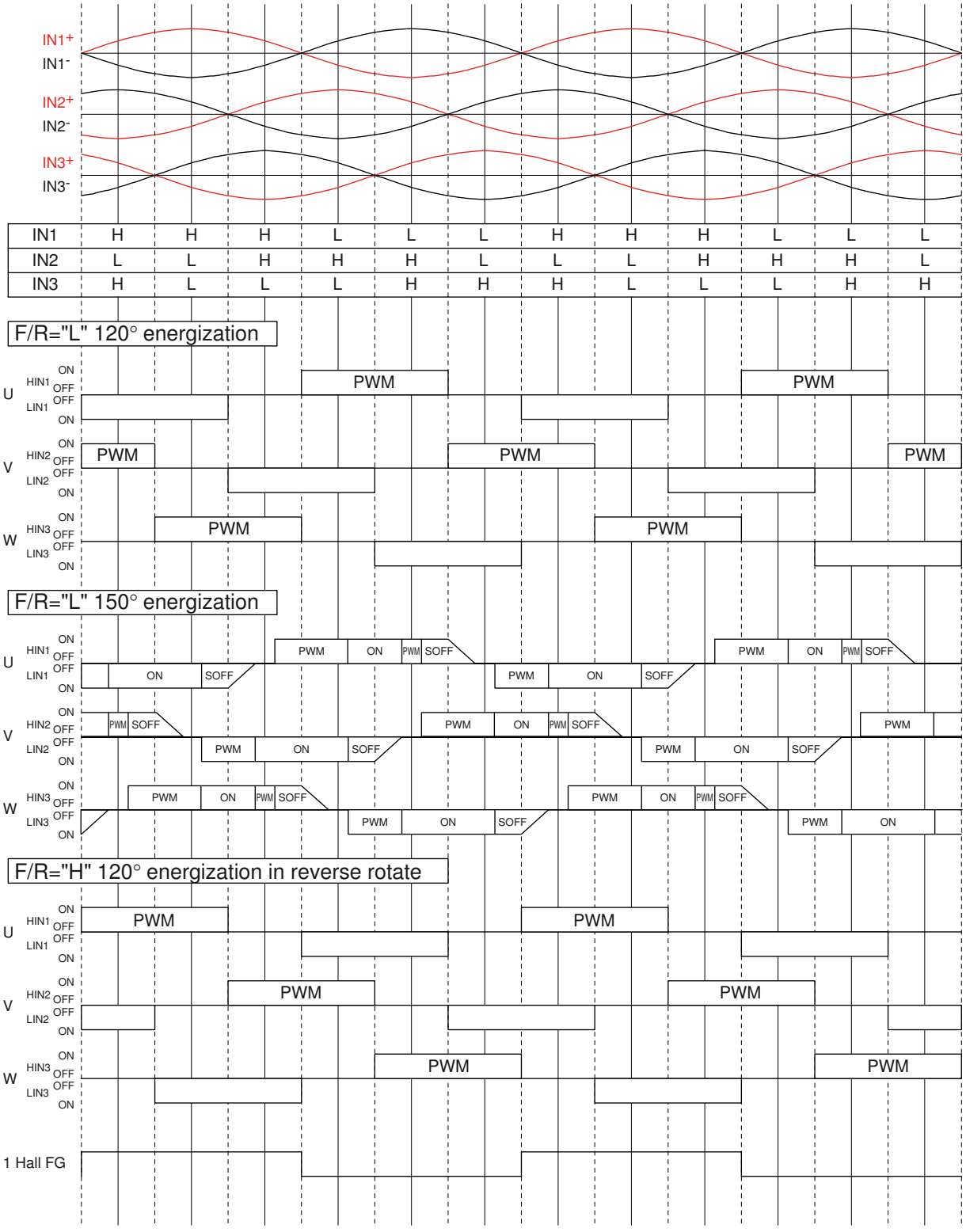
| Pin No. | Pin Name | Pin function | Equivalent Circuit |
|---|---|---|---|
| 29 | CSD | Pin to set the operating time of the motor constraint protection circuit.<br>Insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used. |  |
| 30 | ADP1 | Drive phase adjustment pin.<br>The drive phase can be advanced from 0 to 28 degrees during 150-degree current carrying drive. The lead angle becomes 0 degrees when 0V is input and 28 degrees when VREG is input. |  |

**Timing Chart** (IN = “H”indicates the state in which IN+ is greater than IN-.)

(1) F/R pin = L

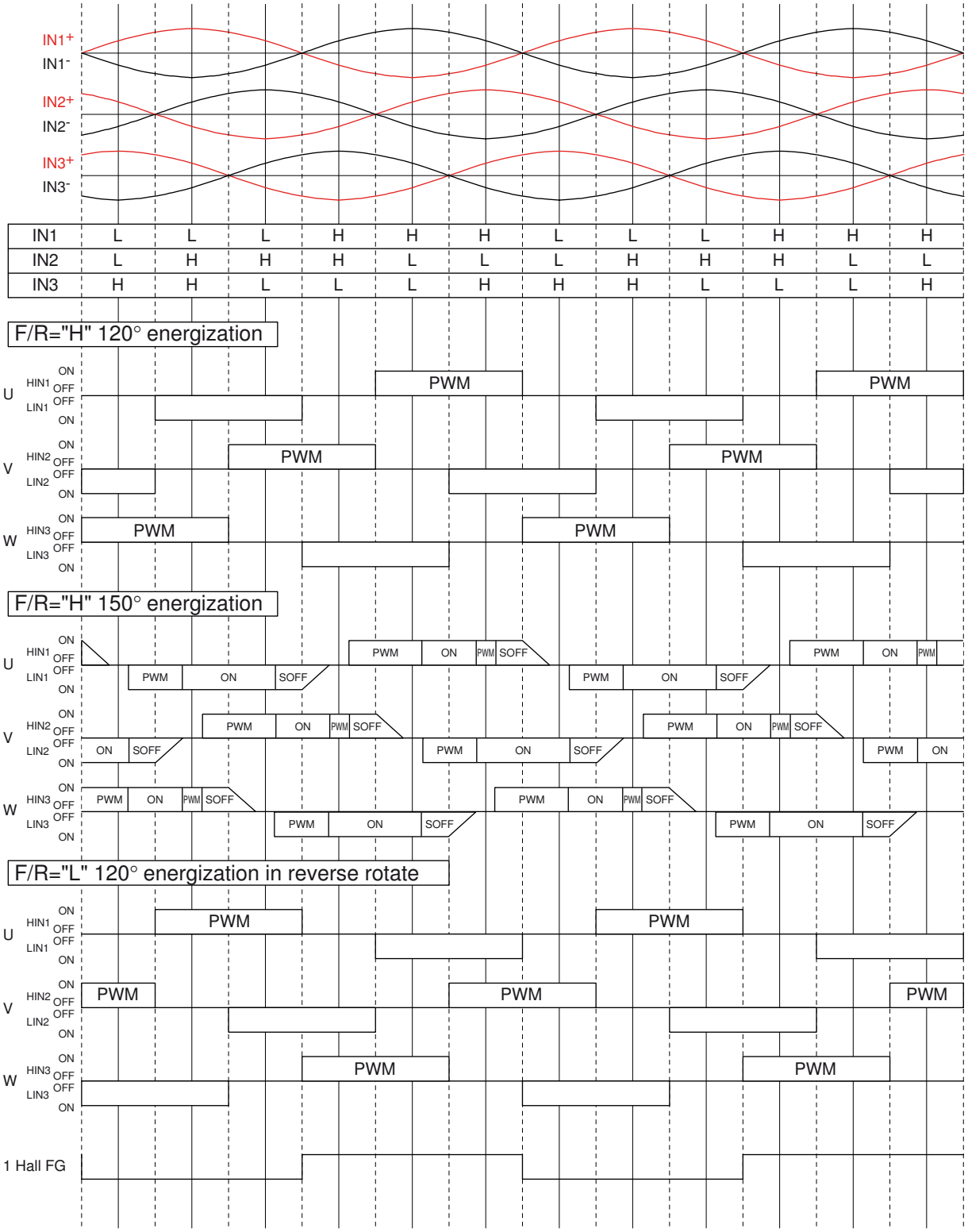



The energization is switched to 120° wher 1 Hall FG frequency is 3.6Hz (typ) or lower

A direction of rotation is detected from Hall signal according to F/R pin input

If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

(2) F/R pin = H




The energization is switched to 120° wher 1 Hall FG frequency is 3.6Hz (typ) or lower
A direction of rotation is detected from Hall signal according to F/R pin input
If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

## Functional Description

• Basic operation of 120-degree ⇔ 150-degree current-carrying switching

At startup, this IC starts at 120-degree current-carrying. The rotation direction is detected using the Hall signal in accordance with the F/R pin input, and if the motor is rotating in the reverse direction with respect to the F/R pin input, the 120-degree current-carrying is forcibly continued. If the motor is rotating in the forward direction with respect to the F/R pin input, the 120-degree current-carrying is switched to 150-degree current-carrying when 1 Hall FG frequency is 3.6Hz (typ) or higher and the rising edge of the IN2 signal has been detected twice in succession.

○ Concerning the Hall signal input sequence

This IC controls the motor rotation direction commands and Hall signal input sequence in order to set the lead angle. If the motor rotation direction commands and Hall signal input sequence do not conform to what is shown on the timing chart, the motor is driven by 120-degree current-carrying.

Sequence 1 : When the Hall signal has been input with the following logic

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IN1 | H | | H | | H | | L | | L | | L |
| IN2 | L | → | L | → | H | → | H | → | H | → | L |
| IN3 | H | | L | | L | | L | | H | | H |

When F/R pin input is high → 120-degree current-carrying
When F/R pin input is low → 150-degree current-carrying

Sequence 2 : When the Hall signal has been input with the following logic

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IN1 | H | | L | | L | | L | | H | | H |
| IN2 | L | → | L | → | H | → | H | → | H | → | L |
| IN3 | H | | H | | H | | L | | L | | L |

When F/R pin input is high → 150-degree current-carrying
When F/R pin input is low → 120-degree current-carrying

• CTL pin input

a) Standby mode $V_{CTL} < V_{IM}$ (1.5V : typ)

When the CTL pin voltage is lower than $V_{IM}$, the IC enters the standby mode. All the $H_{IN}$ and $L_{IN}$ outputs are set to the low level, and the motor prepares to start being driven.

b) Drive mode $V_{IM} \leq V_{CTL} \leq$ VREG

When the CTL pin voltage is $V_{IM} \leq V_{CTL} \leq$ VREG, the IC enters the drive mode, and the motor is driven at the PWM duty ratio corresponding to $V_{CTL}$. When $V_{CTL}$ is increased, the PWM duty ratio increases, and the duty ratio is set internally to 100% at $V_{IH}$ (3.5V: typ), but the output maximum duty ratio is limited to 88%: typ (when the PWM frequency is 17kHz).

• SS pin input

a) Start mode $2.9V < V_{SS} \leq$ VREG

When the SS pin voltage is $2.9V < V_{SS} <$ VREG, the IC enters the start mode, and the motor is driven by 150-degree current-carrying.

b) Stop mode $0V \leq V_{SS} < 0.8V$

When the SS pin voltage is $0V \leq V_{SS} < 0.8V$, the IC enters the stop mode, and the motor stops. In the stop state, the drive output and HB pin are OFF, and the FG signal is output.

c) Test mode $2V < V_{SS} < 2.4V$ (Design target)

When the SS pin voltage is $2V < V_{SS} < 2.4V$, the IC enters the stop mode, and the motor stops. In the stop state, the drive output and HB pin are OFF, and the FG signal is output.

• Bootstrap capacitor initial charging mode

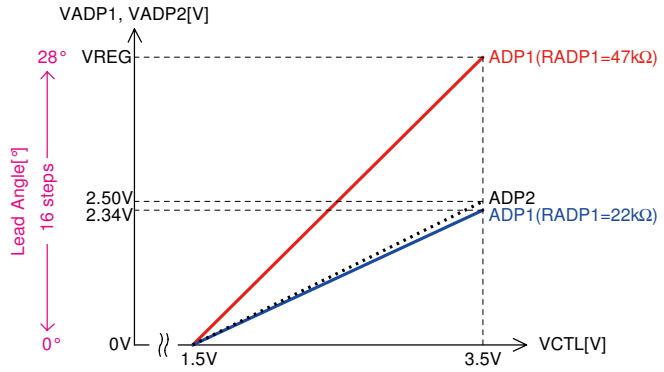
When the mode is changed from stop to start or when the mode is changed from standby to drive, the IC enters the bootstrap capacitor charging mode ($H_{IN}1$, $H_{IN}2$, $H_{IN}3$ = L $L_{IN}1$, $L_{IN}2$, $L_{IN}3$ constitute the output (2.2ms typ) that supports the 120-degree current-carrying mode) in order to charge the bootstrap capacitor.

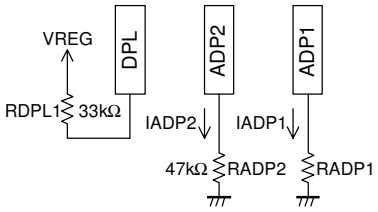
• Drive phase adjustment

During 150-degree current-carrying drive, current-carrying is started from the phase that is 20 degrees ahead of the 120-degree current-carrying. From this state, any lead angle from 0 to 28 degrees can be set using the ADP1 pin voltage (lead angle control). This setting can be adjusted in 16 steps (in 1.875-degree increments) from 0 to 28 degrees using the ADP1 pin voltage, and it is updated every Hall signal cycle (it is sampled at the rising edge of the IN3 input and updated at its falling edge).

A number of lead angle adjustments proportionate to the CTL pin voltage can be undertaken by adjusting the resistance levels of resistors connected to the ADP1 pin, ADP2 pin and DPL pin. When these pins are not going to be used, reference must be made to section 5. 6, and the pins must not be used in the open status. Furthermore, a resistance of 47kΩ or more must be used for the resistor (RADP2) that is connected to the ADP2 pin.

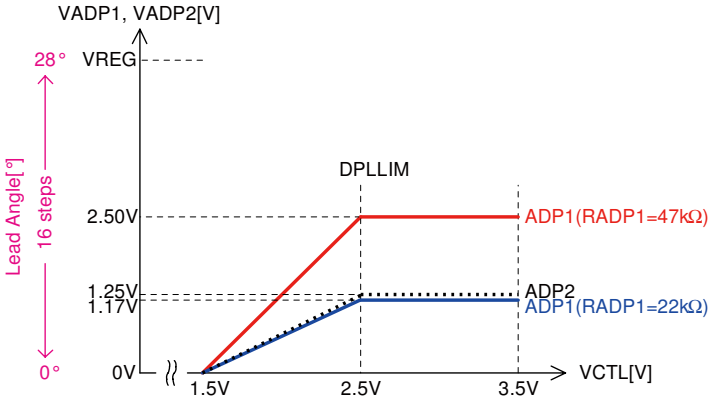
1. The slopes of $V_{CTL}$ and VADP1 can be adjusted by setting the resistance level of the resistor (RADP1) connected to ADP1 (pin 30).

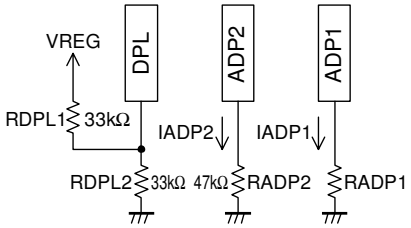



VADP2=(VCTL-1.5)×(2.5/2.0)
IADP2=VADP2/RADP2
IADP1=IADPR×IADP2
VADP1=IADP1×RADP1

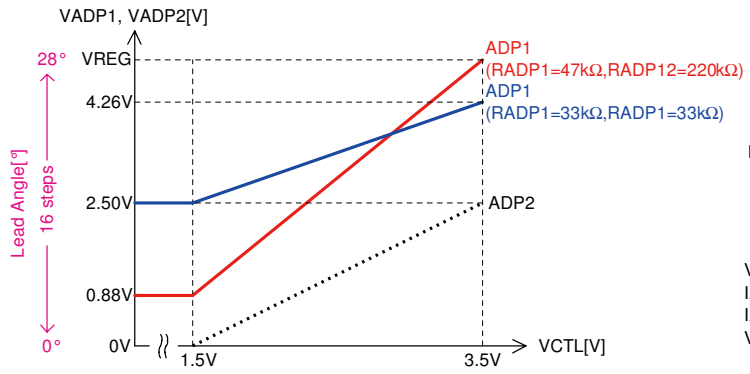
2. The ADP2 pin rise can be halted (a limit on the lead angle adjustment can be set by means of the CTL voltage) by setting DPL (pin 25).

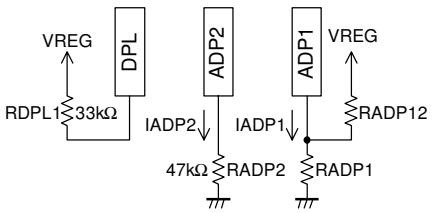



VADP2=(VCTL-1.5)×(2.5/2.0)
IADP2=VADP2/RADP2
IADP1=IADPR×IADP2
VADP1=IADP1×RADP1
DPLLIM=VDPL

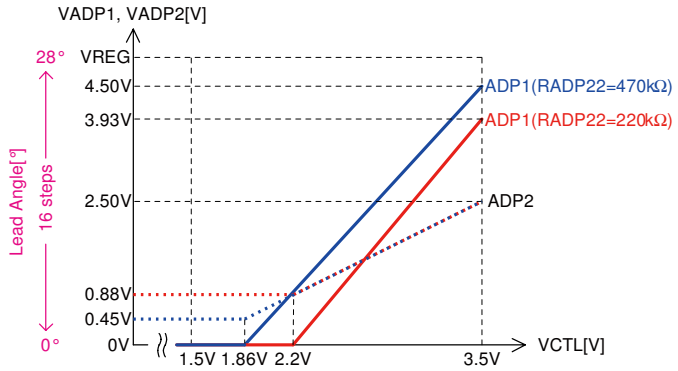
3. The offset and slope can be adjusted as desired by setting RADP1 and RADP12 of ADP1 (pin 30). (It is also possible to set a limit on the lead angle adjustment by means of the CTL voltage by setting DPL.)

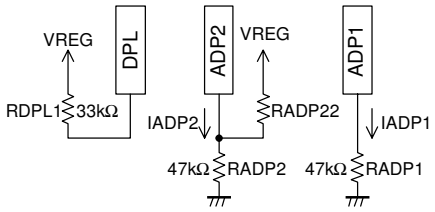



VADP2=(VCTL-1.5)×(2.5/2.0)
IADP2=VADP2/RADP2
IADP1=IADPR×IADP2
VADP1=((RADP1×RADP12)/(RADP1+RADP12))×IADP1
+(RADP1/(RADP1+RADP12))×VREG

4. The rising voltage of ADP1 can be adjusted using the settings of RADP21 and RADP22 of ADP2 (pin 28). However, they must be set in such a way that the ADP2 voltage does not exceed 1V when $V_{CTL}$ is lower than 1.5V.




VADP2=(VCTL-1.5)×(2.5/2.0)
*min: VREG×(RADP2/(RADP2+RADP22))
IADP2=VADP2/RADP2-(VREG-VADP2)/RADP22
*min=0μA
IADP1=IADPR×IADP2
VADP1=IADP1×RADP1

5. When the lead angle is not adjusted
   ADP1 pin: shorted to ground; ADP2 pin and DPL pin: pulled down to ground using the resistors

6. When the lead angle is not adjusted by means of the CTL pin voltage (for use with a fixed lead angle)
   ADP1 pin: lead angle setting by resistance division from VREG; ADP2 pin and DPL pin: pulled down to ground by the resistors

## Description of LV8133

1. Current Limiter Circuit
   The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/Rf$ (where $V_{RF}$ = 0.25V typ, Rf is the value of the current detection resistor). The current limiter operates by reducing the output on duty to suppress the current.
   The current limiter circuit detects the reverse recovery current of the diode due to PWM operation. To assure that the current limiting function does not malfunction, its operation has a delay of approx. 1μs. If the motor coils resistance or a low inductance, current fluctuation at startup (when there is no back electromotive force in the motor) will be rapid. The delay in this circuit means that at such times the current limiter circuit may operate at a point well above the set current. Application must take this increase in the current due to the delay into account when the current limiter value is set.

2. Motor Stop (SS pin)
   With the motor stop operation using the SS pin, the current consumption can be reduced by setting the drive output and HB pin to OFF.
   Furthermore, since the VREG5 voltage and FG1 signal can be output, the motor rotation information can be output even in the motor stop mode by supplying the Hall bias from VREG5.

3. Hall Input Signal
   Signals with an amplitude in excess of the hysteresis (40mV max) is required for the Hall inputs. However, considering the influence of noise and phase displacement, an amplitude of over 120mV is desirable.
   If noise disrupts the output waveform (at phase change), this must be prevented by inserting capacitors or other devices across the Hall inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required.
   If all three phases of the Hall input signal go to the same input state (HHH or LLL), the $H_{IN}/L_{IN}$ outputs are all set to the low state.
   If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or –side) at a voltage within the common-mode input voltage range (0.3V to VREG-1.7V) allows the other input side to be used as an input over the 0V to VREG range.

4. Constraint Protection Circuit
   A constraint protection circuit is incorporated in order to protect the output elements and motor when the motor is constrained. The circuit is activated when the Hall signal is not switched for a specific period of time when the motor is in operation. The counter is reset each time the motor rotates 360 degrees in terms of the electrical angle.
   All the $H_{IN}$ and $L_{IN}$ outputs are set to the low level when the constraint protection circuit is in operation.
   This time is determined by the capacitance of the capacitor connected to the CSD pin.

   Oscillation time of CSD pin (1 pulse) $T = |(V_{OH}-V_{OL})/ICHG1| \times C\ (\mu F) + |(V_{OH}-V_{OL})/ICHG2| \times C\ (\mu F)$
   Constraint protection detection time T1 (s) = T × 256 (count)
   Constraint protection time T2 (s) = T × 2816 (count)

   When a 0.022μF capacitor is attached, T = 8.36ms, T1 = 2.14s and T2 = 23.54s are established as the typical ratings. After the motor has been constrained, the constraint protection state is established at 2.14 (s), and then after 23.54 (s) has elapsed, the constraint protection circuit is reset automatically. A time that provides some leeway in the motor start time that factors in any fluctuations must be selected as the setting.

   Conditions for releasing the constraint protection state other than by automatic resetting:
   - When CTL pin voltage < $V_{IM}$ input → protection release and CSD count reset
   - When the low level is detected on the SS pin → protection release and CSD count reset
   - When FR has been switched → protection release and CSD count reset
   - When TSD protection is detected → CSD count stop

5. Power Supply Stabilization

Since this IC adopts a switching drive technique, the power-supply line level can be disrupted easily. Thus capacitors large enough to stabilize the power supply voltage must be inserted between the $V_{CC}$ pins and ground. If the electrolytic capacitors cannot be connected close to their corresponding pins, ceramic capacitors of about 0.1μF must be connected near these pins.

If diodes are inserted in the power-supply line to prevent destruction of the device when the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.

6. VREG Stabilization

Connect a capacitor with a capacitance of 0.1μF or more between VREG5 and ground in order to stabilize the VREG voltage that is the power supply of the control circuit.

The ground lead of that capacitor must be located as close as possible to the control system ground (SGND) of the IC.

7. Forward/Reverse Switching (F/R pin)

Switching between forward rotation and reverse rotation must not be undertaken while the motor is running.

8. PWM Frequency Setting

$$fCPWM \approx 1/(1.7CR)$$

Components with good temperature characteristics must be used.

An oscillation frequency of about 17kHz is obtained when a 2200pF capacitor and 15kΩ resistor are used. If the PWM frequency is too low, switching noise will be heard from the motor; conversely, if it is too high, the output power loss will increase. For this reason, a frequency between 15kHz and 30kHz or so is desirable. The capacitor ground must be connected as close as possible to the control system ground (SGND pin) of the IC to minimize the effects of the outputs.

If there are no fluctuations in the capacitance or resistance of the external capacitors or resistors and only the IC fluctuations are to be considered, an actual capability of ±3% can be expected.