Ordering number : ENA2143

LV8068V

ON Semiconductor®

http://onsemi.com

Bi-CMOS IC

Fan Motor Driver

Single-Phase Full-Wave Driver

Overview

The LV8068V is single-phase bipolar fan motor is driven, through BTL output linear driver, at high efficiency, low power, and low noise by suppressing the reactive power. The BTL output can put PWM control by an outside signal together, which is optimum for the CPU cooler, etc.

Functions

- Single-phase full-wave operating by BTL output (BTL amplifier gain : +49dB)
- Speed control available by PWM input
- The characteristic of the motor rotational speed adjust by “VCONT” voltage
- The characteristic of the motor rotational minimum speed adjust by “RMI” voltage
- Hall bias output terminal (VHB = 1.32V (typ))
- Built-in Quick Start circuit
- Startup support function (50% Duty Start)
- FG (rotate detection) output terminal (Open drain output)
- RD (Lock detection) output terminal (Open drain output)
- Built-in Current Limiter circuit (limit at I_O = 250mA with Rf = 1 connection, the limiter value determined with Rf.)
- Built-in lock protection and automatic return circuit
- Built-in thermal shut-down (TSD) circuit

Specitications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		18	V
OUT pin output current	I_{OUT} max	In regular mode	1.2	A
OUT pin output voltage handling	V_{OUT} max		18	V
RD output voltage handling	V_{RD} max		18	V
RD output current	I_{RD} max		5	mA
FG output voltage handling	V_{FG} max		18	V
FG output current	I_{FG} max		5	mA
HB output current	I_{HB} max		10	mA
PWM input voltage handling	VPWM max		7	V
Allowable power dissipation	Pd max	IC On board*	0.8	W
Operating temperature	Topr		-40 to +90	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy board

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage1	V_{CC} op1	Active at all circuit	6.0 to 16.0	V
Operating supply voltage2	V_{CC} op2	Start-up with PWM=H and RMI=VCONT=L	4.0 to 6.0	V
Hall input common-mode input voltage range	VICM		0.3 to 5VREG-1.5	V
VCONT input voltage range	VCONTIN		0.3 to 5VREG	V
RMI input voltage range	VRMIIN		0.3 to 5VREG	V
PWM input frequency range	FPWMIN		20 to 50	kHz

Electrical Characteristics at Ta = 25°C, V_{CC} = 12.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_{CC}			6	8	mA
5VREG output voltage	VRGL	I5VREG = 5mA	4.7	5.0	5.3	V
REGH output voltage	VRGH	IREGH = 5mA	V_{CC}-4.6	V_{CC}-4.2	V_{CC}-3.9	V
HB bias voltage	VHB	IHB = 5mA	1.22	1.32	1.42	V
Hall Input bias current	IHIN				1	µA
Output ON voltage	V_O	I_O = 250mA, source + sink		0.35	0.5	V
Current limiter	VRF		200	250	300	mV
Hall amplifier output offset voltage	V_{IN}OFS		-10		10	mV
Hall amplifier voltage gain	GH		44	49		dB
PWM pin bias current	IPWM	PWM = GND	-20	-10	-3	µA
PWM pin input Low level	V_{PWM}L		0		0.7	V
PWM pin input High level	V_{PWM}H		2.5		5VREG	V
PWM input smallest pulse width	TPWM	Design guarantee*		5		µs
CPWM charge current	ICPC		13	18	23	µA
CPWM discharge current	ICPD		13	18	23	µA
CPWM charge/ discharge current ratio	ICPRTO	ICPRTO = ICPC/ICPD	0.7	1	1.2	
CPWM oscillation High level	VCPH		3.3	3.5	3.8	V
CPWM oscillation Low level	VCPL		0.7	1.0	1.3	V
CPWM oscillation amplitude width	VCPA		2.3	2.5	2.7	V
VCONT pin input bias current	ICONT				1	µA
RMI pin input bias current	IRMI				1	µA
RD output Low-level voltage	VRD	IRD = 3mA			0.3	V

*: Design guarantee: Indicates a design target value. These parameters are not tested in the independent IC.

Continued on next page.

Continued from preceding page.

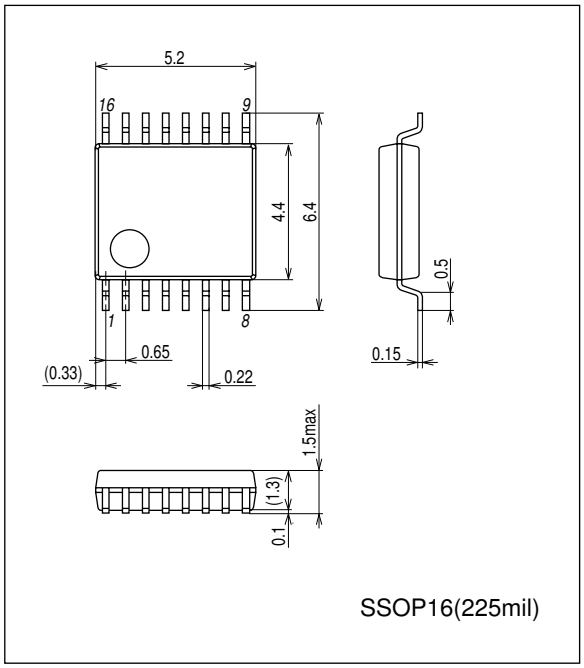
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RD output leakage current	I_{RDL}	VRD = 18V			10	μA
FG output Low-level voltage	V_{FG}	I_{FG} = 3mA			0.3	V
FG output leakage current	I_{FGL}	V_{FG} = 18V			10	μA
FG comparator hysteresis width	ΔVFG		±2	±4	±10	mV
Output ON time in Lock-detection	TACT	CPWM = 100pF	0.35	0.5	0.65	sec
Output OFF time in Lock-detection	TDET	CPWM = 100pF	3.0	4.5	6.0	sec
Output ON/OFF ratio in Lock-detection	TRTO	TRTO = TDET/TACT	7	9	11	
Thermal shutdown oprating temperature	TSD	Design guarantee*		180		°C
Thermal shutdown hysteresis width	ΔTSD	Design guarantee*		40		°C

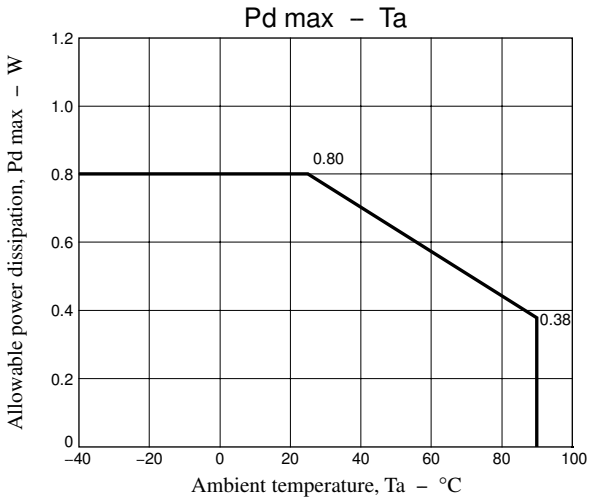
* Design guarantee: Indicates a design target value. These parameters are not tested in the independent IC.

Package Dimensions

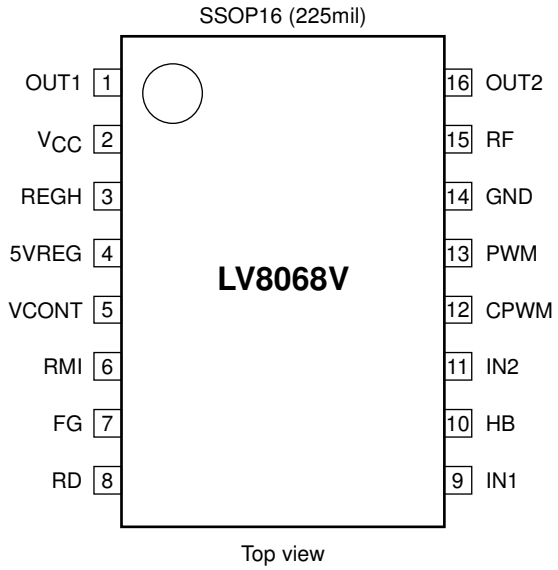
unit : mm (typ)

3178B

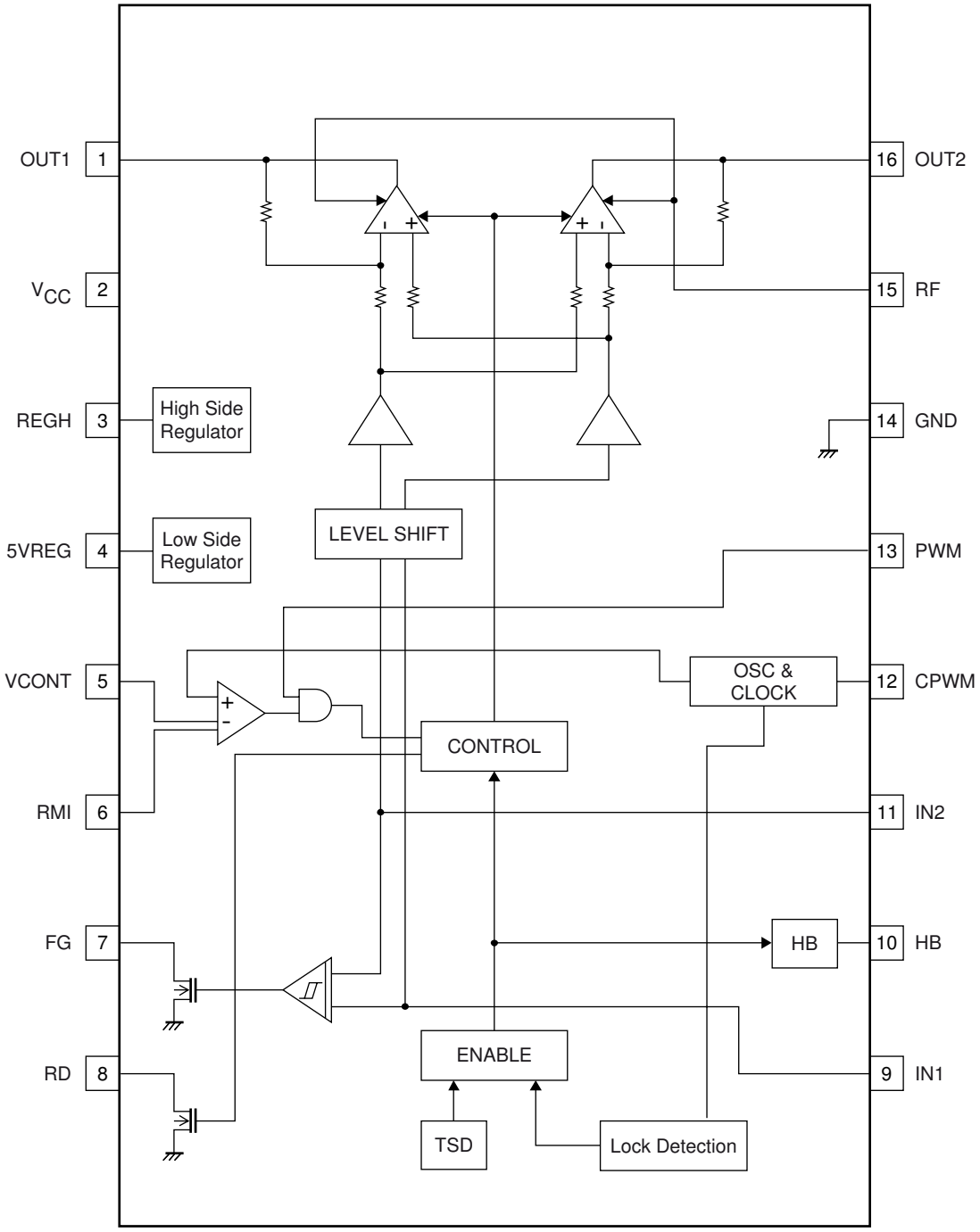




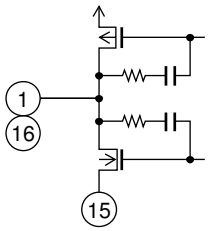
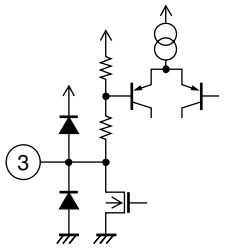
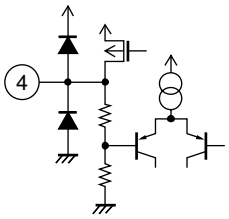
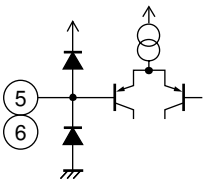
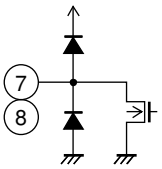
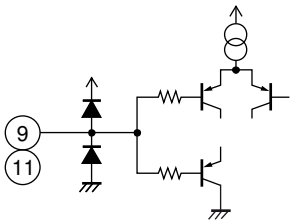
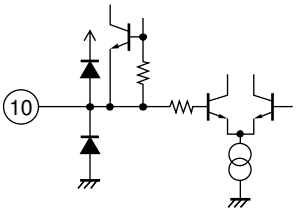
Pin Assignment



Block Diagram

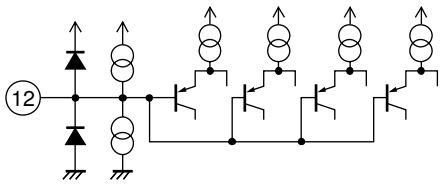
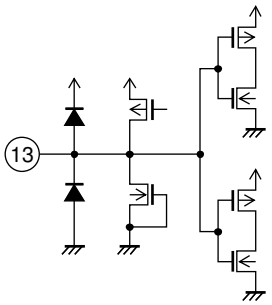
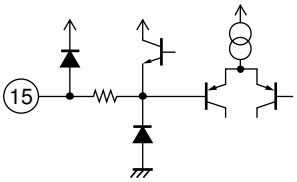


Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	OUT1	Motor driver output pin	
16	OUT2	Motor driver output pin	
2	VCC	Voltage supply pin	
3	REGH	Regulator voltage output pin for internal circuit (Upper side)	
4	5VREG	Regulator voltage output pin for internal circuit (Lower side)	
5	VCONT	Output duty control pin for CPWM	
6	RMI	Output minimum duty control pin for CPWM	
7	FG	FG pulse output pin	
8	RD	RD pulse output pin	
9	IN1	Hall input - pin	
11	IN2	Hall input + pin	
10	HB	Hall bias output pin	

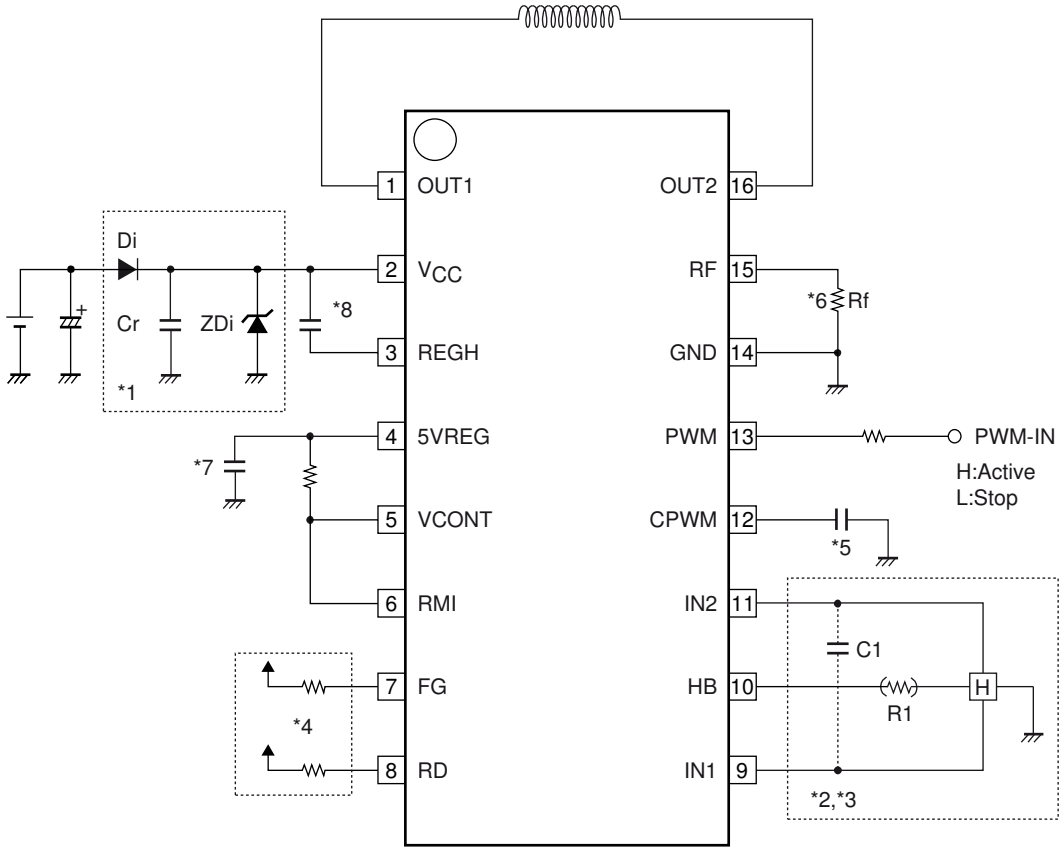
Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Function	Equivalent circuit
12	CPWM	Capacitor connection pin for PWM oscillator and Main clock	
13	PWM	PWM control input pin	
14	GND		
15	RF	Reference voltage pin for current limiter	

Sample Application Circuit

1. Speed control by PWM pin



*1 When the diode Di is used to prevent device destruction from reverse connection, the capacitor Cr must be inserted to assure a path for regenerative currents.
Similarly, if there no nearby capacitors on the fan power supply line, the capacitor Cr is also required to increase reliability. When a protection diode against reverse connection is used, if supply voltage increases due to coil kickback, connect zener diode between power supply and GND.

*2 The Hall element is biased at a constant voltage of approximately 1.3V from the HB pin. Thus the LV8068V provides a stable Hall output with excellent temperature characteristics. If the Hall output is needed to adjust the amplitude, use the resistor R1 as shown in the figure.

*3 When the wiring from the Hall output to IC Hall input is long, noise may be carried through the wiring. In this case, insert the capacitor C1 as shown in the figure.

*4 FG/RD pin is open collector (drain) output. This pin must be left open if unused.

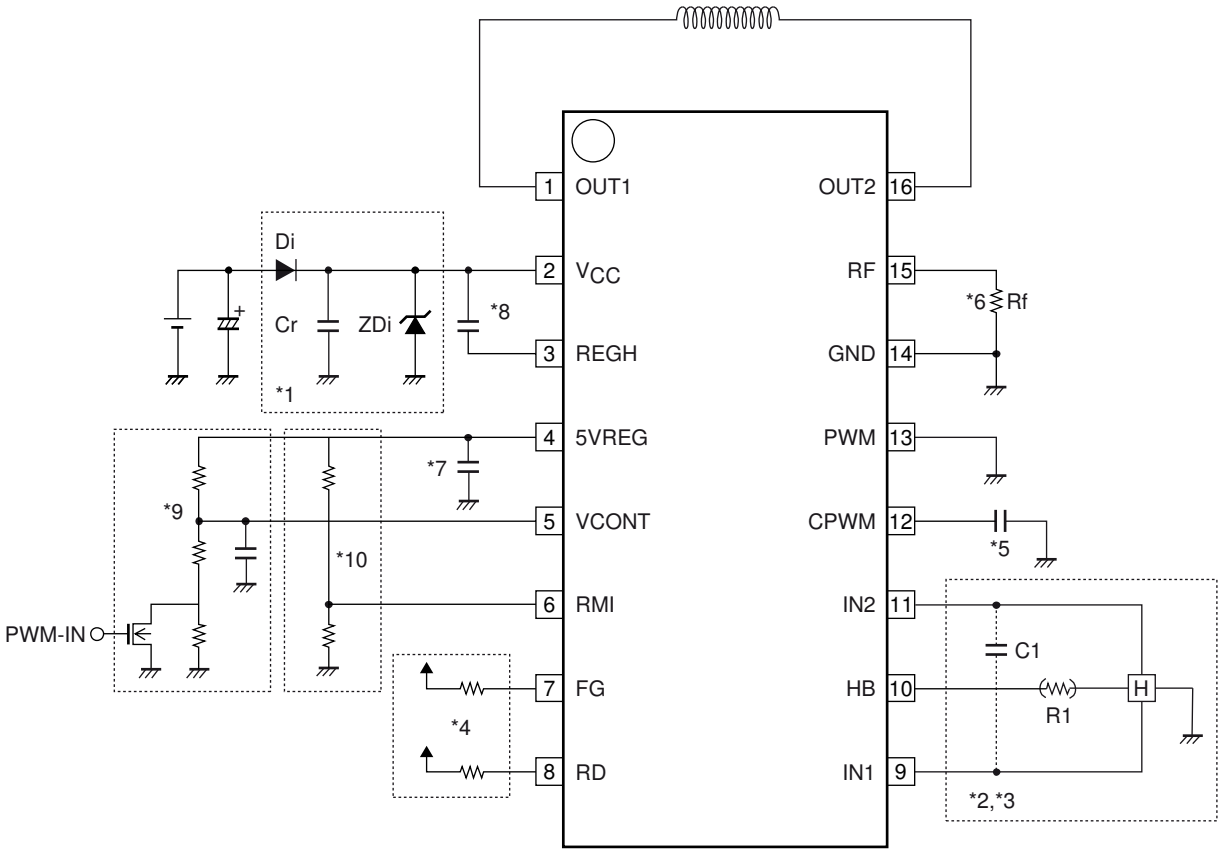
*5 It is a capacitor for PWM oscillations. (Cpwm = 100pF, fpwm = about 33kHz (typ))

*6 The current limiter is activated when the voltage between current detection resistor exceeds 0.25V between GND and RF. The current limiter is activated at I_O = 250mA when R_L = 1Ω. Setting is made with the Rf resistance.
Short-circuit GND and RF when the current-limiter PWM is not to be used.

*7 Please insert enough capacitor value between GND and RGL for stabilization on a terminal.

*8 Please insert enough capacitor value between Vcc and RGH for stabilization on a terminal.

2. Speed control by VCONT/RMI pin



*1 When the diode Di is used to prevent device destruction from reverse connection, the capacitor Cr must be inserted to assure a path for regenerative currents.
Similarly, if there no nearby capacitors on the fan power supply line, the capacitor Cr is also required to increase reliability. When a protection diode against reverse connection is used, if supply voltage increases due to coil kickback, connect zener diode between power supply and GND.

*2 The Hall element is biased at a constant voltage of approximately 1.3V from the HB pin. Thus the LV8068V provides a stable Hall output with excellent temperature characteristics. If the Hall output is needed to adjust the amplitude, use theresistor R1 as shown in the figure.

*3 When the wiring from the Hall output to IC Hall input is long, noise may be carried through the wiring. In this case, insert the capacitor C1 as shown in the figure.

*4 FG/RD pin is open collector (drain) output. This pin must be left open if unused.

*5 It is a capacitor for PWM oscillations. (Cpwm = 100pF, fpwm = about 33kHz (typ))

*6 The current limiter is activated when the voltage between current detection resistor exceeds 0.25V between GND and RF. The current limiter is activated at I_O = 250mA when R_L = 1Ω. Setting is made with the Rf resistance.
Short-circuit GND and RF when the current limiter PWM is not to be used.

*7 Please insert enough capacitor value between GND and RGL for stabilization on a terminal.

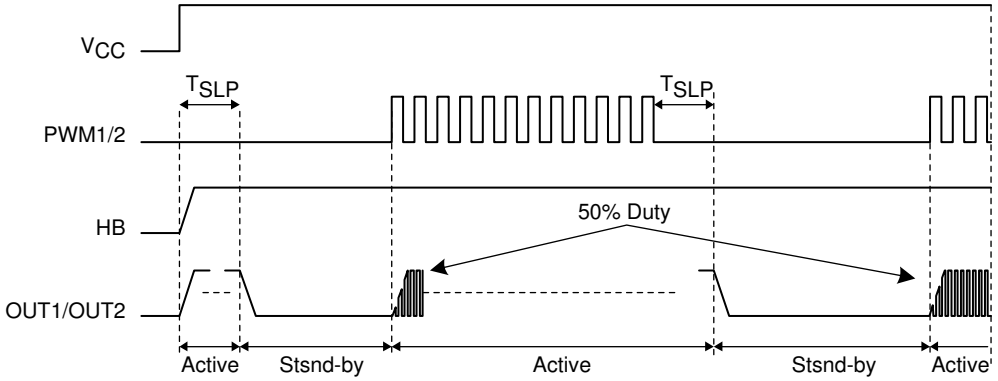
*8 Please insert enough capacitor value between Vcc and RGH for stabilization on a terminal.

*9 VCONT is speed control pin. For the control method ,refer to the timing chart.

*10 RMI is minimum speed setting pin. When you do not use RMI, please make pull-up to 5VREG

Timing Chart

1. Stand-by/Start-up



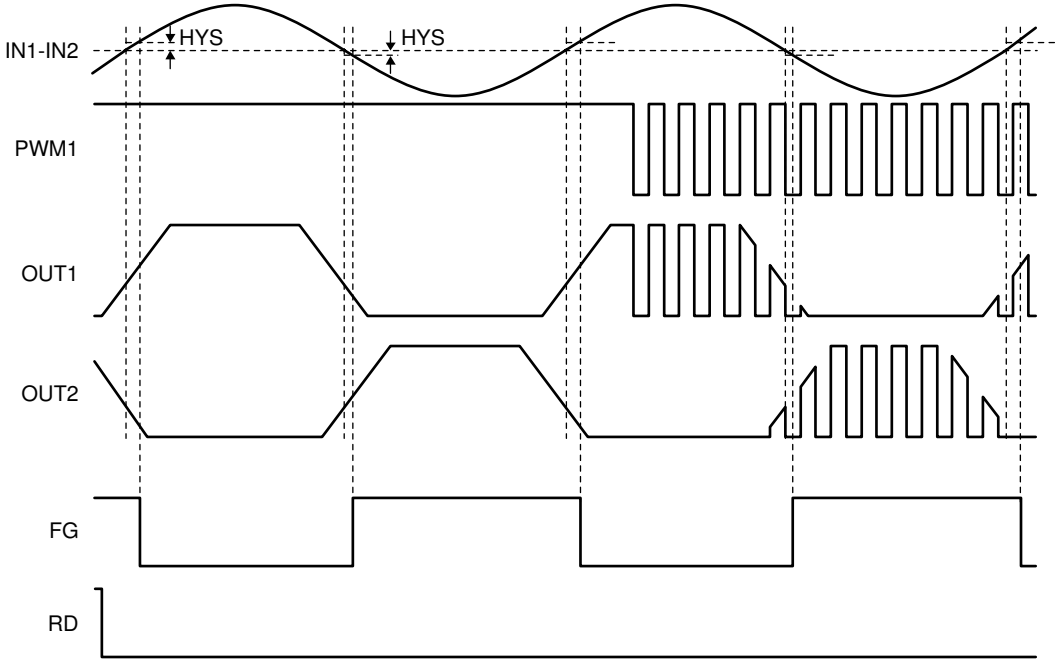
*T_{SLP} = 400μs (typ)

*When PWM signal is input "L" level for continuousness TSLP, it becones the Stand-by mode by detecting above situation.

*When "H" level is input, it becomes the Active mode at once.

2. In Regular-Rotation

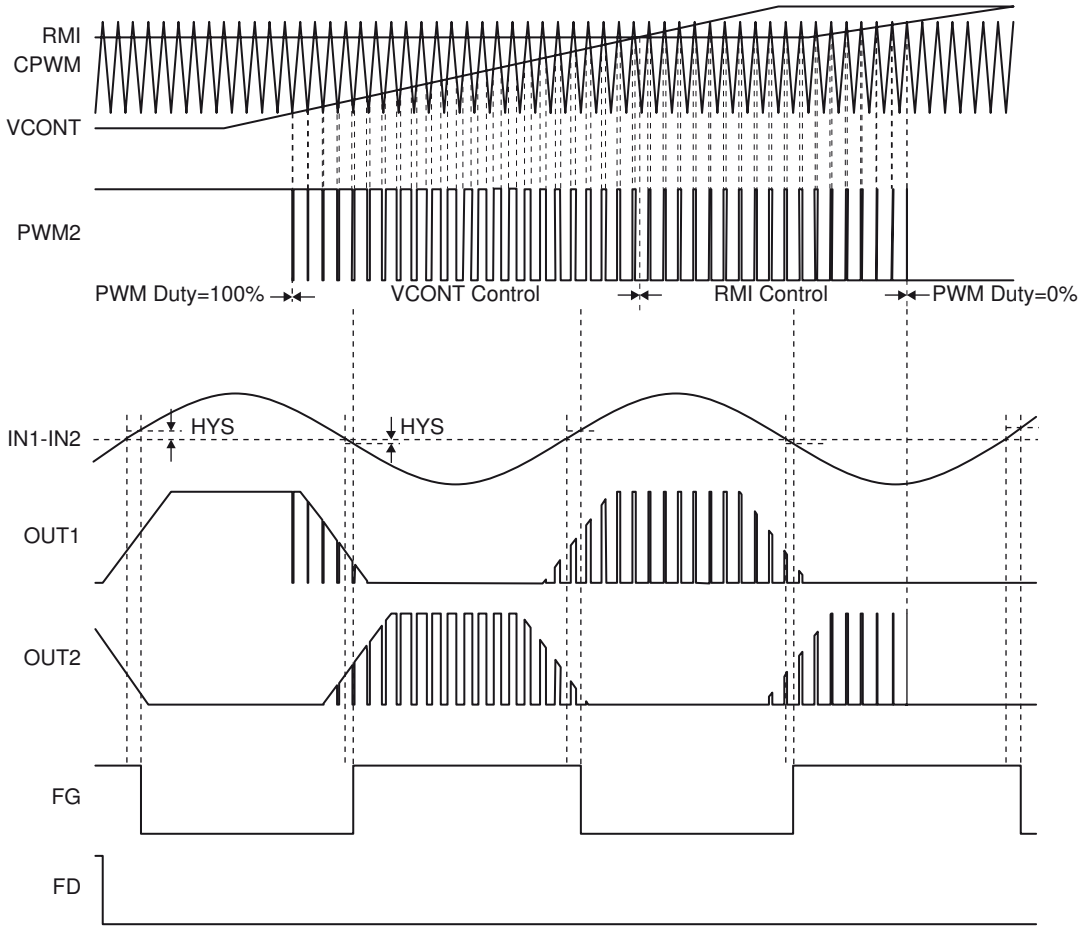
• PWM pin control



• Truth table of mode in Regular-Rotation at PWM pin

IN1	IN2	PWM	OUT1	OUT2	FG	Mode
H	L	H	H	L	L	Drive
		L	L	L		Regenerate
L	H	H	L	H	OFF	Drive
		L	L	L		Regenerate

• VCONT/RMI pin control



• Truth table of mode in Regular-Rotation at VCONT/RMI pin

IN1	IN2	*PWM2	OUT1	OUT2	FG	Mode
H	L	H	H	L	L	Drive
		L	L	L		Regenerate
L	H	H	L	H	OFF	Drive
		L	L	L		Regenerate

*: IC's internal signal

3. In Motor-Lock