Ordering number : ENA0752

STK672-410

ON Semiconductor®

http://onsemi.com

Thick-Film Hybrid IC

2-phase Stepping Motor Driver

Overview

The STK672-410 is a hybrid IC for use as a unipolar, 2-phase stepping motor driver with PWM current control.

Applications

- Office photocopiers, printers, etc.

Features

- Entry of external clock is enough to activate the micro step sinusoidal driver.
- The excitation mode of 2, 1-2, W1-2, 2W1-2, or 4W1-2 can be selected with the external pin.
- The 4-phase distributor switching timing can be set to occur either on both rising and falling edge detection or on rising edge detection only with an external pin (MODE3).
- A phase holding function is provided to prevent phase skip during switching of excitation in the course of operation.
- The motor current is set by a voltage divider formed by an external resistor connected to the Vref pin.
- The CLK input pin is provided with an internal noise filtering circuit in addition to a Schmidt circuit to increase the margin for extraneous noise.
- When set low, the ENABLE pin turns off the motor drive current for all phases and retains the phase excitation state.

June, 2013

91212HKPC 018-08-0108 No.A0752-1/19

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +5.8	V
Output current	I_{OH} max	V_{DD}=5V, CLOCK≥200Hz	3.2	A
Allowable power dissipation	Pd max	With an arbitrarily large heat sink. Per MOSFET	10	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	10 to 45	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input high voltage	V_{IH}		0 to 5.8	V
Output current	I_{OH}	Tc=105°C, CLOCK≥200Hz	3	A
Phase driver withstand voltage	V_{DSS}	TR1, 2, 3, 4 I_D=1mA (Tc=25°C)	100min	V

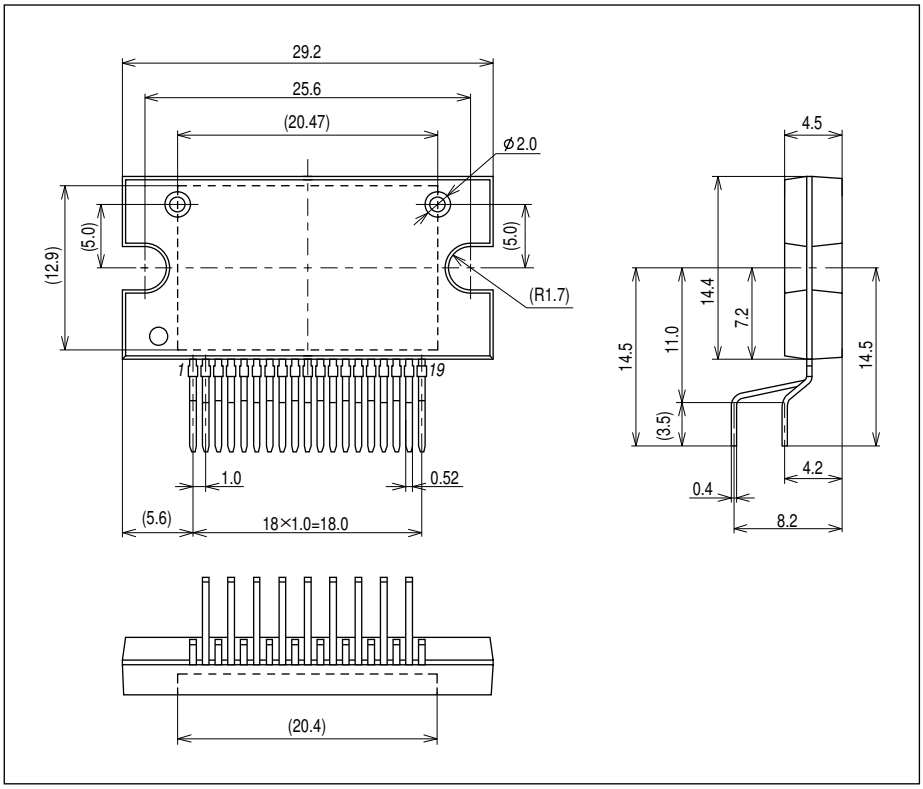
Electrical Characteristics at Tc=25°C, V_{CC}=24V, V_{DD}=5.0V

Parameter			Symbol	Conditions	min	typ	max	unit
V_{DD} supply current			I_{CCO}	V_{DD}=5.0V, ENABLE=Low Vref=2V	6	10	15	mA
Output average current			Ioave	R/L=3Ω/3.8mH in each phase	0.51	0.59	0.66	A
FET diode forward voltage			Vdf	If=1A		1.2	1.6	V
Output saturation voltage			Vsat	R_L=23Ω		0.3	0.5	V
Control input pin	Input voltage		V_{IH}	Except for the Vref pin	2.5			V
			V_{IL}	Except for the Vref pin			0.6	V
	Input current		I_{IH}	Except for the Vref pin V_{IN}=5V			10	μA
			I_{IL}	Except for the Vref pin V_{IN}=0V			10	μA
Vref pin	Input voltage		VI	Pin 19	2		V_{DD}	V
	Input current		Ios	Pin 19, V_{DD} input		12.5		μA
PWM frequency			fc		37.5	50	62.5	kHz
Current Distribution Ratio								
2W1-2	W1-2	1-2	Vref *1	θ=7/8		100		%
2W1-2	W1-2			θ=6/8		93		
2W1-2				θ=5/8		84		
2W1-2	W1-2	1-2		θ=4/8		71		
2W1-2				θ=3/8		55		
2W1-2	W1-2			θ=2/8		40		
2W1-2				θ=1/8		19		
2						100		

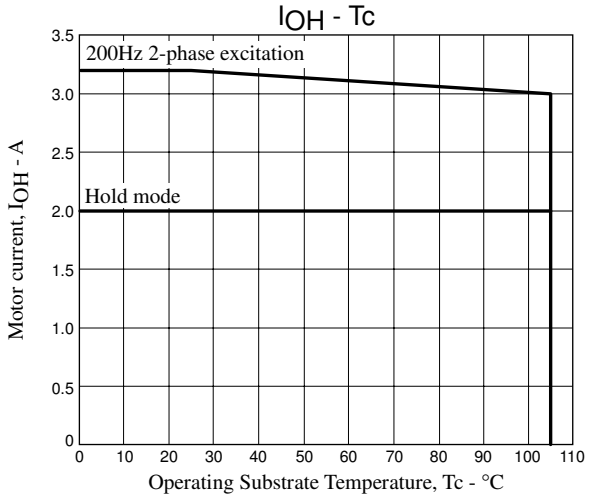
Notes: A fixed-voltage power supply must be used.
The value of Item 1 is the design target and not measured.

Package Dimensions

unit:mm (typ)



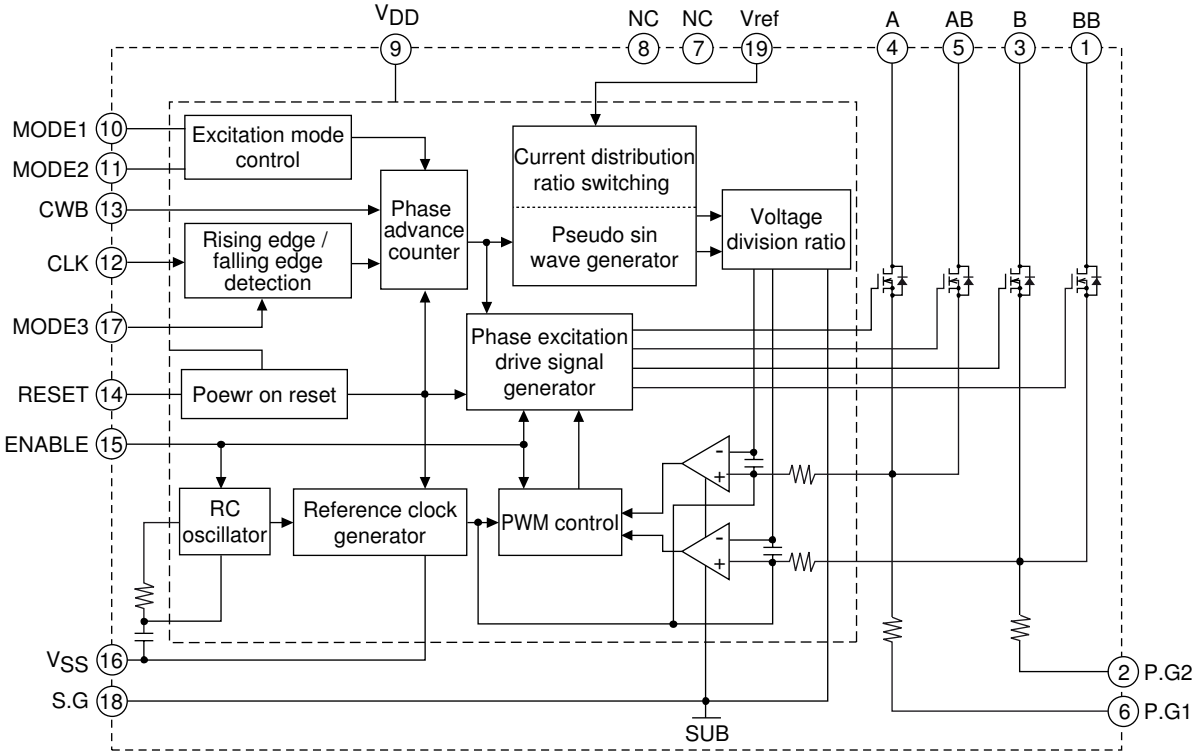
Derating Curve of Motor Current, I_{OH}, vs. STK672-410 Operating Substrate Temperature, Tc



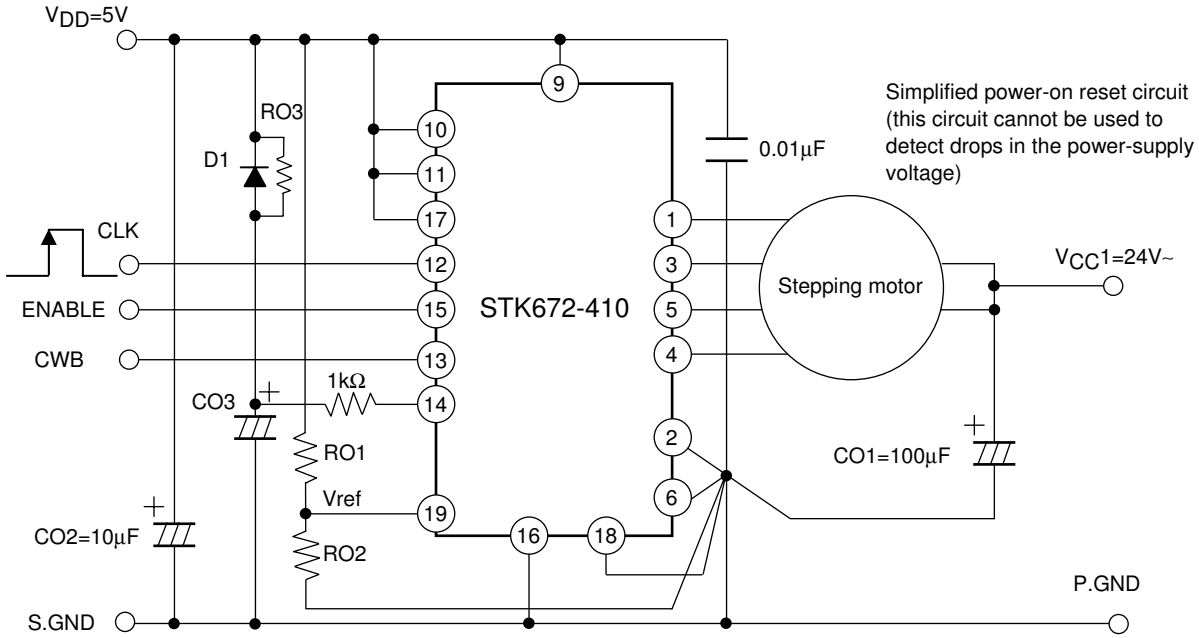
Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-4** series hybrid ICs given in a separate document.
- The operating substrate temperature, Tc, given above is measured while the motor is operating.
  Because Tc varies depending on the ambient temperature, Ta, the value of I_{OH}, and the continuous or intermittent operation of I_{OH}, always verify this value using an actual set.

Block Diagram



Sample Application Circuit



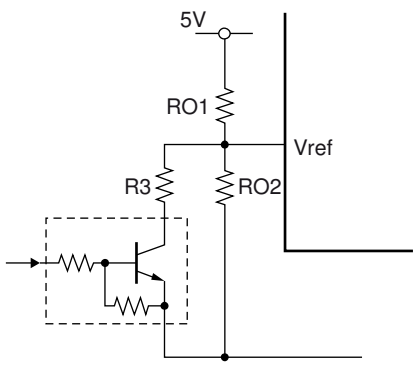
Precautions

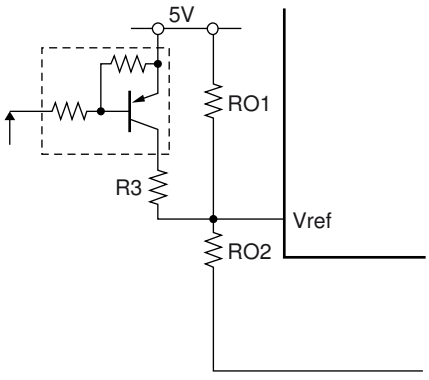
[Internal MOSFET Destruction]
- The internal MOSFFET gate voltage is supplied from the 5V power supply. If the 5V power supply voltage is below its allowable operating voltage range, the resultant insufficient gate drive state may destroy the MOSFET.

[GND wiring]
- To reduce noise in the 24V system, locate the ground side of CO1 in the circuit above as close as possible to pins 2 and 6 on the hybrid IC. Also, to assure that the current is set accurately, the Vref ground side must be connected to a ground point that is a shared connection between the ground pin (pin 18, S.G) used for the current setting and P.G1 and P.G2.
- If the V_{SS} pin (pin 16) near the driver, the S.G pin (pin 18), the P.G1 pin (pin 2), and the P.G2 pin (pin 6) cannot be connected to a single-point ground, connect the V_{SS} pin to the control system S.GND, and the S.G pin to the P.G1 pin and the P.G2 pin.

[Input pins]
- The voltage range for the input pins is -0.3 to +5.8V. Design applications so that voltages lower than -0.3V and higher than 5.8V are never applied to the input pin.
- Do not connect any of the NC pins (pins 7, and 8) shown in the internal equivalent circuit block diagram to the circuit pattern on the printed circuit board.
- Connect a resistor (1kΩ) so that discharge energy of capacitor CO2 does not enter the hybrid IC.
- Inputs to pins 10, 11, 12, 13, 14, 15, and 17 are signal whose high level is 2.5V. Both TTL and CMOS inputs are supported.
- Internal pull-up resistors are not provided for the input pins. If this hybrid IC's inputs are controlled by open-collector type circuits, external pull-up resistors must be provided.
- If resistors are connected in series with the inputs, insert capacitors between the inputs and ground to prevent malfunctions due to the hybrid IC's switching noise.
- In the application circuit example, a simple reset circuit is formed by D1, RO3, CO2, and a 1kΩ resistor. This circuit will not create a reset signal if the 5V supply voltage drops briefly. This circuit structure requires the 5V supply voltage to fall below 0.6V to operate.
  Connect the hybrid IC directly to V_{DD} to use the hybrid IC's power on reset function.
- A power on reset operation must be applied when the 5V power supply level is first applied.

[Vref Current Setting]
- To reduce the influence of input impedance 200kΩ input current of the terminal Vref, RO1 recommends about 1kΩ.
- We recommend using the following circuit to temporarily reduce the motor current.
- Although the driver provides a constant current control function, it does not have an overcurrent protection function to assure that the maximum output current, I_{OH} max, is not exceeded. If Vref is set by mistake to a voltage that such that I_{OH} max is exceeded, the driver will draw excessive current and the device will be destroyed.
- If the Vref pin (pin 19) is left open, the Vref voltage will be set to about 2.5V. With the STK672-400, the motor current will then be about 1.8A. With the STK672-410, the motor current will be about 3.2A. These current settings are close to I_{OH} max.

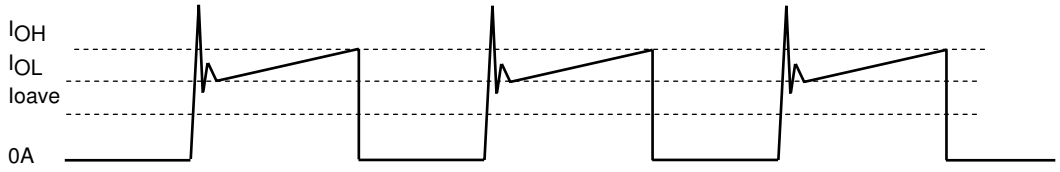




[Setting the motor current]
The motor current is set by the hybrid IC's pin 19V, Vref. The formula shows below gives the relationship between I_{OH} and Vref.

$$Vref = V_{DD}-(I_{OH} \times Rs \times K) \quad \cdots\cdots (1)$$

K: 6.55 (voltage divider ratio)
Rs: 0.122Ω (hybrid IC internal current detection resistance: precision = ±3%)



Model of the Motor Phase Current Flowing into the Hybrid IC

Function Table

M2	0	0	1	1	Phase switching clock edge timing
M1 / M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	CLK rising edge
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Both CLK edges

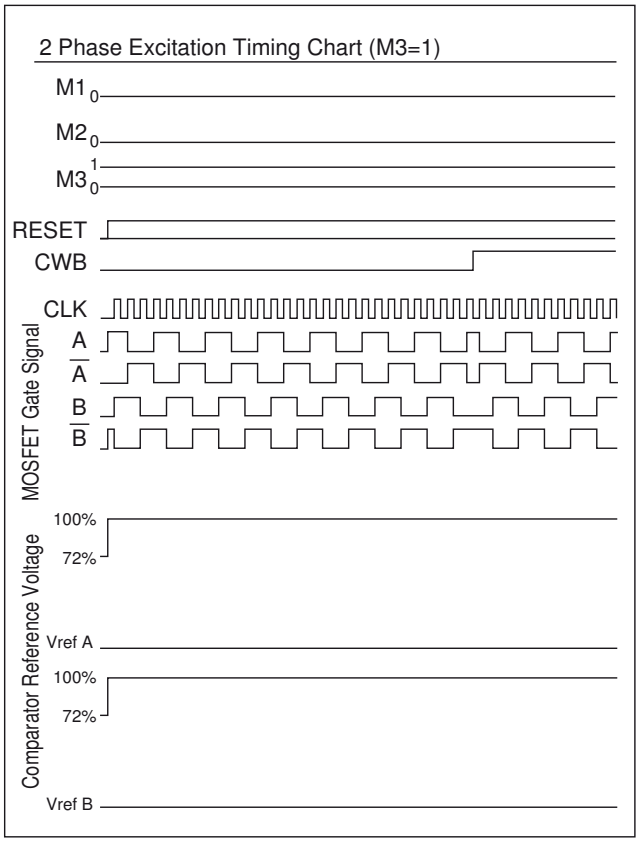
CWB pin

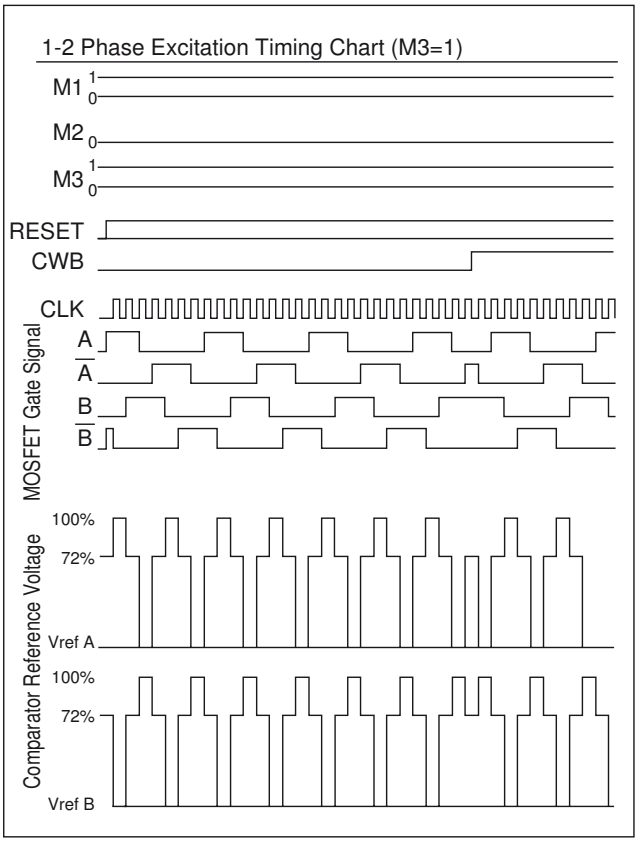
	Forward	Reverse
CWB	0	1

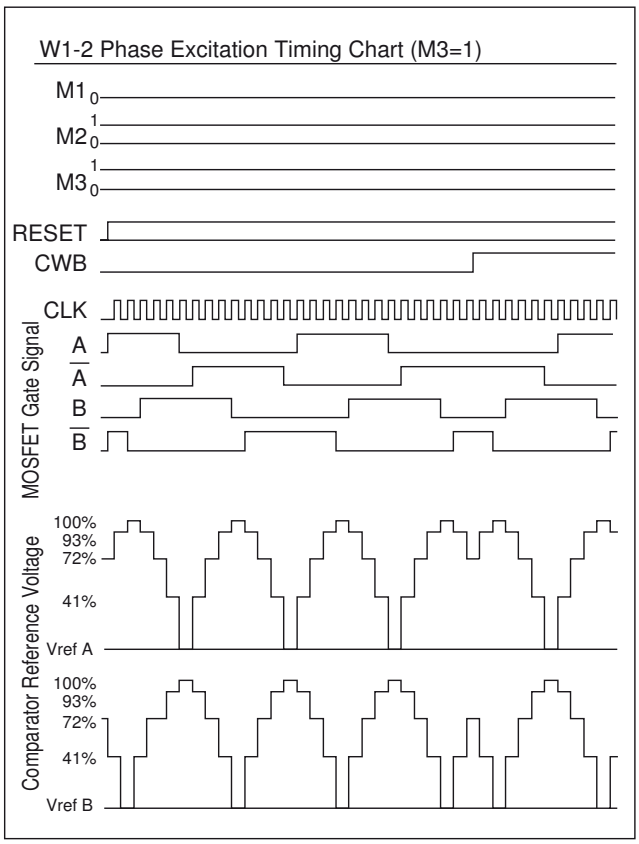
ENABLE and RESET pins

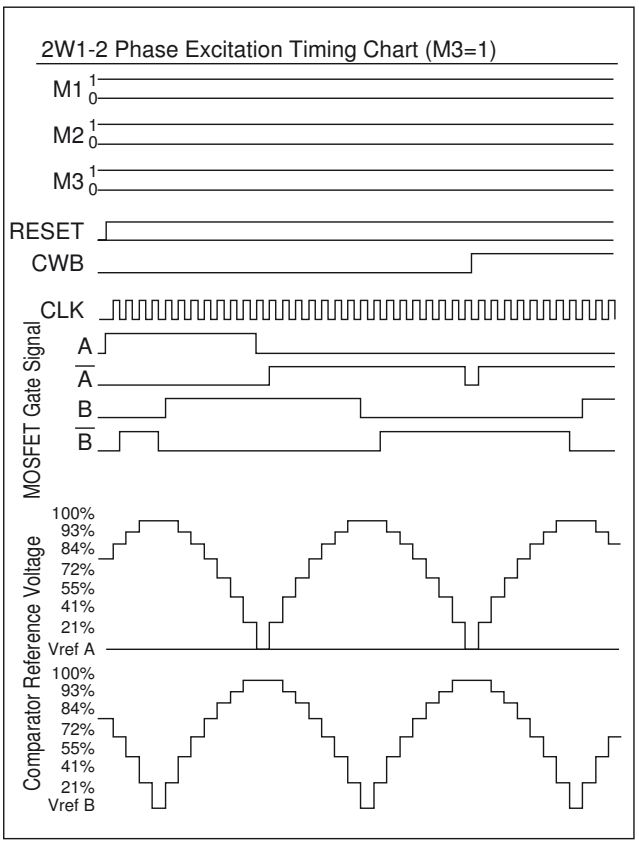
ENABLE	Motor current cut: Low
RESET	Active Low

Timing Charts

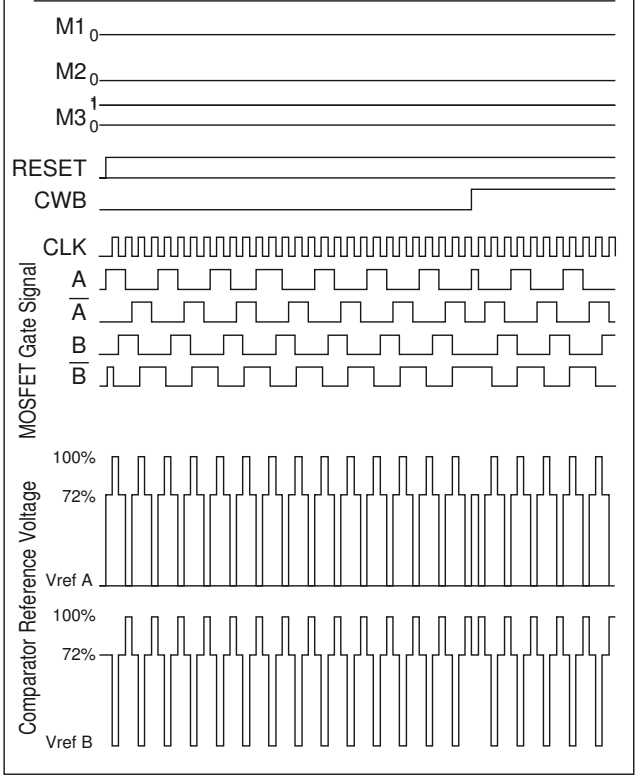




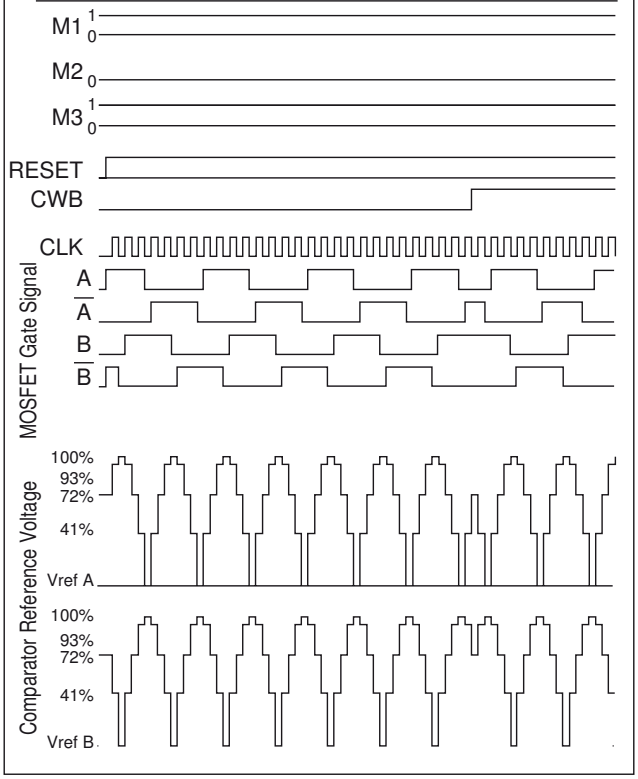




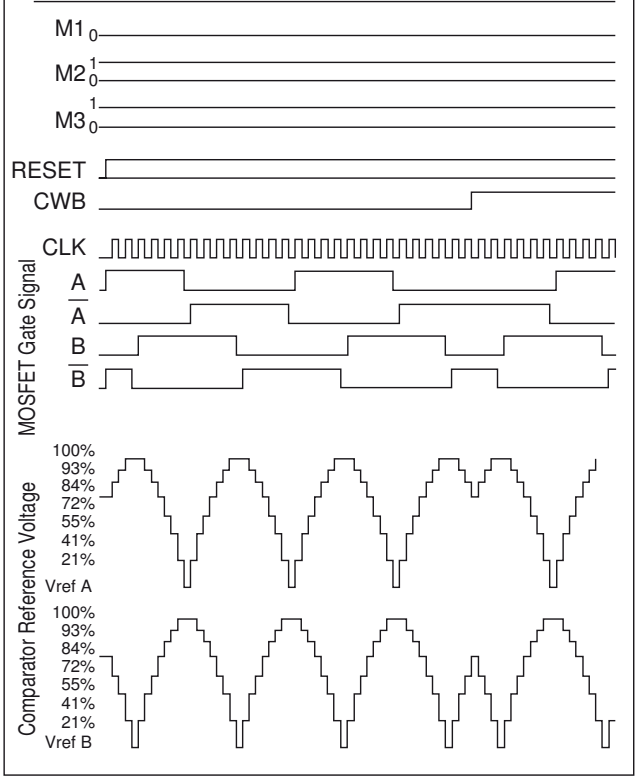
1-2 Phase Excitation Timing Chart (M3=0)



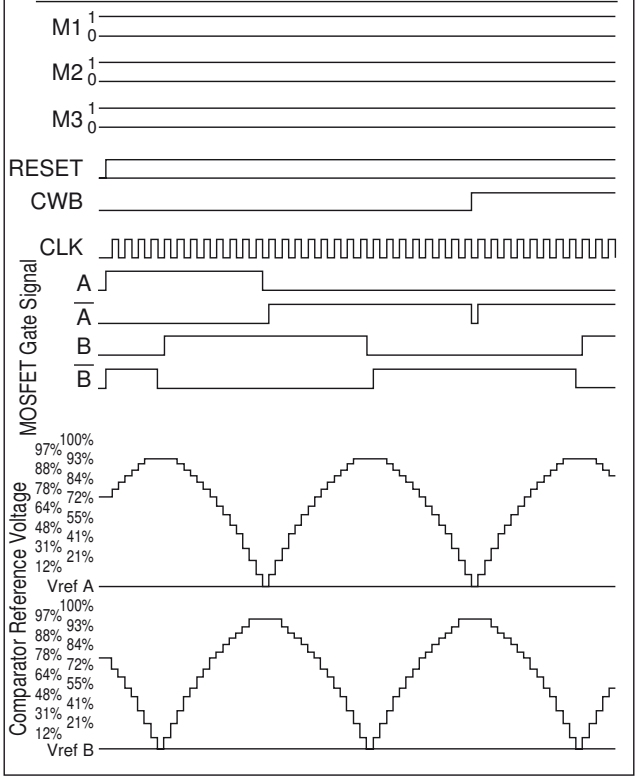
W1-2 Phase Excitation Timing Chart (M3=0)



2W1-2 Phase Excitation Timing Chart (M3=0)



4W1-2 Phase Excitation Timing Chart (M3=0)



Usage Notes

1. Input pins and functional overview

[Input pins]

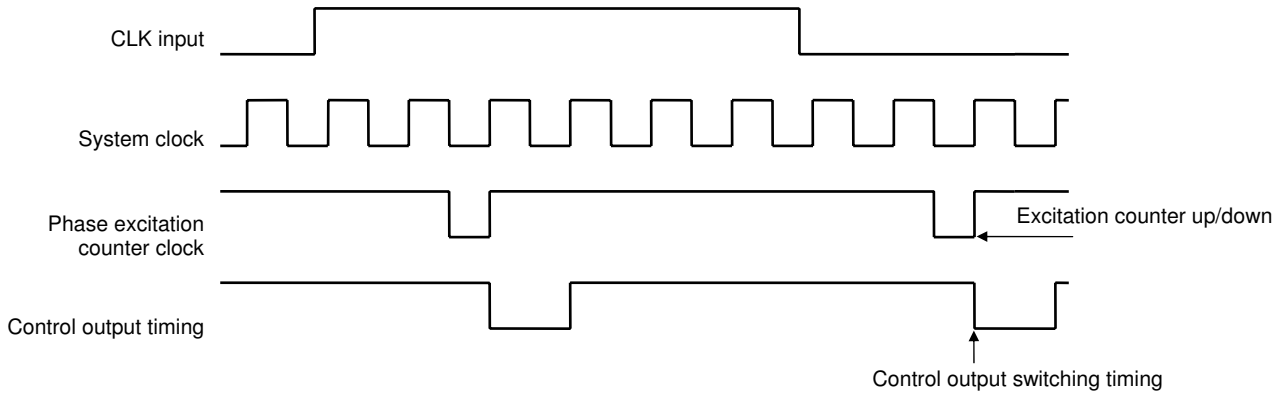
Hybrid IC pin No.	Symbol	Function	Pin type
19	Vref	Current setting	Input impedance: 200kΩ (typical)
10, 11, 13	MODE1, MODE2, MODE3	Excitation mode setting	TTL level Schmitt input
12	CLK	Phase switching clock (speed command)	Same as the above
13	CWB	Motor direction setting	Same as the above
14	RESET	System reset	Same as the above
15	ENABLE	Motor current off	Same as the above

2. Input signal functions

[CLK (Phase switching clock)]

(1) Input frequency: DC to 50kHz
(2) Minimum pulse width: 10μs
(3) Pulse width duty: 40 to 60%
(4) Pin circuit type: TTL level Schmitt trigger input
(5) A multi-stage noise exclusion circuit is included.
(6) Function
- M3:1
  When M3 is 1:The excitation phase is advanced one step on each CLK signal rising edge.
- M3:0
  When M3 is 0:The excitation phase is advanced one step alternately on each CLK signal rising or falling edge.

• Timing chart



[CWB (Motor direction setting)]

(1) Pin circuit type: TTL level Schmitt trigger input
(2) Function
- When CWB = 0: The motor turns in the clockwise direction
- When CWB = 1: The motor turns in the counterclockwise direction

(3) Note: The value of the CWB input must not be changed in the period from 7μs before a CLK input rising or falling edge until 7μs after that edge.

[ENABLE (Forces the excitation drive outputs A, AB, B, and BB to the off state and selects the hybrid IC's internal state to be operating or hold)]

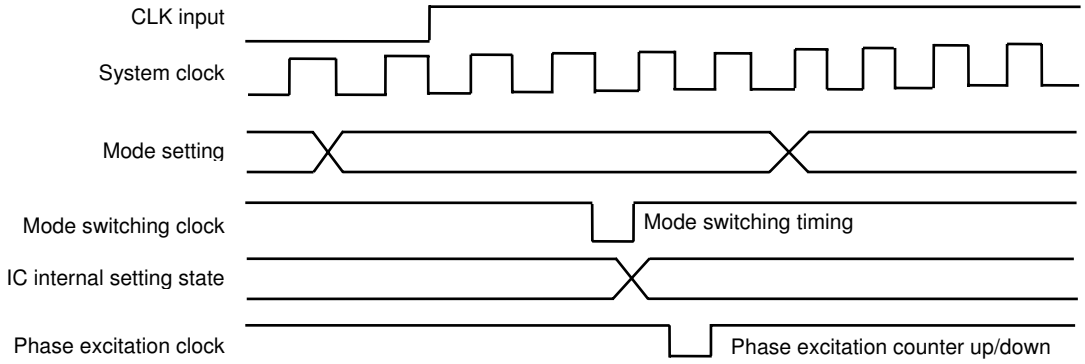
(1) Pin circuit type: TTL level Schmitt trigger input
(2) Function
a) When ENABLE is 1: Normal operating state
b) When ENABLE is 0: The motor current is turned off and the excitation drive output is turned off forcibly. At this time, the hybrid IC's system clock is stopped and the hybrid IC is not influenced by changes to any input pins other than the reset input.

[MODE1, MODE2, and MODE3 (Excitation mode and timing mode selection)]

(1) Pin circuit type: TTL level Schmitt trigger input

(2) Excitation mode selection (See the application circuit example page for details on excitation mode selection.)

(3) Valid mode setting timing: Do not change the mode within the ±7μs period around any rising or falling edge on the CLK input signal.



Mode Setting Acquisition Timing

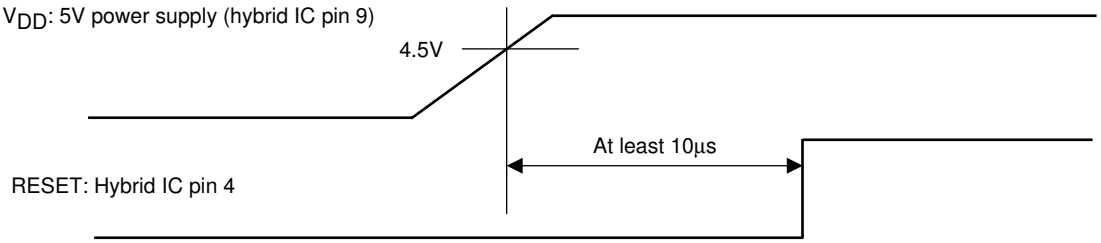
[RESET (Whole system reset)]

(1) Pin circuit type: TTL level Schmitt trigger input

(2) Function: The reset signal to this hybrid IC's internal sequencer can be selected to be either the hybrid IC internal power-on reset function or an external signal. To operate the hybrid IC internal sequencer from the hybrid IC internal power-on reset signal, connect the hybrid IC's pin 14 to V_{DD}. The hybrid IC internal reset signal is generated with a timing such that it is output to internal circuits when V_{DD} is in the range 2.9 to 3.9V.

Alternatively, if an external signal is used as the reset signal, it must have the timing relative to the rise of the V_{DD} voltage shown in the figure below. Note that the reset pulse must have a pulse width of at least 10μs.

• External reset and power supply application sequence



[Vref (Sets the current that is used as the reference for setting the output current)]

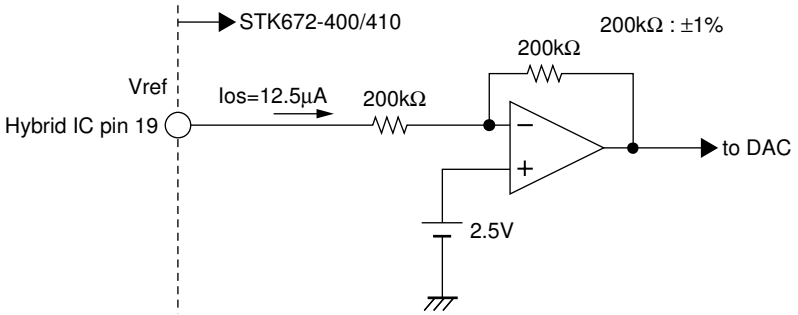
(1) Pin circuit type: Analog input (differential amplifier). Input resistance: 200kΩ

(2) Function: The input voltage must be in the voltage range from the control system power supply V_{DD} to 2V. Note that there is a resistance component (200kΩ, typical) in this hybrid IC's input and that therefore an input current occurs.

If the Vref voltage structure is formed as a resistor voltage divider, that circuit must be designed to take that input current into account. The input current is 12.5μA (typical). Note that this is the current when Vref is 5V. The input current falls according to the formula shown below when the Vref voltage is below that level.

Ios=Vref/(200k+200k) --------- (1)

• Input circuit structure



3. Calculating STK672-410 HIC Internal Power Loss

HIC internal loss calculation of STK672-410
The internal average power loss in the excitation modes of STK672-400 is calculated as follows:

[Excitation modes]
2 phase excitation mode
$2PdAV = (Vsat+Vdf)\times0.5\times CLOCK\times I_{OH}\times t2+0.5\times CLOCK\times I_{OH}\times (Vsat\times t1+Vdf\times t3)$ ---------- (3-1)

1-2 phase excitation mode
$1\text{-}2PdAV = (Vsat+Vdf)\times0.25\times CLOCK\times I_{OH}\times t2+0.25\times CLOCK\times I_{OH}\times (Vsat\times t1+Vdf\times t3)$ ---------- (3-2)

W1-2 phase excitation mode
$W1\text{-}2PdAV =0.64[(Vsat+Vdf)\times0.25\times CLOCK\times I_{OH}\times t2+0.25\times CLOCK\times I_{OH}\times (Vsat\times t1+Vdf\times t3)]$ ---------- (3-3)

2W1-2 phase excitation mode
$2W1\text{-}2PdAV =0.64[(Vsat+Vdf)\times0.0625\times CLOCK\times I_{OH}\times t2+0.0625\times CLOCK\times I_{OH}\times (Vsat\times t1+Vdf\times t3)]$ ------ (3-4)

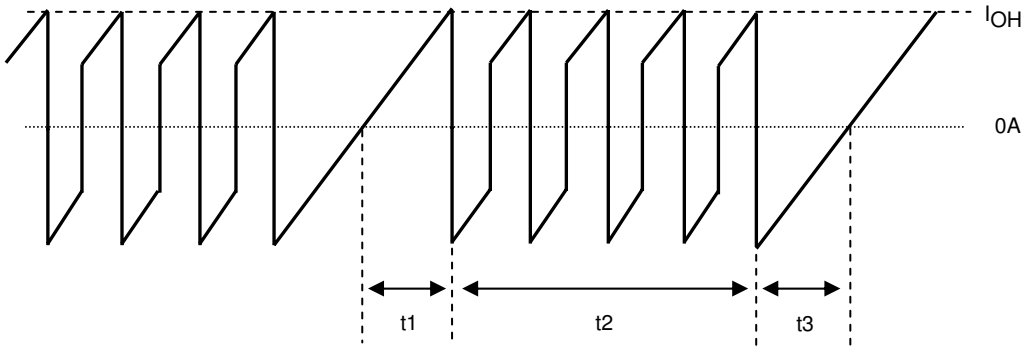
4W1-2 phase excitation mode
$4W1\text{-}2PdAV =0.64[(Vsat+Vdf)\times0.0625\times CLOCK\times I_{OH}\times t2+0.0625\times CLOCK\times I_{OH}\times (Vsat\times t1+Vdf\times t3)]$ ------ (3-5)

At motor hold
$Hold\ PdAV = (Vsat+Vdf)\times I_{OH}$---------- (3-6)

Note: 2-phase 100% conductance is assumed in Equation (3-6).

Vsat: Synthetic voltage of Ron voltage drop + Synthetic voltage of current detection resistance
Vdf: Synthetic voltage of FET body diode Vdf + Synthetic voltage of current detection resistance
CLOCK: Input clock CLK (reference frequency before splitting into four phases)

t1, t2, and t3 are waveforms shown in the following figure:
t1: Time till the winding current reaches the set value (I_{OH}).
t2: Time for the constant-current control (PWM) region
t3: Time from the phase signal OFF up to regenerative consumption of the counter electromotive force



Motor COM Current Waveform Model

$t1= (-L/(R+0.3))\ \ln\ (1-((R+0.3)/V_{CC}1)\times I_{OH}))$ ---------- (3-7)
$t3= (-L/R)\ \ln\ ((V_{CC}1+0.3)/(I_{OH}\times R+V_{CC}1+0.3))$ ---------- (3-8)
$V_{CC}1$: Motor supply voltage (V)
L: Motor inductance (H)
R: Motor winding resistance (Ω)
I_{OH}: Motor set output current crest value (A)

Phase signal ON time T and constant-current control time t2 in excitation modes

(1) 2 phase excitation mode	t2 = (2÷CLOCK) - (t1 + t3)·····(3-9)
(2) 1-2 phase excitation mode	t2 = (3÷CLOCK) - t1·····(3-10)
(3) W1-2 mode	t2 = (7÷CLOCK) - t1·····(3-11)
(4) 2W1-2 phase excitation (4W1-2 phase excitation)	t2 = (15÷CLOCK) - t1·····(3-12)

Enter the value of Vsat and Vdf from Vsat vs I_{OH} and Vdf vs I_{OH} graphs for the set current value of I_{OH}.
Compare the HIC average power loss thus determined with the ΔTc vs Pd graph to determine whether the heat sink is necessary. See the section on STK672-410 thermal design section later in this document for details on heat sink design.
The value HIC for the average power loss PdAV is the loss when the device is not in the avalanche state. To add the avalanche state loss, add the STK672-410 avalanche energy allowable value from equation (2) to the PdAV value above.
When the fin is not used, the HIC substrate temperature Tc changes because of the effect of air convection, etc. Be sure to check temperature rise with the set.

[Calculating PAVL, the average power loss in the avalanche state]
The average power loss in the avalanche state, PAVL, is given by formula (4-2), which is the expression for the loss, PAVL, in the avalanche state during constant-current chopping operation multiplied by the chopping frequency.

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \cdots\cdots (4\text{-}2)$$

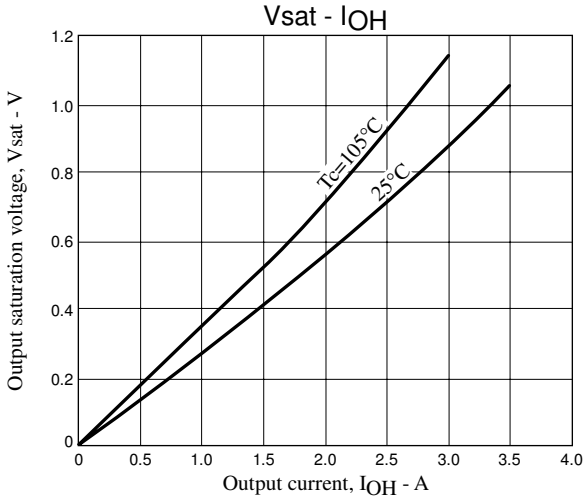
fc: Hz (Use the maximum PWM frequency for the STK672-400 series.)

The values for V_{DSS}, IAVL, and tAVL must be observed with an oscilloscope in an actual operating circuit based on the STK672-410 series device, and those values must then be substituted into these equations.

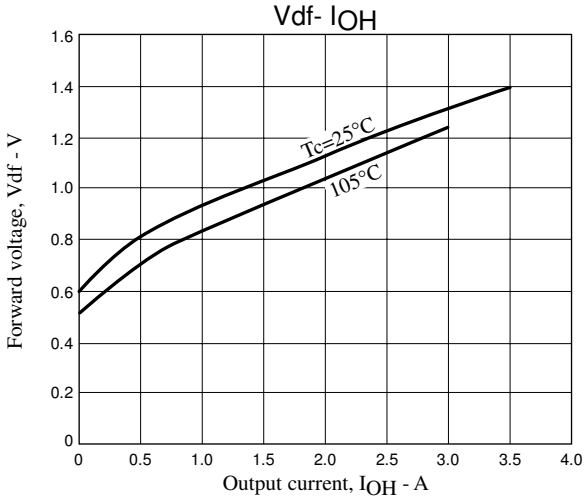
The PAVL added differs for the different excitation modes: for modes other than 2 phase excitation, multiply PAVL by the following constant and then add to the hybrid IC internal average power loss.

For 1-2 phase excitation and higher modes: PAVL(1)=0.7×PAVL·····(3-13)
For 2 phase excitation mode and motor hold mode: PAVL(1)=1×PAVL·····(3-14)

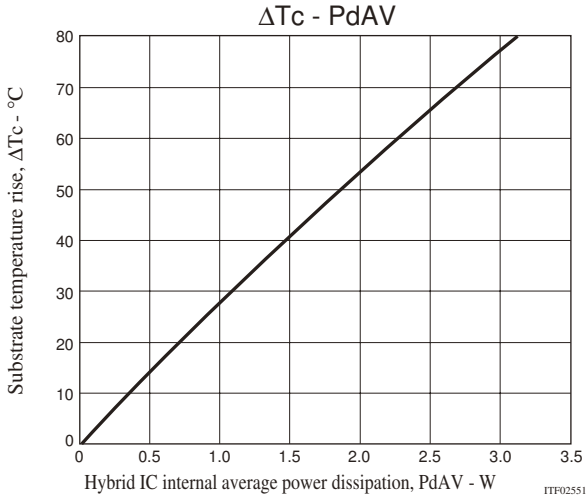
STK672-410 Output saturation voltage, Vsat - Output current, I_{OH}



STK672-410 Forward voltage, Vdf -Output current, I_{OH}



Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV



4. STK672-410 Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-400 hybrid IC, the waveforms shown in Figure 1 below result for the output current, I_D, and voltage, V_{DS}.

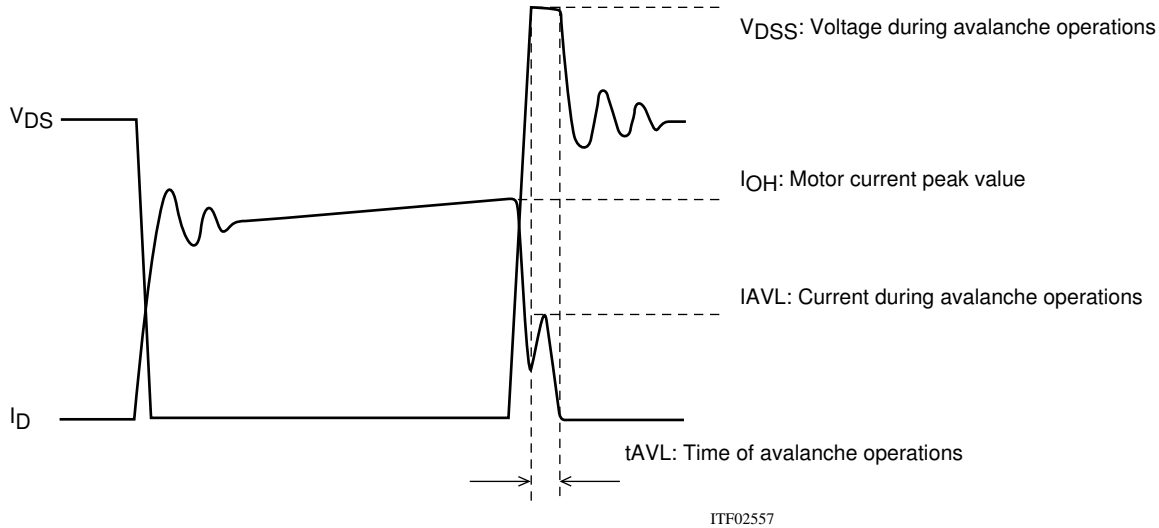


Figure 1 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-400 Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-400 Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (4-1).

$$EAVL1=V_{DSS}\times IAVL\times 0.5\times tAVL \quad \text{---------- (4-1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (4-1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-400 Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (4-2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (4-1).

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \quad \text{---------- (4-2)}$$

fc: Hz units (fc is set to the PWM frequency of 62.5kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-400 Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=0.8A, tAVL=0.2µs when using a STK672-410 driver, the result is:

$PAVL=110\times 0.8\times 0.5\times 0.2\times 10^{-6}\times 62.5\times 10^{3}=0.55W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (4-2) falls within the allowable range for avalanche operations.

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.
- Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

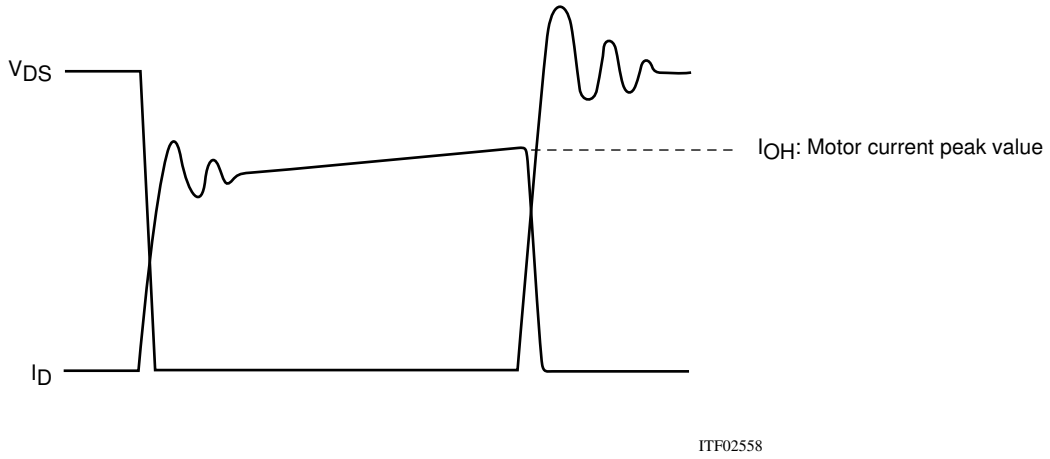
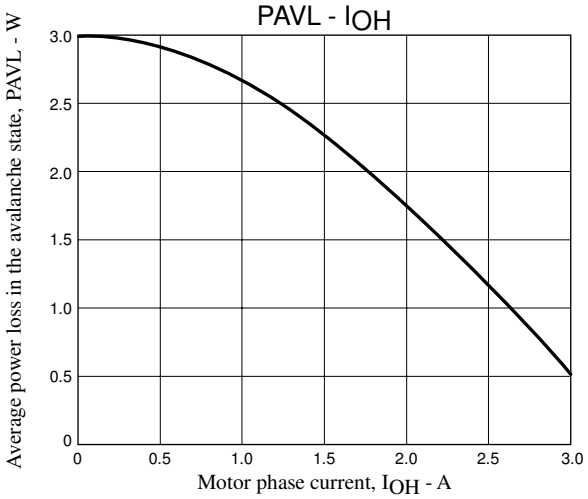


Figure 2 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-400 when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 3 Allowable Loss Range, PAVL-I_{OH} During STK672-410 Avalanche Operations



Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 3W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

Consider using these devices in the usage ranges for an operating substrate temperature Tc of 105°C.

5. STK672-410 Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to "Calculating Internal HIC Loss for the STK672-410" in the specification document.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations.

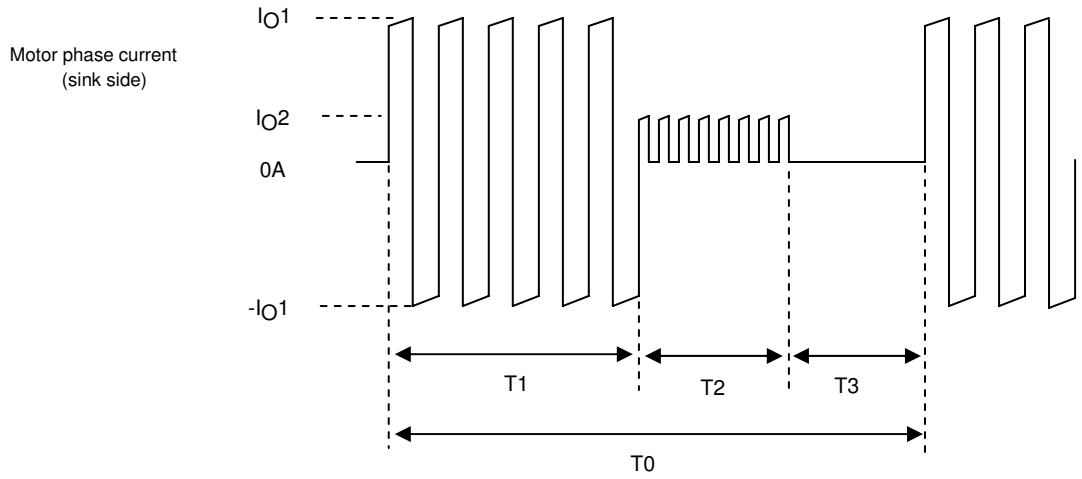


Figure 1 Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
I_O1 and I_O2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.
The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

PdAV= (T1×P1+T2×P2+T3×0) ÷TO ---------- (I)

(Here, P1 is the PdAV for I_O1 and P2 is the PdAV for I_O2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

θc-a= (Tc max-Ta) ÷PdAV ---------- (II)

Tc max: Maximum operating substrate temperature =105°C

Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (4-2), "Allowable STK672-400 Avalanche Energy Value", to PdAV.

Figure 2 Substrate temperature rise, ΔTc - Internal average power dissipation, PdAV

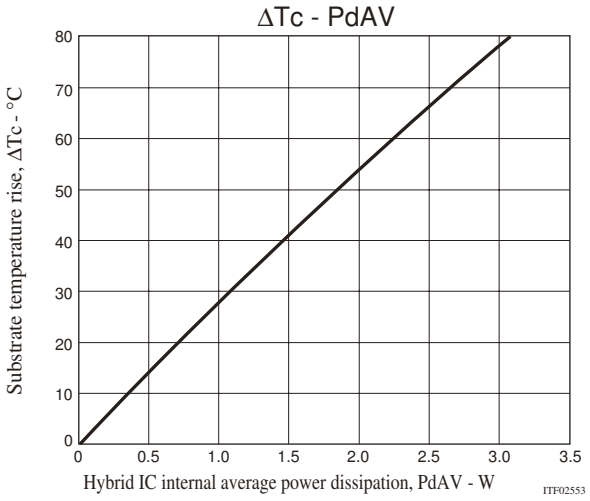
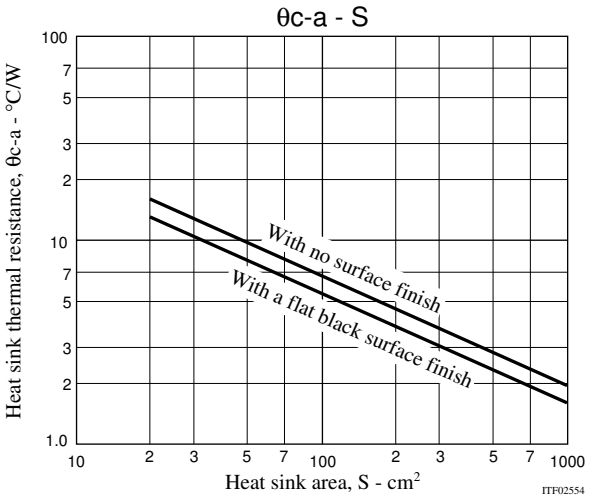


Figure 3 Heat sink area (thickness: 2mm) - θc-a



6. STK672-400 and 410 Ambient Temperature Ta Package Power Loss PdPK Derating Curve

The package power loss PdPK is the internal average power loss PdAV that is allowed without a heat sink. The figure below shows the power loss PdPK that is allowable as the ambient temperature Ta changes.
At Ta=25°C a power loss of 3.1W is allowable, and at Ta=60°C, 1.75W is allowable.

STK672-400 and 410 package power loss PdPK (no heat sink) - Ambient temperature Ta