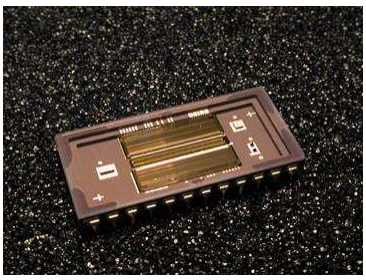


PDA-640-SFF
Small Form Factor 640 Pixel, InGaAs Photodetector Sensor with High Speed Readout

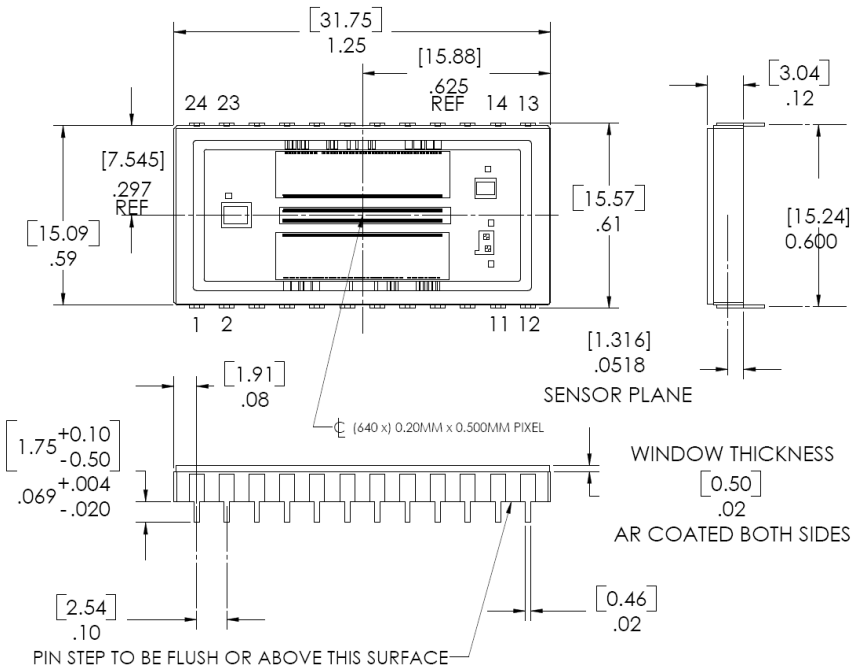
The Princeton Lightwave 640 pixel detector consists of an InGaAs photodetector array hybridized with a high speed, low noise readout circuit. The hybridized array is mounted on low profile ceramic leaded package, with an optical window. Optically black pixels are provided for real-time dark voltage offset correction. This device is ideal for low noise spectroscopy in industrial sensing, telecommunication and defense applications. It is qualified to t Telcordia 468 CORE.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Typ.	Max.
VDD / Analog supply voltage		4.75	5.0	5.25
Operating temperature range	deg C	-20	25	70
Storage temperature range	deg C	-40		85

Mechanical Layout

(Dimensions are in [mm] / inches)



Pin Designations

Pin	Signal	Pin	Signal
1	VDD_D	24	N.C.
2	VDD_A	23	RESET
3	VSS_D	22	C_{INT} SELECT
4	VSS_A	21	VSS_A
5	Even Vid1	20	Odd Video 2
6	Even Vid2	19	Odd Video 1
7	VSS_A	18	V_{REF}
8	Case Gnd (VSS_D)	17	V_{PDA}SET
9	Integrate	16	VSS_A
10	Clock	15	BW
11	Anti-bloom	14	R_{THERM2}
12	N.C.	13	R_{THERM1}

Sensor Performance

Specifications at VDD=5.00, VSS=0V, T_{CHIP}=25°C, unless otherwise indicated.					
Parameter	**Units**	**Condition**	**Min**	**Typ**	**Max**
Active Pixels	pixels	-		640	
Pixel Dimensions – Pitch and Height	um x um			20 x 500	
Optically Black Pixels - note 1	pixels	-		16	
Inoperable Active Pixels	pixels	-			0
Peak Wavelength	nm	-		1550	
Quantum Efficiency	%	1100-1700 nm		70	
Responsivity	nV/photon	C_{INT} =HIGH C_{INT} =LOW	10 75	12 90	14 105
PRNU	%	80% V_{SAT}		±5	±10
Linearity	%	20-80% V_{SAT}, T_{INT}=50mS			5
VDD	V		4.75	5.00	5.25
IDD	mA			85	120
VSS	V			0	
R_{THERM}	ohms		4900	5000	5100
VRef	V		3.15	3.25	3.35
Clock					
HIGH	V			VDD	
LOW	V			VSS	
Frequency	MHz		0.01		5.00
Duty Cycle	%		45	50	55
Integrate					
HIGH	V			VDD	
LOW	V			VSS	
WIDTH			10 Clocks or 20 usec.		
C_{INT} Select					
HIGH (High Dynamic Range)	V			VDD	
LOW (High Sensitivity)	V			VSS	
Full Well Capacity					
C_{INT}=LOW	pC e-			3.19 2.00 X 10^7	
C_{INT}=HIGH (default)	pC e-			24 1.50 X 10^8	
Gain					
C_{INT}=LOW	nV/e-		105	120	135
C_{INT}=HIGH	nV/e-		14.0	16.0	18.0
V_{SAT}	V		2.0	2.4	2.8
Dark Rate	V/Sec			0.3	1.9
Readout Noise					
C_{INT}=LOW	e-/rt-scan			1000	1600
Dynamic Range	dB	F_{CLK} = 250KHz	41	43	
C_{INT}=HIGH	e-/rt-scan	BW Select = LOW		3800	6000
Dynamic Range	dB		44	46	
Crosstalk	dB				-30
Video Output					
Impedance	ohms				2000
Settling time (to 16-bits)	ns				100
Pixel Rate - note 2	MP/S		0.1		10

Note 1: Dark pixels are optically opaque pixels provided for real-time dark offset correction.

Note 2: Maximum rate of 5MPS per video output, 2 interleaved video outputs, (10MPS total).

Signal Descriptions

Pin	Type	I/O	Signal	Description
1, 2	Power	Power	V_{DD}	Device power supply, +5.0V nominal. Bypass capacitors of 0.1uF and 10uF close to the package pins are recommended for optimum noise performance.
3,4,7,16,21	Power	Power	V_{SS}	Device power supply return.
5	analog	O	Even Video1	Even pixel zero video reference level. May be used for differential subtraction of video offset level. Signal is typically 3.25V
6	analog	O	Even Video2	Even pixel video signal. Pixel video levels are updated on the clock falling edge. Dark signal is approximately 3.25V, saturated signal is approximately 1.25V
8	Power	Gnd	Case GND	May be connected to power supply ground in the user's application
9	digital	I	Integrate	Integration and readout control. Integration begins 5.5 clock cycles after the rising edge and ends 3.5 clock cycles after the falling edge. (Integration time=T_{INT}-2 Clk). Active pixel video readout begins with pixel #1, 12 clock cycles after the falling edge. Minimum high time is the greater of 20us or 10 clocks.
10	digital	I	Clock	Pixel readout clock
11	digital	I	Antibloom	Antibloom Enable - active high. Internal pull-down for disabled state if left unconnected.
13	analog	passive	R_{THERM1}	5Kohm thermistor connection
14	analog	passive	R_{THERM2}	5Kohm thermistor connection
15	digital	I	BW Select	CTIA Bandwidth Select. Internal pull-down. For best noise performance with pixel clocks of <1MHz, this pin should be tied low or left unconnected. For pixel clocks above 1MHz, this pin should be tied high for faster video settling time.
17			V_{PDA}SET	Controls reverse bias to the InGaAs photodiode array. No connection required for 0V bias, may be bypassed with 0.1µF to ground for lowest noise performance. 3.25V nominal (0V Bias), More positive drive voltage causes negative PDA bias.
18	analog	O	V_{REF}	Video reference level, typically 3.25V. May be bypassed externally with 0.1uF for improved noise performance.
19	analog	O	Odd Video 1	Odd pixel zero video reference level. May be used for differential subtraction of video offset level. Signal is typically 3.25V
20	analog	O	Odd Video 2	Odd pixel video signal. Pixel video levels are updated on the clock rising edge. Dark signal is approximately 3.25V, saturated signal is approximately 1.25V
22	digital	I	C_{INT} Select	Integration capacitor select - Internal pull-up for high dynamic range mode (10pF Cint) if left unconnected.
23	digital	I	Reset	Device reset - active low. Device contains a 0.1µF reset capacitor to ground and a 70µA pull-up current to provide power-on reset function (Reset for ~5ms at power-on). Pin may be left unconnected, or driven low by the user for device reset.
12, 24		-	no connection	Pins should be left unconnected.

1. Principles of Operation

The PLI 640 linear array contains an InGaAs photodiode array with 640 “active” pixels on a 20um pitch and 16 “dark” pixels available for user dark offset correction. The CMOS read-out integrated circuit architecture consists of capacitive transimpedance amplifiers (CTIA), in which the photocurrent is buffered, amplified and stored, and a video multiplexer for read-out of the integrated charge values. The CTIA architecture is illustrated in Figure 1.

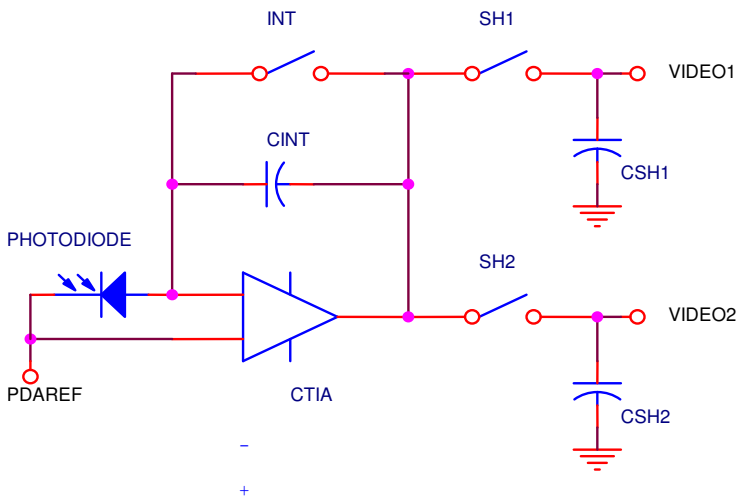


Figure 1. PLI 640 array pixel integration architecture.
PDAREF and control signals for INT, SH1, and SH2 are generated internally.

Within each read-out pixel is a CTIA with the photodiode at the input. During the integration period, the photocurrent is integrated on the feedback capacitor CINT. Two values of feedback capacitor are available, (1.33pF and 10.0pF), and can be selected externally

Nominally, there is a –5mV bias across the photodiodes. Referring to Figure 1, the level of this bias is set at PDAREF. PDAREF is generated internally as a fixed offset to the VREF potential. VREF is nominal fixed at 3.25 V by a built-in bandgap reference. The actual bias across the photodiode can vary ±5 mV from the 5mV nominal set-point. Each pixel will exhibit a dark current of; Idark = (VPDAREF-VREF)/Ro; (the pixel's bias divided by that pixel's shunt resistance). Photodiode dark current appears as a fixed pattern noise (FPN) that deviates both positively and negatively from the zero signal level ($\mathbf{V_{REF}}$).

There are two sample-and-hold circuits at the output of the each pixel's CTIA. This allows the array to operate in a parallel-in, serial-out "snapshot" mode. Between exposures, all of the pixels are held in reset (CINT discharged), then released so that the "zero" levels can be captured with the first sample-and-hold capacitors (CSH1). Following the integration time, the total charge levels are captured with the second sample-and-hold capacitors (CSH2). The pixels are then read out sequentially through a video multiplexer stage. Both the initial signal (**Video 1**) and the final signal (**Video 2**) will deviate from $\mathbf{V_{REF}}$ with bipolar dark current and negative-going photocurrent.

In a typical application, **Video 1** and **Video 2** can be differentially amplified as a form of external correlated double-sampling. This technique eliminates much of the multiplexer related switching noise.

The Integrate/Read-Out sequence is shown in Figure 2.

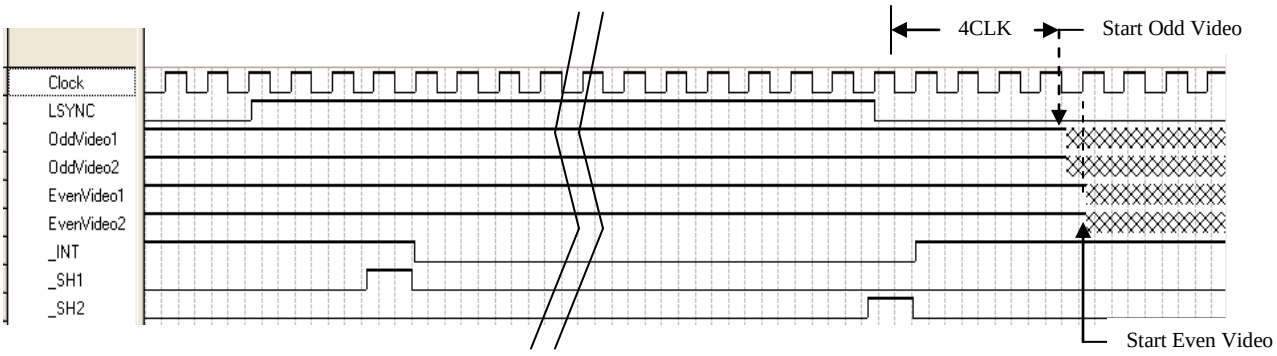


Figure 2. PLI 640 Array Integrate/Read-Out sequence
Clock & Integrate and are provided by the user. _INT, _SH1, and _SH2 are generated internally.

- While waiting for a line sequence to be initiated, the CTIA feedback capacitors are held in reset. Upon assertion (the rising edge of **Integrate**), the following events occur:

  1. The INT switch is opened, which allows charge to accumulate.
  2. SH1 is activated to sample the signal at the beginning of charge integration.
  3. Charge continues to integrate on the feedback capacitor.

- When the line sequence is terminated (on the falling edge of **Integrate**), the following events occur:

  1. SH2 is activated to sample the signal at the end of charge integration.
  2. The INT switch is closed, draining charge from the feedback capacitors.
  3. The shift registers begin operation so that the pixel-by-pixel pre-integration and post-integration charge signals appear at **Video 1** and **Video 2** serially.

All of the above functions are generated internally.
The user need only provide a continuous master clock (**Odd Clock**/**Even Clock**) and a line-trigger/integrate pulse (**Integrate**).

2.0 Operating the PLI 640 Array

2.1 General Considerations

1. Power Supply: 5.0VDC ±5%

2. Power Supply Decoupling: It is recommended to decouple the power supply using 0.1uF and 10uF capacitors in parallel, mounted close to the $\mathbf{V_{DD}}$ and $\mathbf{V_{SS}}$ pins.

3. V_{REF} is an internally generated bias. It may be bypassed using a 0.1uF capacitor to signal ground for best noise performance.

4. Reset contains a 0.1uF reset capacitor with a weak pull-up to provide automatic power-on reset function. Nominal power-on reset time is 5ms. The pin may be driven externally to force a reset or alter power-on reset timing.

3. Timing is derived from a continuous master clock (**Odd Clock**/**Even Clock**). A single control line (**Integrate**) is used to initiate the integration, end the integration, and initiate the serial video readout.

4. To avoid transients at the start of video readout, the output amplifiers are clamped to the **V_{REF}** potential when the video readout circuitry is inactive. This reference potential is approximately 3.25 V, and represents the true zero signal level.

5. Observe video setup and hold times (t_{VS}, t_{VH}) to ensure the acquisition video sampling point has allowed the signal to settle to full accuracy.

6. The default integration capacitance is 10.0 pF which is the high dynamic range mode. If **C_{INT} Select** is tied LOW, the integration capacitance is 1.33 pF, which is the high sensitivity mode.

2.2 Pixel Configuration

1. Odd Video 1 & 2 outputs are updated on each Odd Clock falling edge.

2. Even Video 1 & 2 outputs are updated on each Even Clock rising edge.

3. Even Clock and Odd Clock are normally tied together.

4. Video read-out is initiated by the rising edge of the Integrate signal (end of integration).

5. “Active” Pixels: 640 active pixels on 20um pitch, (12.8mm line width). Video information is inverted, where a signal level about 3.25V represents the dark level and about 1.25V represents full scale brightness.

6. “Dark” Pixels: 16 dark pixels are provided, 8 on each side of the active array. Dark pixels are integrated with all active pixels and appear in every line read-out. Dark pixels may be used for systematic dark offset correction.

7. “Buffer” Pixels: 14 buffer pixels between active and dark pixels. Buffer pixels provide an optical margin between the active pixels and dark pixels. Video output values of buffer pixels are indeterminate.

Pixel Sequence of Video Outputs

Assumes common **Even Clock** and **Odd Clock**.
Pixel positions are in reference to the falling edge of Integrate (End of Integration)

	|---> Start of Dark Pixels								**|---> Start of Buffer Pixels**						**|---> Start of Active Pixels**					
Channel	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E
Type	DRK1	DRK2	DRK3	DRK4	DRK5	DRK6	DRK7	DRK8	BUF1	BUF2	BUF3	BUF4	BUF5	BUF6	1/640	2/640	3/640	4/640	5/640	6/640
Clock	4F	5R	5F	6R	6F	7R	7F	8R	8F	9R	9F	10R	10F	11R	11F	12R	12F	13R	13F	14R

Clock numbers are in reference to falling edge of of L_{SYNC} and indicate the clock edge on which the pixel value is updated in the video stream

- 1st Dark Pixel appears on the odd channel at the 4th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.
- 1st Buffer Pixel appears on the odd channel at the 8th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.
- 1st Active Pixel appears on the odd channel at the 11th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.

	End of Active Pixels--->|								**End of Buffer Pixels--->|**										**End of Dark Pixels--->|**	
Channel	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E
Type	637/640	638/640	639/640	640/640	BUF7	BUF8	BUF9	BUF10	BUF11	BUF12	BUF13	BUF14	DRK9	DRK10	DRK11	DRK12	DRK13	DRK14	DRK15	DRK16
Clock	329F	330R	330F	331R	331F	332R	332F	333R	333F	334R	334F	335R	335F	336R	336F	337R	337F	338R	338F	339R

- Last Dark Pixel appears on the even channel at the 331st rising edge of **Even Clock** after the falling edge of L_{SYNC}.
- Last Buffer Pixel appears on the even channel at the 335th rising edge of **Even Clock** after the falling edge of L_{SYNC}.
- Last Active Pixel appears on the even channel at the 339th rising edge of **Even Clock** after the falling edge of L_{SYNC}.

2.3 Timing

The only control signals required to operate the ROIC are a continuous master clock (CLK) and an exposure time signal (Integrate).

1. **Odd Clock** and **Even Clock** pins are normally tied together.

2. **Clock** should run continuously to allow internal timing functions to occur. If the clock has not been run for an extended duration, or power has been recently applied, the device should be run through an integration/read-out cycle to completely reset the device.

3. The clock frequency should not exceed 5 MHz. Odd pixels are read-out at the falling edges of **Odd Clock**, and even pixels are read-out on the rising edges of **Even Clock**. (Two pixels are delivered every clock period, for a maximum composite readout rate of 10 million pixels per second.

4. **Integrate** should rise and fall on the rising edge of the clock. The minimum duration of **Integrate** high time is 10 clock cycles or 20 µs; whichever is longer. The actual integrated exposure time is three clock cycles less than the total duration of **Integrate** high period.

5. Active pixel #1 video levels will appear at the **Odd Video 1 & 2** pins beginning at the 11th falling edge of **Odd Clock** after the falling edge of **Integrate**.
   Active pixel #2 video levels will appear at the **Even Video 1 & 2** pins beginning at the 11th rising edge of **Even Clock** after the falling edge of **Integrate**.

6. The next exposure can begin anytime after the readout of the previous exposure is complete. (The minimum duration of **Integrate** LOW between integrations is 340 CLK cycles to ensure complete read-out of the previous integration line).

7. **Video1** and **Video2** outputs are clamped to $\mathbf{V_{REF}}$ level between active readout periods.

2.3.1 Clock and Integrate Timing

The Clock and **Integrate** timing requirements are shown in Figure 3:

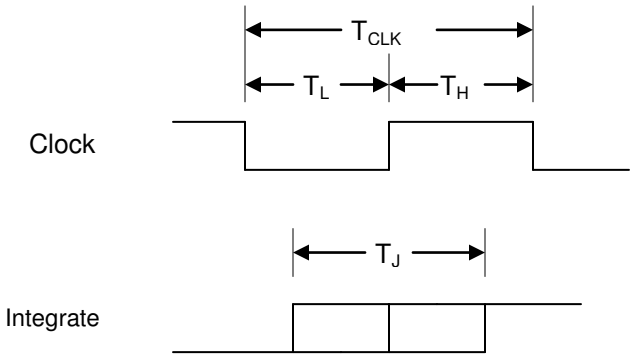


Figure 3. Timing relationships for Integrate and CLK.

1. T_{CLK} is the master clock period. It must be at least 200ns long (maximum clock freq is 5 MHz) and no longer than 100us (minimum clock freq is 10 kHz).

2. CLK will typically have a 50% duty cycle, however, what is explicitly required is that both T_H (the high half period) and T_L (the low half period) be a minimum of 90 ns.

3. Both the rising and falling edges of **Integrate** should occur on the rising edge of the clock. The allowable **Integrate** edge jitter (T_J) is $\pm T_{CLK}/3$.

2.3.2 Video Timing

The timing of the pixel video output is summarized in Figure 4:

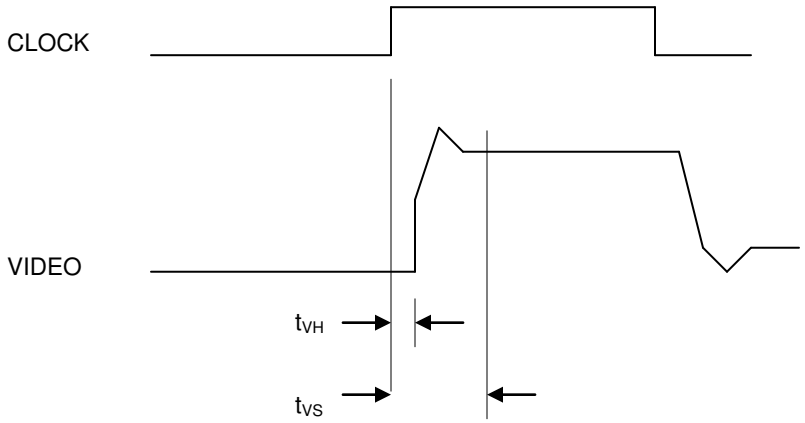


Figure 4. Pixel video timing

1. Video Hold Time: (t_{VH}): The minimum time between detection of a clock edge and the beginning of the transition to the next pixels video level. It is less than 50 ns.

2. Video Setup Time (t_{VS}): The maximum time required after detection of a clock edge until the video signal is sufficiently settled so that it can be digitized with 16 bit precision. It is less than 100 ns.

2.4 Thermistor

The sensor module incorporates a thermistor for monitoring the temperature of the photodiode array and electronics.

Thermistor: Negative temperature coefficient (NTC) type with a nominal value of 5Kohms at 25°C.
Thermal Coefficients: Alpha = -4.39%, Beta = 3892±1.0%
Steinhart-Hart Coefficients: $A=1.28745 \times 10^{-3}$, $B=2.357394 \times 10^{-4}$, $C=9.5052 \times 10^{-8}$

PRODUCT HANDLING NOTES

Semiconductor devices are sensitive to electrostatic discharge (ESD) and should be handled with appropriate caution, including the use of ESD protective equipment such as grounding straps and anti-static mats.