

1 FEATURES

- Horizontal or vertical mounting
- High reliability and robustness over long lifetime
- Low vibration sensitivity
- High overload and shock capability (5000 g)
- Butterfly balanced design for high mechanical common mode rejection
- Closed-loop force feedback operation with electrostatic frequency tuning
- Low bias drift
- Ideal mono crystalline Si material
- Wafer level sealing with controlled Q-factor
- Low power
- Single supply +5 VDC
- Fully digital with SPI communication and on chip OTP calibration
- Digitally controlled sample rate up to 2000 SPS
- Bandwidth defined by built in 4th order digital LP filter
- Intrinsic continuous diagnostic monitoring
- Temperature sensor
- No external components required



2 GENERAL DESCRIPTION

The SAR100 consists of a ButterflyGyro™ MEMS die and a BiCMOS ASIC housed in a rigid custom ceramic LCC package to accommodate dual axis surface mounting. The function is based on the excitation of a reference motion in the butterfly structure. An angular rotation of the device will generate Coriolis forces, whose frequency equals that of the reference motion and whose resulting vibration amplitude is a measure for the angular rotation. By utilizing Sensoror Technologies' unique patented sealed cavity technology, the vibrating masses are contained within the low-pressure hermetic environment needed for creating low dynamic damping and high Q factors, without any degradation over the lifetime of the device.

The gyro die is built as a triple stack consisting of a bottom glass die with metalized patterns defining excitation and detection electrodes, a middle micro machined mono crystalline silicon die with the oscillating masses, which also represent a common opposite electrode, and a third top cap glass die. A time multiplexed, switched interface is used between the gyro die and the ASIC. This makes it possible to improve the symmetry by using the same electrodes for drive interface and sense interface. By the symmetric mechanical design and by connecting the electrodes cross-wise symmetric, the "butterfly" masses are operating in a balanced anti-phase movement. The balanced operation of both the excitation mode and the detection mode makes SAR100 almost insensitive to environmental vibrations, limiting effects causing bias drift as well as improves the Q-factors. A fine-tuning of the oscillation frequencies, to allow for force-feedback operation, is done during final test for each sensor by applying and programming an electrostatic bias to reduce the mechanical stiffness and thereby calibrate the detection mode frequency. Fixed algorithms use individually determined calibration coefficients stored in OTPROM poly fuse cells. Readings from the internal temperature sensor are used for accurate angular rate definitions. An SPI interface enables communication between application and SAR100.

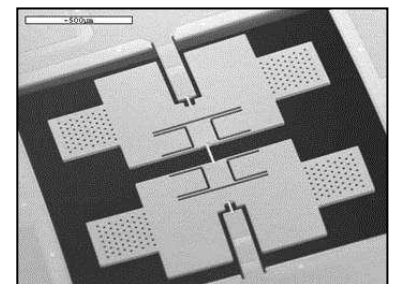


Figure 1-1: SAR100 element structure

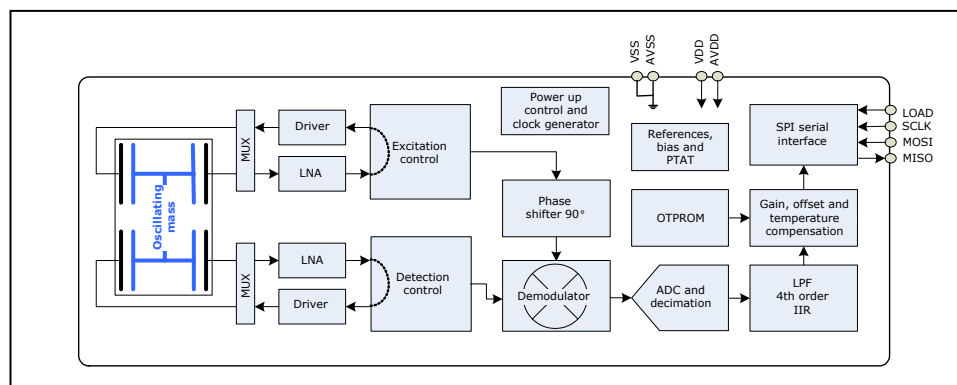


Figure 2-1: SAR100 block diagram

The angular rate data output is in a 12-bit 2's complement format. A number of functions are available through the digital SPI interface.

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4 ABBREVIATIONS AND DEFINITIONS

4.1 Abbreviations

FSI	Full Scale Input
FSO	Full Scale Output
SPI	Serial Peripheral Interface
ASIC	Application Specific Integrated Circuit
ESD	Electro Static Discharge
MSB	Most Significant Bit
LSB	Least Significant Bit
OTPROM	One-Time Programmable Read Only Memory

4.2 Definitions

- Specifications herein are over the complete temperature and supply voltage operating range unless otherwise is noted
- Voltages are referenced to AVSS/VSS unless otherwise is specified

5 RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Input range	Ω FSI			±400		°/s
	Ω FSI			±250		°/s
	Ω FSI			±100		°/s
Dynamic overload, angular rate	Ω OVL	1,5	±1200	±5000		°/s
Dynamic overload, shock		1,4,5	±500	±1500		g
Recovery time dynamic overload		1,5		30		ms
Supply voltage	VDD, AVDD	2	4.45	5.0	5.5	VDC
Current consumption		3			17	mA
Sensor oscillation frequency	fOSC			9.4		kHz
Internal master clock	fMCLK			8.0		MHz
Operating temperature	TOPER		-40		+90	°C

Note 1: The PRCEN command will have to be issued to revert to normal functionality.

Note 2: Both digital (V_{DD}) and analog (AV_{DD}) supply voltage.

Note 3: Total current consumption from both analog and digital supply.

Note 4: Shock below 500g/1ms will never result in an error condition.

Note 5: By design.

6 ABSOLUTE MAXIMUM RATINGS

Prolonged exposure to absolute maximum ratings may affect the performance and/or reliability of the device.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Supply voltage	VDD, AVDD		-0.5		7.0	VDC
Input voltage, any pin			-0.5		VDD +0.5	VDC
Input transient current, any pin					±100	mA
Short circuit immunity to VDD/AVDD or VSS/AVSS, any output					10	Min
ESD voltage immunity, Human Body Model, any pin		1			2000	V
ESD voltage immunity, Charge Device Model, any pin		2			500	V
Mechanical shock		3			5000	G
Ambient temperature when operating			-40		+125	°C
Storage temperature			-55		+125	°C

Note 1: According to AEC-Q100-002 Rev. C or JESD22-A114 Rev. F.

Note 2: According to AEC-Q100-011 Rev. B or JESD22-C101 Rev. D.

Note 3: According to MIL-STD 883E.

7 SPI SERIAL DATA INTERFACE

Serial data communication with the application is through the SPI interface. The 8 MSBs of an angular rate data sample are mapped to the 8 bit response of the RARH (read angular rate high byte) command. The 4 LSBs of the sample are mapped to the 4 LSBs of the 8 bit response of the RARLX (read angular rate low byte) command. The RARH command latches the 4 LSBs of a sample such that a RARH, RARLX command sequence guarantees bits from the same angular rate sample. The 4 MSBs of the response from the RARLX command is always a '0101' SPI error check bit pattern.

7.1 Signal Definitions and Characteristics

The SPI interface consists of the 4 signals MOSI, MISO, SCLK and LOAD.

Name	Signal Description
MOSI	Master Out, Slave In. After a negative edge on LOAD, 8-bit command is shifted in on MOSI, clocked by SCLK (MSB first).
MISO	Master In, Slave Out. Output from previous command is stored in a Data Register. At a negative edge on LOAD, the content of the Data Register is loaded to the Data Output Register. While command byte is shifted into the Command Register, Data Output is shifted out on MISO (MSB first).
LOAD	Chip Select/Transfer Start Strobe. As long as LOAD=1, the MISO output is in a high-Z mode (tri-stated). A negative edge on LOAD initiates an SPI transfer. The new command is executed after a positive edge on LOAD. If a positive edge occurs on LOAD before at least 8 bits are shifted in on MOSI, the command will be ignored.
SCLK	Serial Data Clock. MOSI is read on the positive edge of SCLK, and MISO is shifted out on the negative edge of SCLK.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
High ('1') level	VH	2	0.7VDD			V
Low ('0') level	VL	2			0.3VDD	V
Input rise time	trI	2			1/(20fSCLK)	s
Input fall time	tfl	2			1/(20fSCLK)	s
Output fall time	tPHL	1,2			8.5	ns
Output rise time	tPLH	1,2			8.6	ns
Output enable delay	tPHZ tPLZ tPZH tPZL	1,2			1.2 0.97 8.4 8.2	ns
Data rate	fSCLK	3			8.5	Mbits/s
Capacitive load, MISO	CMISO	2			100	pF

- Note 1:** With load of 100pF connected to V_{SS}.
Note 2: Characteristic is based on proven library I/O cell performance.
Note 3: By design.

7.2 SPI Commands

Name	Command	Address	Output	Description	Note
Read Commands					
RARH	10000000	-	dddd dddd	Read angular rate, high byte	2
RARLX	10001110	-	0101 dddd	Read angular rate, low byte extended	
RTMP	10110000	-	dddd dddd	Read internal temperature	
RSR	10110100	-	Status byte	Read status register	
SafeGuard Commands					
SGDIS1	01001110	11010111	1000 0000	SafeGuard disable command 1	1
SGDIS2	01100011	01010000	1000 0000	SafeGuard disable command 2	
SGDIS3	00010010	10101000	1000 0000	SafeGuard disable command 3	
SGEN	01010101	-	0000 0000	SafeGuard enable command	
Error Handling Commands					
PRCEN	10101010	-	1000 0000	Re-enable signal processing after error condition	3

- Note 1:** The three SafeGuard disable commands MUST be issued in the -1,-2,-3 sequence, and with the addresses shown. Any in-between commands or incorrect addresses will reset the SafeGuard disable sequence. A single SGEN command re-enables the SafeGuard.
Note 2: The RARH command latches high and low bytes such that a sequence of RARH first followed by RARLX guarantees bits from the same Angular rate sample.
Note 3: In case of a recoverable error condition, issuing this command re-enables continued angular rate readout. Note that for this command to function the SafeGuard must be disabled. See also chapter 8 for details.

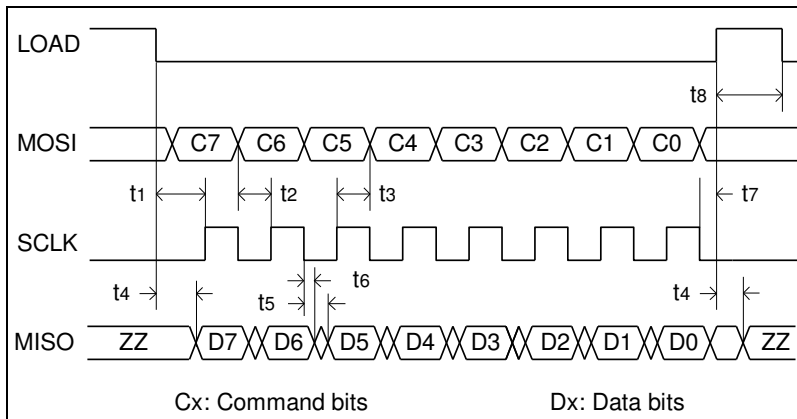


Figure 7-1: SPI interface signal timing diagram

For commands that need an address, the address byte is shifted in prior to the command byte.

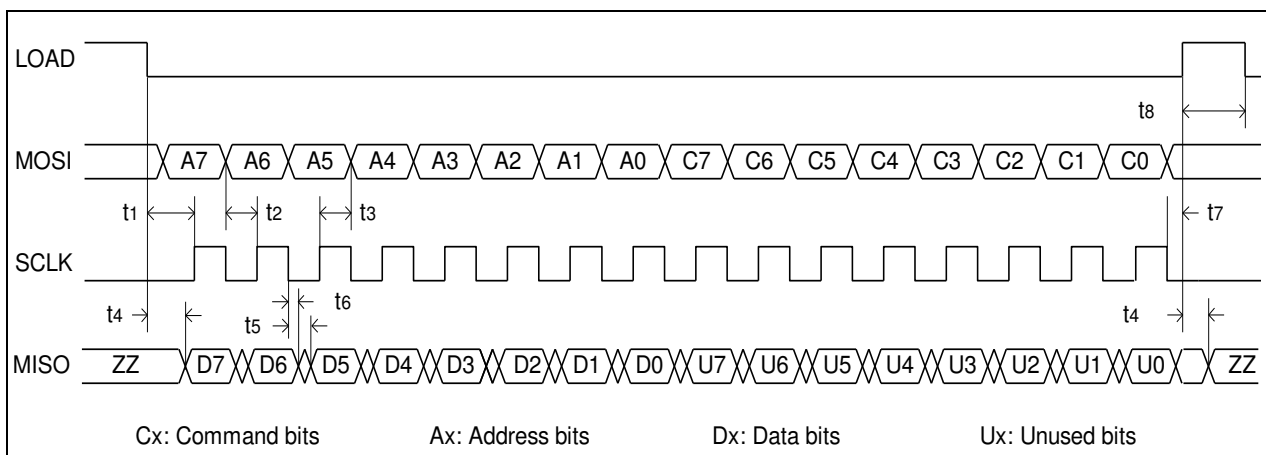


Figure 7-2: SPI interface signal timing diagram for command with address byte

Symbol	Parameter	Specification			Note
		Min	Max	Units	
t1	Delay from falling edge of LOAD to the first rising edge of SCLK	10		ns	2
t2	Delay from stable data at MOSI to rising edge of SCLK (MOSI data setup time)	10		ns	2
t3	Delay from rising edge of SCLK to new data at MOSI (MOSI data hold time)	10		ns	2
t4	Delay from falling edge or rising edge of LOAD to active or high-Z state of MISO		20	ns	2
t5	Delay from falling edge of SCLK to stable new data at MISO (MISO data output delay)		20	ns	2
t6	Delay from falling edge of SCLK to removal of old data at MISO (MISO data hold time)	0		ns	2
t7	Delay from last falling edge of SCLK to next rising edge of LOAD	20		ns	2
t8	Delay from rising edge of LOAD to falling edge of LOAD	527		ns	1,2

Note 1: Minimum 4 internal MCLK cycles = $4 * 1/7.6\text{MHz}$.

Note 2: By design.

7.3 Error Code

The Error Code is a bit pattern defined as 1000 0000₂. This Error Code is the SPI response during device startup, if an illegal or undefined SPI command is attempted executed, or if a RARH or RARLX command was executed while at the same time any one or more of the Status Register flags is a '0'. The RARH command accesses the 8 MSBs of the 12 bit 2's complement rate data. Negative angular rate data is limited (clamped) to -2032 (binary 1000 0001 0000₂) since the 8 MSBs of rate data in the range -2048 to -2033 (1000 0000 0000₂ to 1000 0000 1111₂) could otherwise be confused with the Error Code. For symmetry reasons positive angular rate data is likewise limited to 2032. Note that this angular rate data limiting does not affect any Status Register flags.

8 ANGULAR RATE AND TEMPERATURE OUTPUT

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Angular rate data format						
Word length			12			bit
Format			2's complement			
SPI commands			RARH RARLX			
Scale factor				0.25 0.25 0.10		(%/s)/LSB (%/s)/LSB (%/s)/LSB
Full scale signal	+ Ω FSO - Ω FSO	1	High byte 00111110 11000001	Low byte 01011000 01011000		
Zero rate output			High byte 00000000	Low byte 01010000		
Error Code			High byte 10000000	Low byte 10000000		
Sensitivity		10				
Accuracy		1,7		±1		%
Shift over temperature		8		±0.5		%
Non-linearity				0.1		%FSO
Noise						
Noise				0.25 0.25 0.15		°/s (rms) °/s (rms) °/s (rms)
Rate noise density				0.03 0.03 0.02		°/s/√Hz °/s/√Hz °/s/√Hz
Bias		10				
Initial bias		7	-400	0	+400	LSB
In-run bias stability		7,9		0.02		°/s
Bias temperature accuracy		8		±0.5		°/s
Linear acceleration effect		5			±0.05	(°/s)/g
Alignment error				±1		°
Frequency response		4				
Filter sampling rate	fS			2		kHz
Pass band ripple		4,6			0.2	dB
Group delay		6			13	ms
Passband cut-off frequency	fH	3,6		50		Hz
Roll-off for f > fH		6		100		dB/dec
Attenuation for f > 310 Hz		6		85		dB

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Temperature sensor		10				
Word length			8			bit
Format			2's complement			
SPI commands			RTMP			
Scale Factor				1		°C/LSB
Full scale signal	Tmax Tmin	7	01011111 11011000		+95°C -40°C	
Accuracy		8		±2		°C

- Note 1:** Calibrated at $f_0 = 2\text{Hz}$.
Note 2: Integrated over $\Delta f = fH$.
Note 3: -3dB frequency.
Note 4:

$$\text{LP-filter transfer function: } H(z) = \frac{b_{01} + b_{11} \cdot z^{-1} + b_{21} \cdot z^{-2}}{1 - a_{11} \cdot z^{-1} - a_{21} \cdot z^{-2}} \cdot \frac{b_{02} + b_{12} \cdot z^{-1} + b_{22} \cdot z^{-2}}{1 - a_{12} \cdot z^{-1} - a_{22} \cdot z^{-2}}$$

a11	1.91064453125E+00	a12	1.829833984375E+00
a21	-9.31640625E-01	a22	-8.40087890625E-01
b01	1.0498046875E-02	b02	7.8125E-03
b11	-1.0498046875E-02	b12	4.8828125E-03
b21	1.0498046875E-02	b22	7.8125E-03

- Note 5:** For any axis. Frequencies < 5.4 [kHz]. Stationary vibrations at resonant modes at frequencies > 5.4 [kHz] may cause larger effects.
Note 6: By design.
Note 7: At 25 °C.
Note 8: At 5.0 VDC. Within -30 to +70 °C.
Note 9: By Allan Variance method.
Note 10: Maximum temperature gradient ±5K/min.

9 POWER SUPPLY AND START-UP

The SAR100 is designed for a single +5 volt supply. The device has four pins for power connection: V_{DD} , AV_{DD} , V_{SS} and AV_{SS} . The V_{DD} (pin 16/T14) and AV_{DD} (pin 14/T16) should be connected together on the printed circuit board as close as possible to the device. The same rule applies to V_{SS} (pin 28) and AV_{SS} (pin 2). A simultaneous power-on of the two supplies is essential to prevent internal latch-up conditions.

An external decoupling capacitor is needed for the power supply. This should be a low ESR 100nF capacitor connected on the printed circuit board as close as possible to the V_{DD} and V_{SS} pins. The same rule applies for a decoupling capacitor between REFV (pin 4) and V_{SS} . This should be a low ESR 10nF capacitor.

The SAR100 has a supply voltage surveillance circuit which sets the Status Register flag PRNG_OK to '1' only if AV_{DD} is within specified range. If outside this range, the PRNG_OK flag is set to '0'.

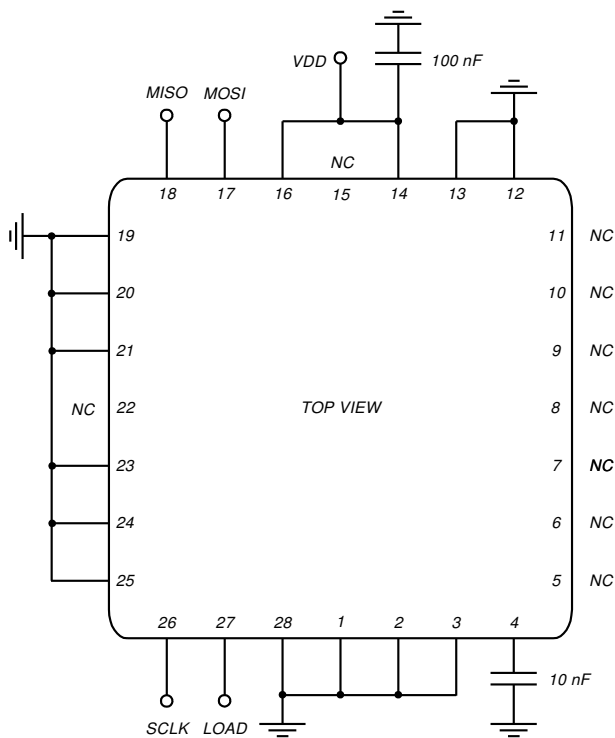


Figure 9-1 SAR100 electrical connections (horizontal mount)

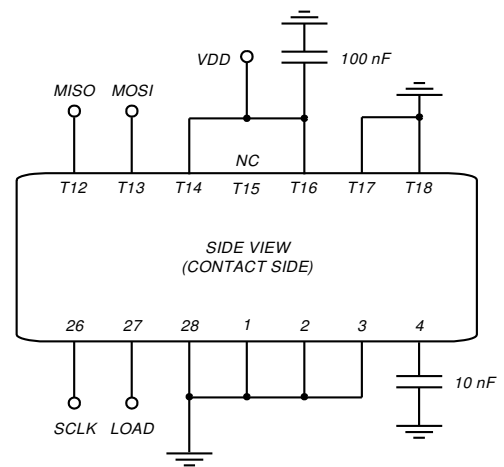


Figure 9-2 SAR100 electrical connections (vertical mount)

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Supply voltage rise time to VDD-MIN	tD	1	0.001		10	ms
Start-up time	tINIT	2		90		ms
Time to rate data within full specifications	tSTABLE	2			500	ms
AVDD for internal RESET	VRU	3, 7			1.0	VDC
Detectable AVDD glitch	tG	7	10			ns
Reset threshold	VRESET	4	2.5		3.5	VDC
Status Register AVDD OK flag (PRNG_OK) threshold	VPRNGH	5	5.55		5.91	VDC
	VPRNGL		4.2		4.43	
Reset delay	tRSTN	6, 7	128		208	μs

- Note 1:** The voltage V_{DD-MIN} is the lower limit for V_{DD} and A_{VDD} as specified in chapter 5.
- Note 2:** The startup time is defined as the time until the Status Register EXC_OK flag goes to '1' (sensor excitation has stabilized). Reading from the device during this time interval causes the device to respond with Error Code. The time to stable data is defined as the time from the end of t_{INIT} until the angular rate data is within full specifications. Angular rate data can however be read from the device during this time interval.
- Note 3:** Internal reset signal is defined for supply voltage above V_{RU} .
- Note 4:** Internal reset is activated when the supply voltage passes V_{RESET} . The reset threshold has a small hysteresis (approx. 0.1V).
- Note 5:** The RARH and RARLX commands return the Error Code when $AV_{DD} \leq V_{PRNGL}$ or $AV_{DD} \geq V_{PRNGH}$.
- Note 6:** For correct OTP power-down a reset pulse width of minimum 50 μs is needed.
- Note 7:** By design.

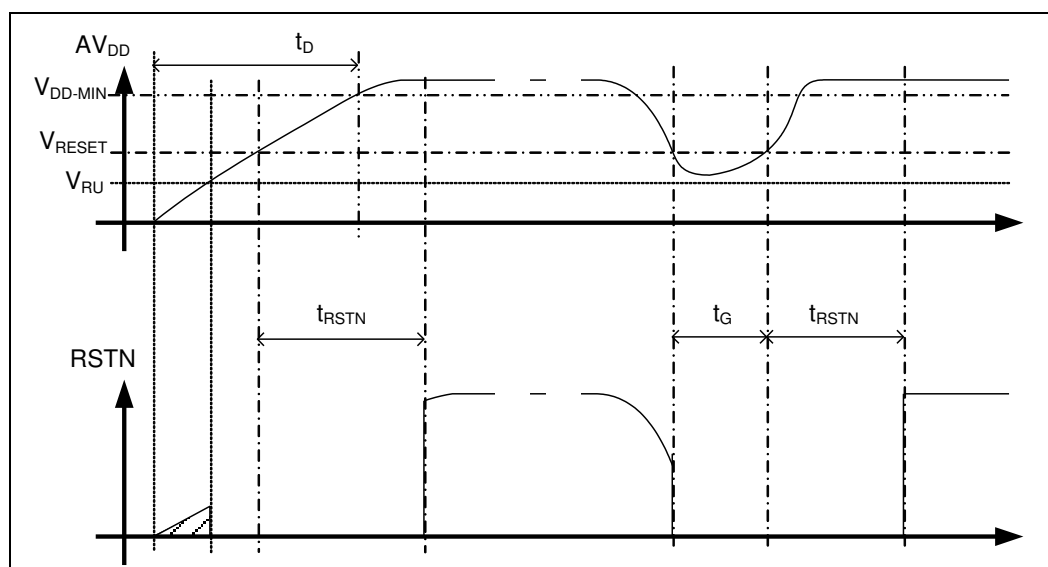


Figure 9-3 Power-up and power glitch reset timing

10 STATUS REGISTER AND INTERNAL DIAGNOSTIC MONITORING

Internally in the SAR100, there are 6 error monitoring functions employed to make sure irregular output angular rate is detected. If any of the monitoring functions detects an irregular condition the corresponding flag becomes '0', otherwise it becomes '1'. The Status Register flags are available to the application via the RSR SPI command. It is assumed that a flag can signal an "error" for any length of time. To make sure short error ('0') pulses are visible to the application, the '0' pulses are "stretched" in time to between 1.5 and 2.0 ms.

Bit Position	Flag Name	Monitoring function	Recoverable
7	ADC_OK	ADC_OK is '0' if an ADC overflow occurs, otherwise '1'.	Yes
6	SIG_OK	SIG_OK is '0' if an arithmetic overflow or underflow occurs in the digital signal processing, EXCEPT if the signal amplitude exceeds the output range in the final scaling (by the S0INV parameter), otherwise '1'.	No
5	OTPPAR_OK	OTPPAR_OK is '0' if OTP parity check fails, otherwise '1'.	No
4	ATEST_INACTIVE	ATEST_INACTIVE is '0' if an analog test mode is active, otherwise '1'. This monitoring function will not result in any Error Code signaling.	-
3	PRNG_OK	PRNG_OK is '0' if the AVDD voltage is out of range, otherwise '1'.	No
2	DET_OK	DET_OK is '0' if a sensor die detection electrode connection is open or if a leakage current is present on one or both electrodes, otherwise '1'.	No
1	EXC_OK	EXC_OK is '0' if the excitation control loop fails to lock on resonance frequency such that the excitation amplitude falls below a critical level, otherwise '1'.	Yes
0	(no name)	Not used. Always '1'.	-

After power-up, and until the device start-up is complete, the output from the RARH and RARLX commands is substituted by the Error Code, see chapter 7.3. After start-up, if any of the flags go to '0' (the internal monitoring functions indicate that the output is irregular), the Error Code is the output from the RARH and RARLX commands, and also internal digital signal processing is held. This signaling continues indefinitely until the device is powered down, or, in case of some of the 'Recoverable' error conditions in the table above, until the PRCEN command is issued.

The PRCEN command execution must obey the following algorithm:

1. Wait until no recoverable error conditions are flagged (polling the Status Register)
2. Wait minimum 30 ms (recommended 100 ms)
3. Execute the SGDIS1, -2 and -3 commands
4. Execute the PRCEN command
5. Execute the SGEN command

Note that for the PRCEN command to take effect, the Safe Guard must first be disabled by means of the SGDIS1,-2 and -3 commands. To resume normal operation after recovery, the SafeGuard is re-enabled by using the SGEN command. Note also that no error conditions will be latched while the SafeGuard is disabled.

11 PACKAGE INFORMATION

11.1 Physical dimensions, material and weight

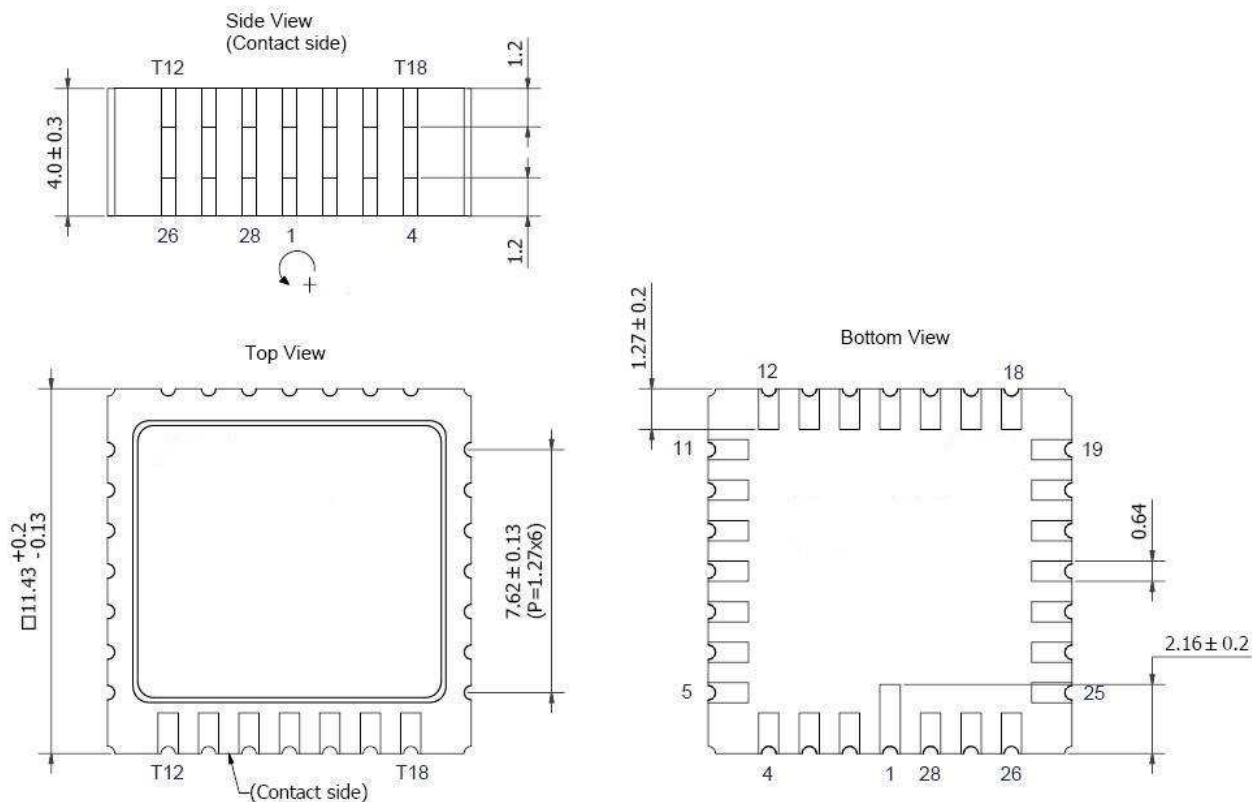


Figure 11-1: SAR100 package dimensions. Top, side and bottom view

Notice the direction of positive rotation for SAR100 (indicated in the upper left of the figure).

Characteristics	Specifications
Package type	Ceramic alumina LCC
Number of pins	28
SAR100 weight	1.5 grams

11.2 Labeling

Label text	Specifications
SAR100	Product name
###	Angular rate range in %s
YY	Year
WW	Week
XXX	Lot number
ZZZ	Device serial number

11.3 Pin Configuration

Horizontal Mount	Vertical Mount	Pin Name	Type	Direction	Note	Function and comment
1	1	GND	Power			Ground plane of die attach area. Connect to ground
2	2	AVSS	Power			Analog ground. Connect to ground
3	3				1	Test pin. Connect to ground
4	4	REFV				Internal voltage reference. Connect a 10 nF low ESR decoupling capacitor between this pin and ground.
5					2	NC
6					2	NC
7					2	NC
8					2	NC
9					2	NC
10					2	NC
11					2	NC
12	T18				1	Test pin. Connect to ground
13	T17				1	Test pin. Connect to ground
14	T16	AVDD	Power		3	Analog supply voltage
15	T15				2	NC
16	T14	VDD	Power		3	Digital supply voltage
17	T13	MOSI	Digital	Input		SPI data input
18	T12	MISO	Digital	Output	4	SPI data output
19					1	Test pin. Connect to ground
20					1	Test pin. Connect to ground
21					1	Test pin. Connect to ground
22					2	NC
23					1	Test pin. Connect to ground
24					1	Test pin. Connect to ground
25					1	Test pin. Connect to ground
26	26	SCLK	Digital	Input		SPI clock
27	27	LOAD	Digital	Input		SPI load
28	28	VSS	Power			Digital ground. Connect to ground

Note 1: Connect to ground to minimize noise levels.

Note 2: These pins are not connected to anything.

Note 3: Connect these pins together on the printed circuit board and from there a 100 nF low ESR decoupling capacitor to ground.

Note 4: This signal is tri-stated when LOAD is logical '1' ($> 0.7V_{DD}$).

NOTES

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