RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 32 watt asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, P_{out} = 32 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

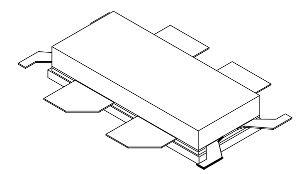
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	14.9	45.7	8.0	-28.9
2570 MHz	15.4	45.6	7.9	-30.8
2690 MHz	15.1	44.5	7.8	-33.0

Features

- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13-inch Reel.

AFT26H160-4S4R3

2496-2690 MHz, 32 W AVG., 28 V



NI-880XS-4L4S

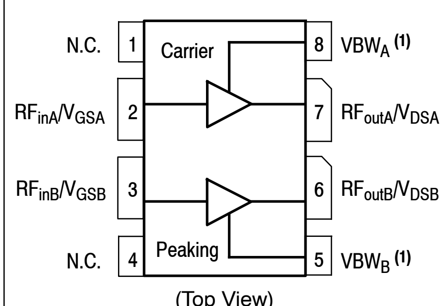


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 5 and pin 8.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 32 W W-CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, 2590 MHz	$R_{\theta JC}$	0.41	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (4) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 80 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 500 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 6 Vdc, I_D = 0.8 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics - Side B (4) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 6 Vdc, I_D = 1.2 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, P_{out} = 32 W Avg., f = 2496 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.5	14.9	16.5	dB
Drain Efficiency	η_D	41.5	45.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	8.0	—	dB
Adjacent Channel Power Ratio	ACPR	—	-28.9	-26.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 500 mA, f = 2570 MHz					
VSWR 10:1 at 32 Vdc, 160 W CW Output Power (3 dB Input Overdrive from 100 W CW Rated Power)	No Device Degradation				
Typical Performances (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.6 Vdc, 2496-2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	100	—	W
P_{out} @ 3 dB Compression Point [3]	P3dB	—	200	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496-2690 MHz frequency range)	Φ	—	-30.1	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 32 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.009	—	dB/°C

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

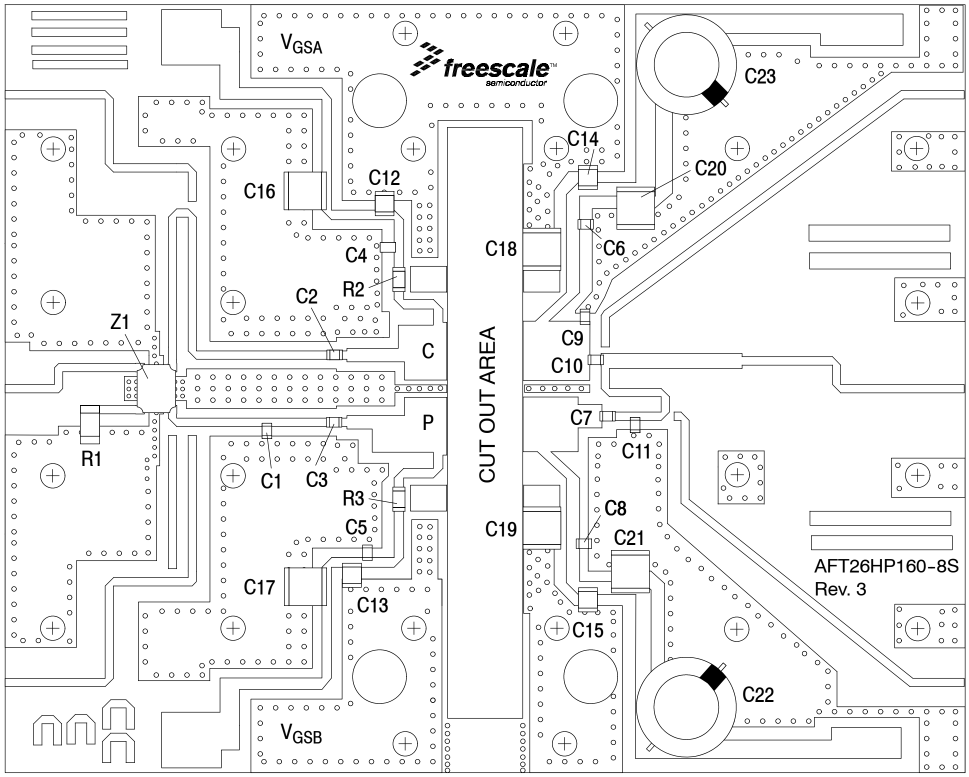


Figure 2. AFT26H160-4S4R3 Test Circuit Component Layout

Table 5. AFT26H160-4S4R3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C11	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C2, C3, C4, C5, C6, C7, C8	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C9	0.4 pF Chip Capacitor	ATC600F0R4BT250XT	ATC
C10	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
C12, C13, C14, C15	2.2 μF Chip Capacitors	C3225X7R2A225K230AB	TDK
C16, C17, C18, C19, C20, C21	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C22, C23	220 μF, 100 V Electrolytic Capacitors	MCGPR100V227M16X26-RH	Multicomp
R1	50 Ω, 4 W Termination	CW12010T0050GBK	ATC
R2, R3	2.7 Ω, 1/4 W Chip Resistors	CRCW12062R7FKEA	Vishay
Z1	2300-2700 MHz Band, 90°, 5 dB Hybrid Coupler	X3C25P1-05S	Anaren
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

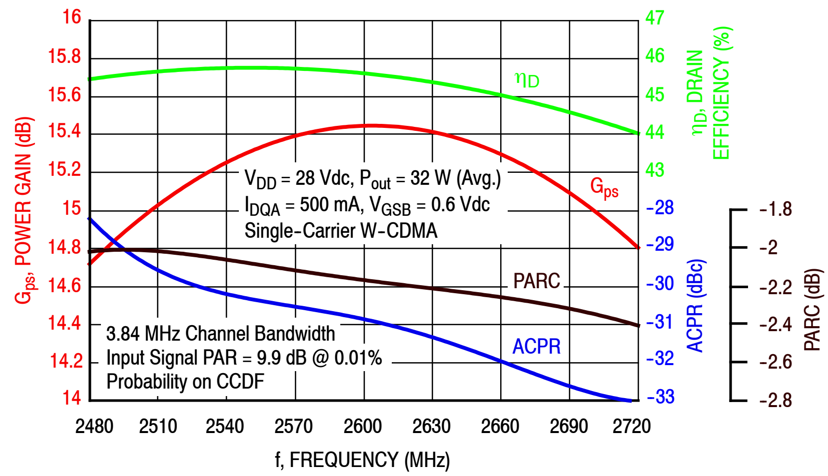


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 32 Watts Avg.

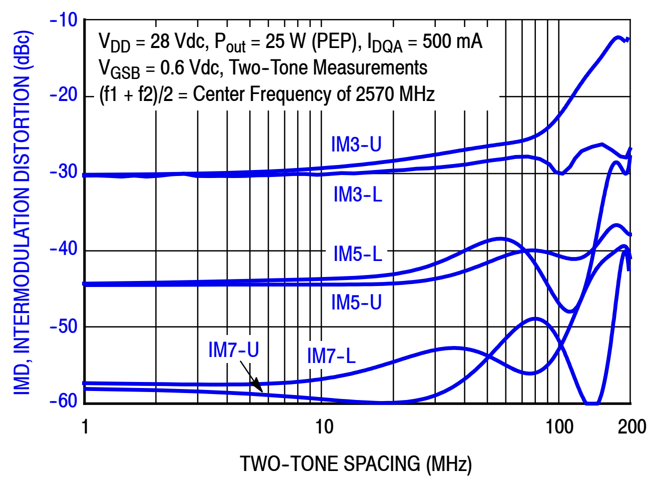


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

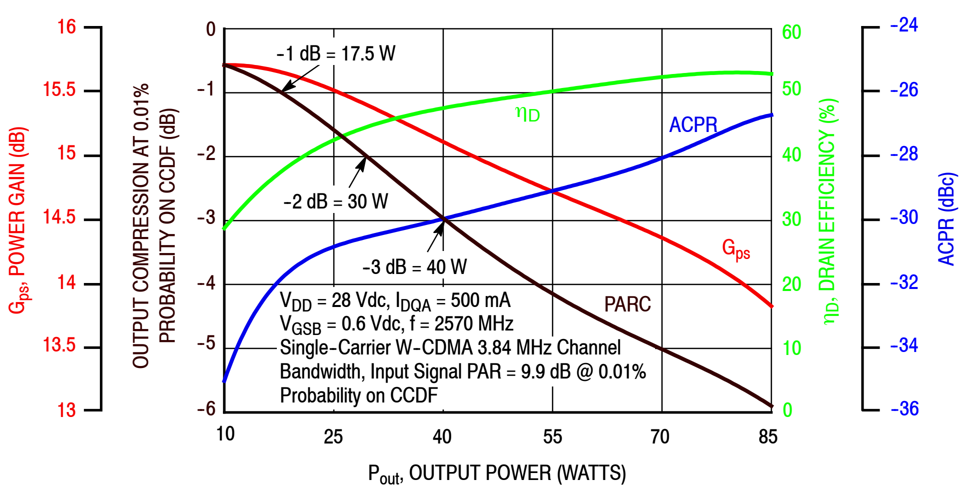


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

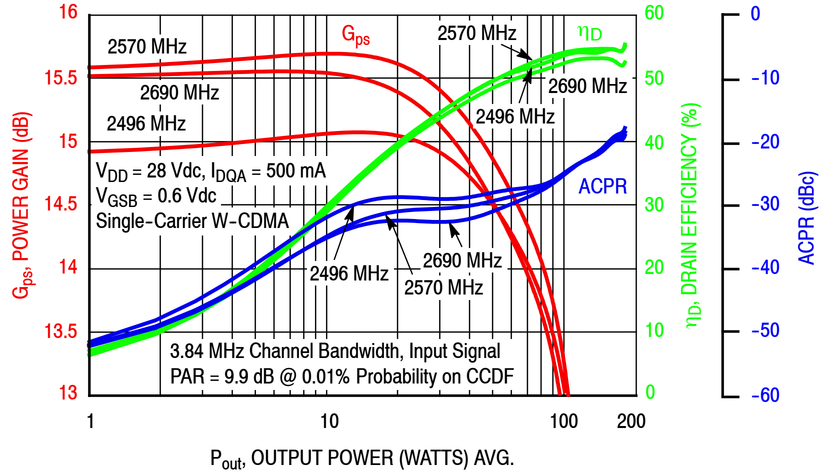


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

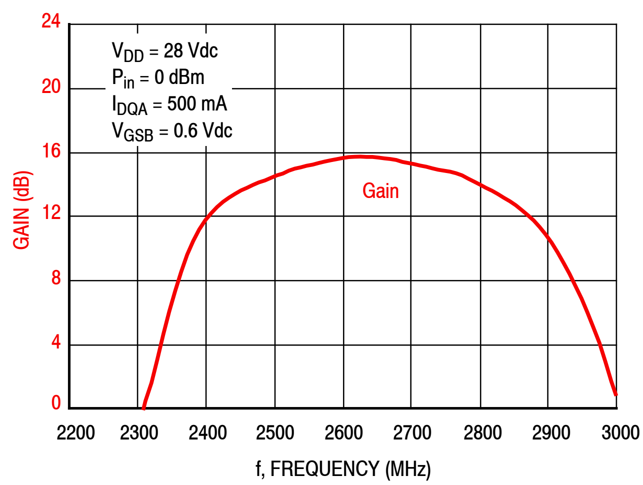


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 492 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.68 – j14.6	6.44 + j14.3	4.25 – j6.60	18.7	49.3	86	54.2	–12
2570	10.5 – j14.5	9.37 + j14.6	4.08 – j6.60	18.6	49.3	86	54.6	–13
2690	18.5 – j7.11	18.7 + j7.55	3.90 – j7.10	18.6	49.2	84	52.9	–12

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.68 – j14.6	6.75 + j15.3	4.01 – j7.07	16.5	50.2	104	53.7	–17
2570	10.5 – j14.5	10.4 + j15.8	3.85 – j7.11	16.3	50.1	103	53.5	–17
2690	18.5 – j7.11	21.2 + j5.79	3.85 – j7.75	16.4	50.0	101	52.1	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

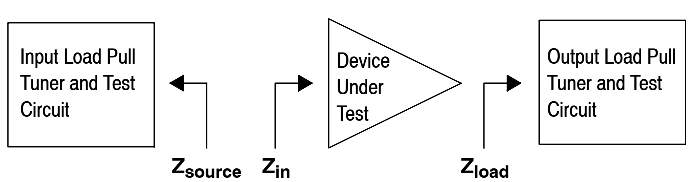
V_{DD} = 28 Vdc, I_{DQA} = 492 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.68 – j14.6	6.05 + j14.7	9.14 – j4.04	21.0	47.6	58	62.8	–20
2570	10.5 – j14.5	8.94 + j15.3	7.19 – j3.17	20.8	47.7	59	63.2	–21
2690	18.5 – j7.11	19.1 + j8.75	5.76 – j3.49	20.8	47.6	58	61.6	–21

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.68 – j14.6	6.36 + j15.5	7.51 – j5.25	18.4	49.0	79	63.6	–25
2570	10.5 – j14.5	9.81 + j16.4	6.90 – j3.94	18.5	48.7	74	63.7	–27
2690	18.5 – j7.11	21.7 + j6.99	5.56 – j4.59	18.4	48.8	75	61.9	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.34 – j16.2	4.65 + j15.8	6.04 – j9.43	13.5	51.0	126	53.4	26
2570	6.43 – j16.1	6.85 + j16.3	6.01 – j9.36	13.5	51.0	125	53.3	21
2690	15.7 – j11.8	15.8 + j12.5	6.40 – j10.4	13.4	50.9	122	51.6	25

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.34 – j16.2	5.00 + j16.4	5.78 – j10.4	11.2	51.7	148	53.8	18
2570	6.43 – j16.1	7.70 + j17.1	6.01 – j10.3	11.4	51.6	146	53.8	16
2690	15.7 – j11.8	18.0 + j11.1	6.96 – j11.3	11.3	51.5	141	52.1	23

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.34 – j16.2	4.19 + j15.8	13.7 – j7.40	14.5	49.5	89	62.6	18
2570	6.43 – j16.1	6.11 + j16.5	9.99 – j4.88	14.7	49.7	94	63.5	22
2690	15.7 – j11.8	15.0 + j14.0	8.15 – j5.32	14.5	49.8	95	61.7	21

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	4.34 – j16.2	4.56 + j16.4	13.7 – j8.25	12.5	50.1	102	62.1	9
2570	6.43 – j16.1	7.00 + j17.2	11.9 – j5.77	12.6	50.1	103	63.2	11
2690	15.7 – j11.8	17.5 + j12.7	8.15 – j5.47	12.5	50.3	108	61.5	12

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

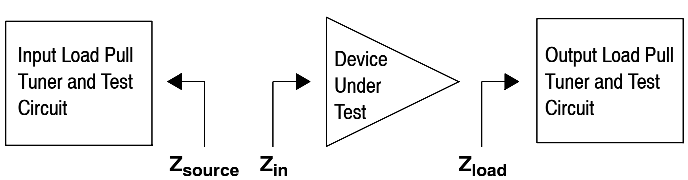


Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2570 MHz

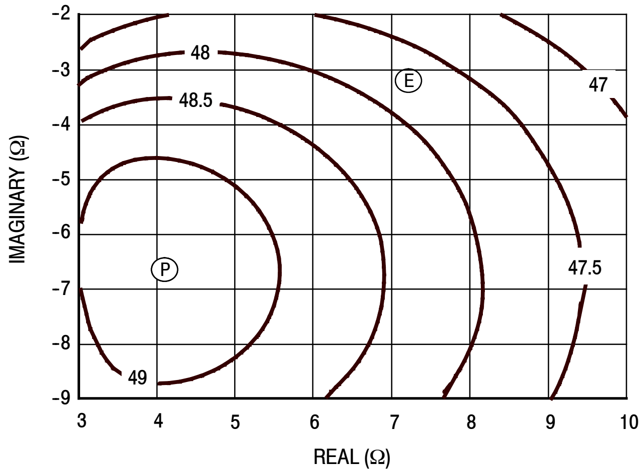


Figure 12. P1dB Load Pull Output Power Contours (dBm)

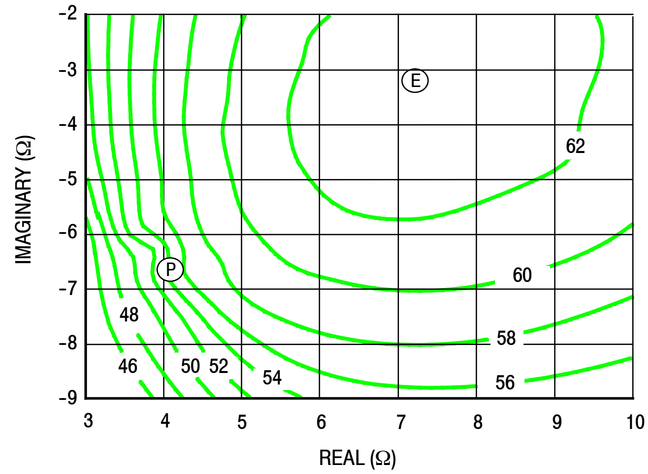


Figure 13. P1dB Load Pull Efficiency Contours (%)

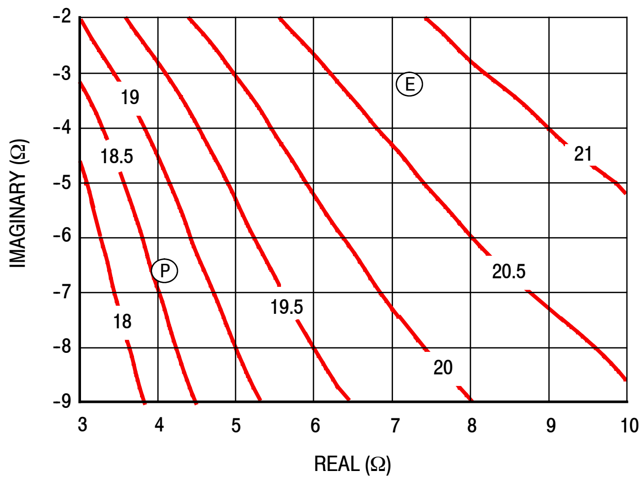


Figure 14. P1dB Load Pull Gain Contours (dB)

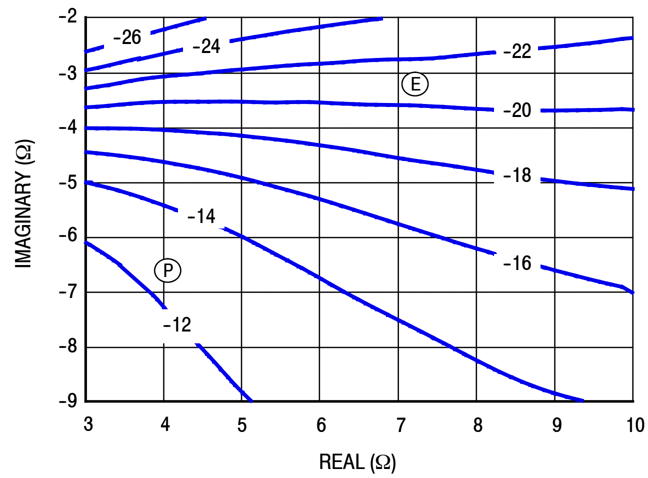


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2570 MHz

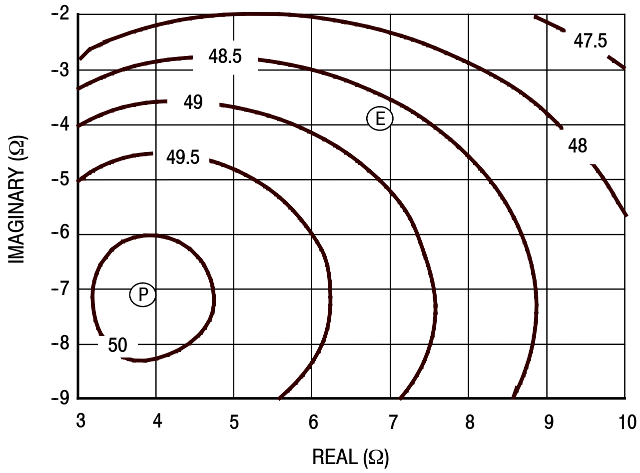


Figure 16. P3dB Load Pull Output Power Contours (dBm)

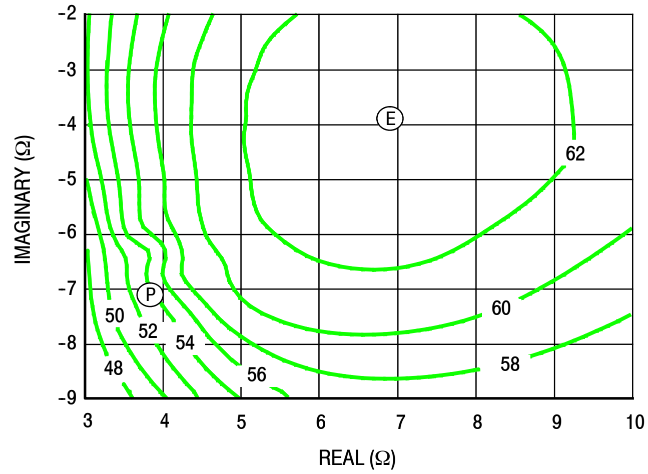


Figure 17. P3dB Load Pull Efficiency Contours (%)

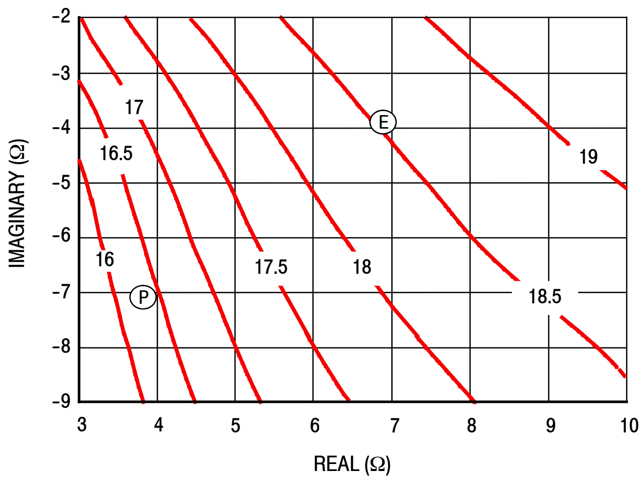


Figure 18. P3dB Load Pull Gain Contours (dB)

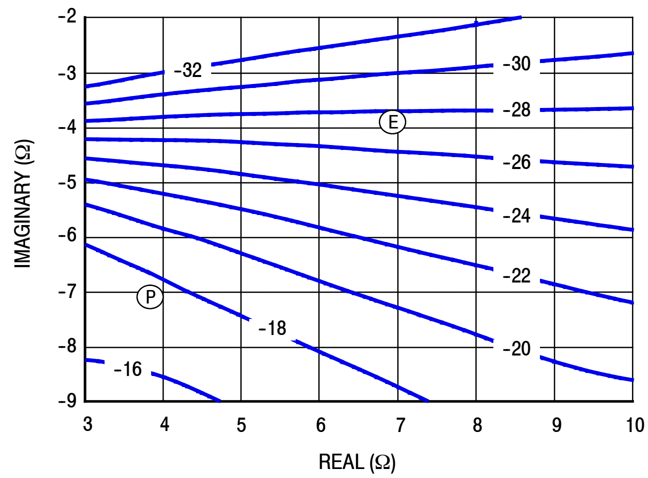


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2570 MHz

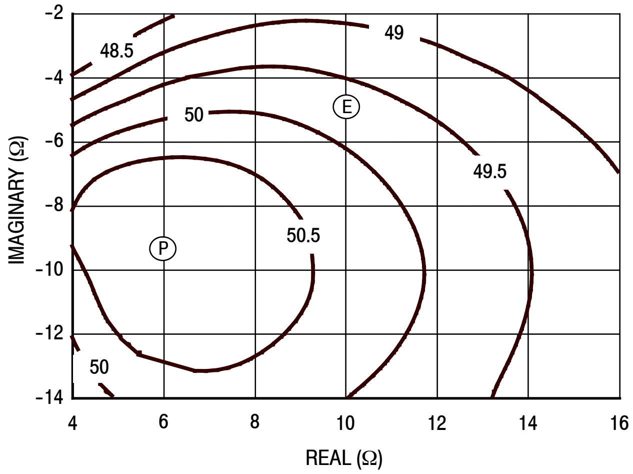


Figure 20. P1dB Load Pull Output Power Contours (dBm)

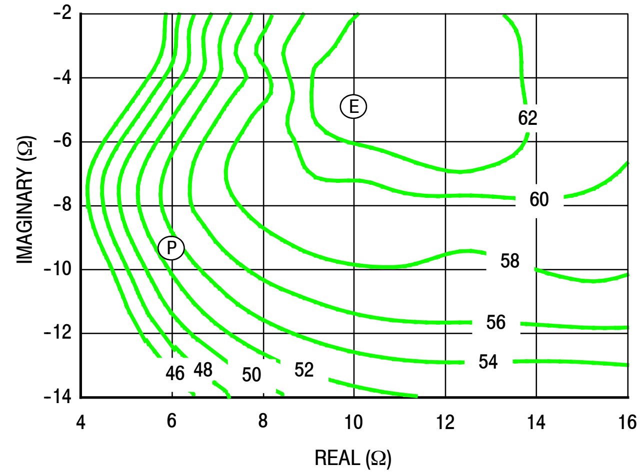


Figure 21. P1dB Load Pull Efficiency Contours (%)

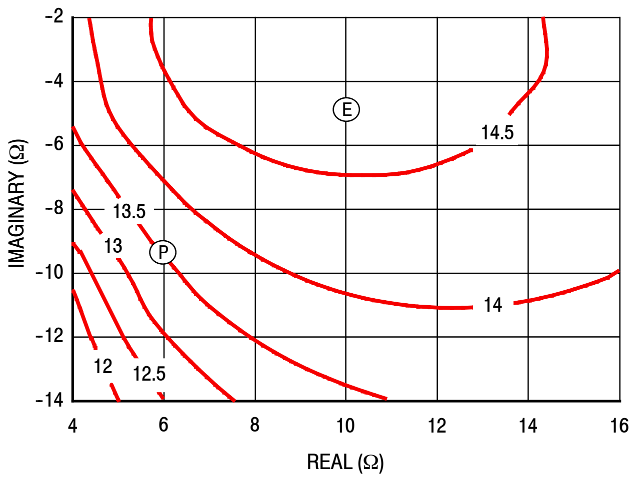


Figure 22. P1dB Load Pull Gain Contours (dB)

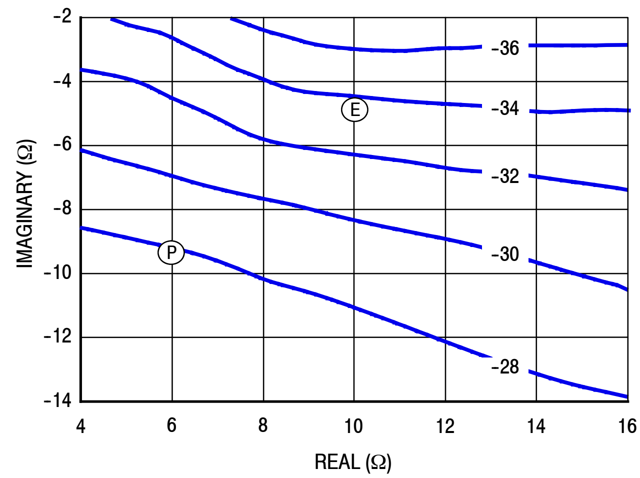


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2570 MHz

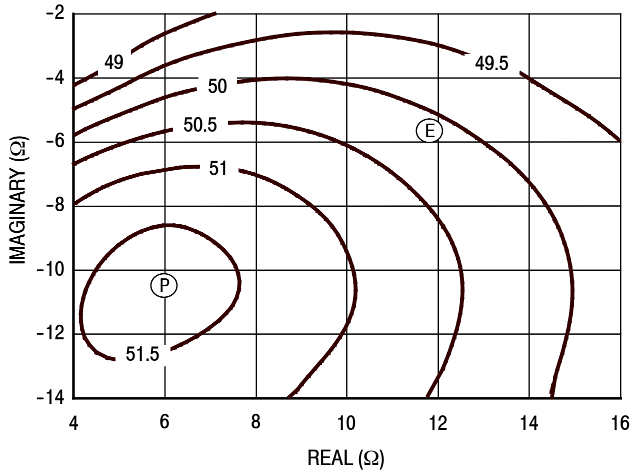


Figure 24. P3dB Load Pull Output Power Contours (dBm)

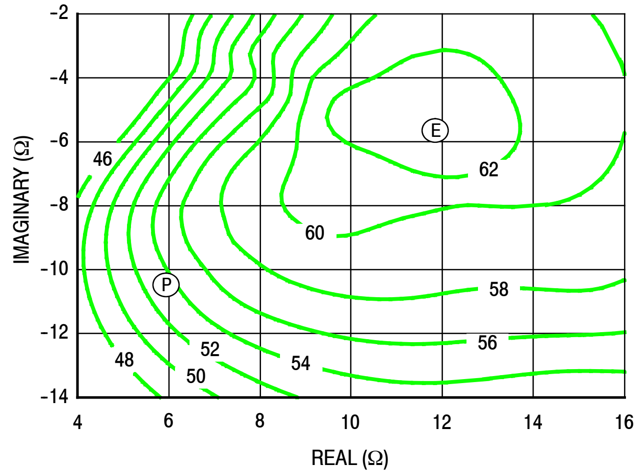


Figure 25. P3dB Load Pull Efficiency Contours (%)

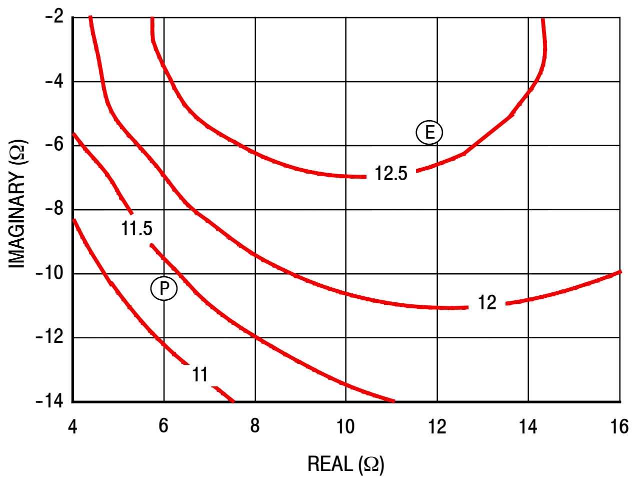


Figure 26. P3dB Load Pull Gain Contours (dB)

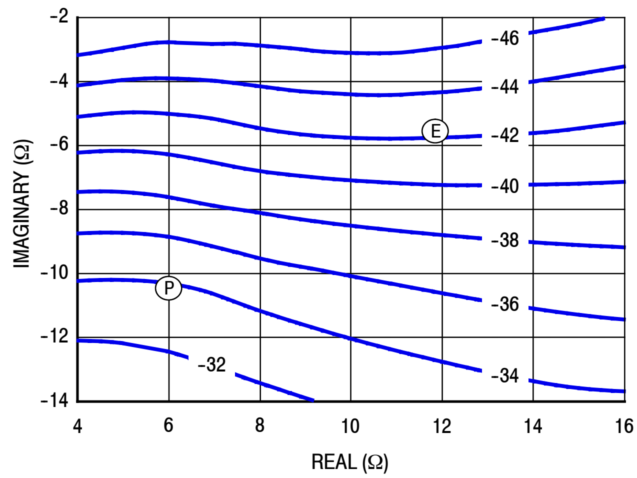


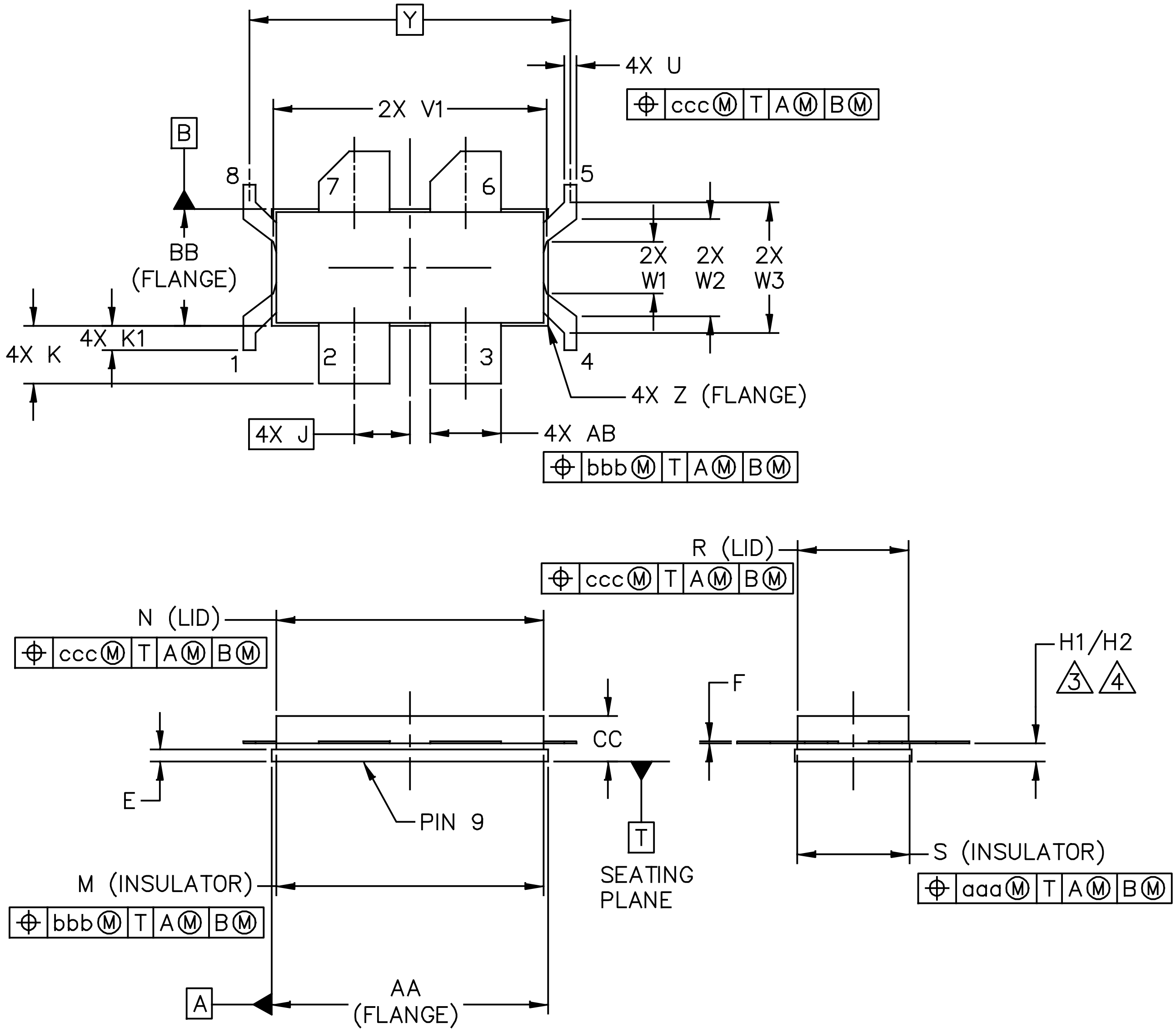
Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

2. CONTROLLING DIMENSION: INCH

3. (△) DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2, 3, 6 & 7. H2 APPLIES TO PINS 1, 4, 5 & 8.

4. (△) TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.905	.915	22.99	23.24	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.895	.905	22.73	22.99
F	.004	.007	0.10	0.18	W1	.165	.175	4.19	4.45
H1	.057	.067	1.45	1.70	W2	.315	.325	8.00	8.26
H2	.054	.070	1.37	1.78	W3	.425	.435	10.80	11.05
J	.184 BSC		4.66 BSC		Y	1.056 BSC		26.82 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
K1	.070	.090	1.78	2.29	AB	.228	.238	5.79	6.05
M	.874	.886	22.20	22.50	aaa	.005		0.13	
N	.872	.888	22.15	22.56	bbb	.010		0.25	
					ccc	.015		0.38	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2013	• Initial Release of Data Sheet

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