

DATASHEET

Easily balance performance with power and area requirements

Optimized interconnect provides advanced features with low gate count
 Small generated logic clusters ease maximum SoC core packing
 Low power for maximum battery life

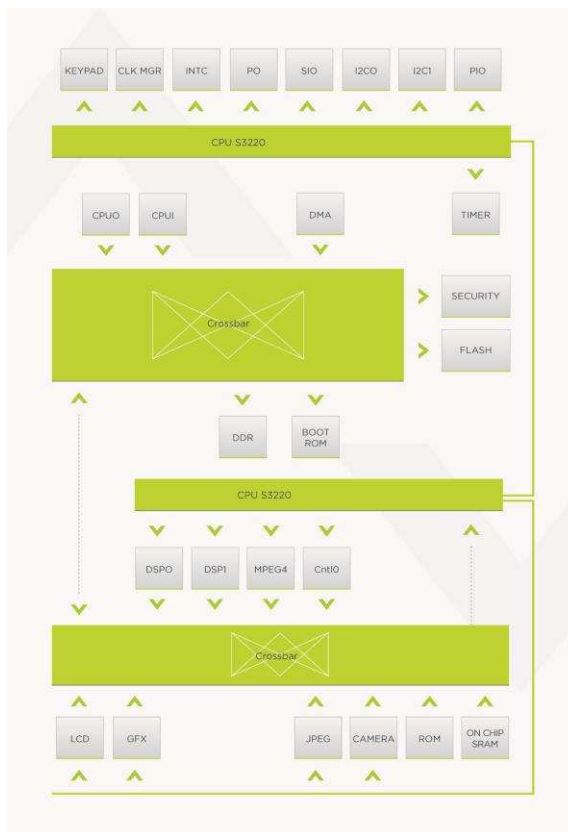
Simplify complex SoC designs

Universal Connectivity: Seamless connection to OCP, AHB, and AXI based cores
 Full user control of latency, performance, and area
 Robust development tools with pre-configured SoC templates speed time-to-market

Sonics expertise helps speed time-to-market and ensures quality

Unique design methodology eases timing closure and speeds design iteration cycles
 Integrated performance analysis tools rapidly uncover design hotspots for quick recovery
 World-class engineering support for first-time-right silicon

The SonicsLX on-chip network from Sonics, offers SoC designers a configurable system IP block designed for the creation of complex on-chip interconnections between cores. SonicsLX offers designers a balanced solution which couples low-power and tuned area, with high performance. SonicsLX utilizes state-of-the-art physical structure design and advanced protocol management to deliver guaranteed high bandwidth together with fine grained power management. Employing both a full or partial crossbar bus structure, the SonicsLX interconnect provides low latency paths between high-bandwidth master and target IP cores.



SonicsLX is configured using Sonics state-of-the-art development tool suite, StudioXE. StudioXE provides designers with a comprehensive development tool designed to speed interconnect configuration, analyze performance, and perform system validation. Designed with both SoC experts and new users in mind, StudioXE scales for both sets of users. For expert designers, StudioXE allows fine-grained tweaking of a vast array of modules and settings within each specific IP component, allowing users to tune the IP to their specific design needs. For less experienced users, StudioXE provides quick start templates for popular SoC designs, allowing for a quicker time to completion as settings are pre-configured for each specific design.

Gain Access to Advanced Technology and Make Better Products

SonicsLX incorporates technology innovations designed for practical application for today's Multicore SoCs. SonicsLX is also highly configurable so that each instantiation can exactly match specific SoC design requirements while also maintaining an interconnect centric, or platform style, architecture across product lines:

- Low latency interconnect – SonicsLX combines key networking concepts, such as protocol layering, internal transports, end to end QoS mechanisms, and advanced error management, with flexible decoupling and topology choices to enable instances that offer both the low latency of computer structures and the scalability of networks. Intelligent point to point protocol management ensures that high performance data flows are achieved while maintaining low latencies.
- Multithreaded non-blocking flow control – A key design challenge of multicore SoCs is the ability to design and verify complex interconnect fabric architectures that guarantee IP cores can gain and maintain access to the system and external memory when needed. The advanced technology innovations built into SonicsLX enables interconnect solutions that exactly match each SoC application while minimizing traffic interaction across the high volume of transactions that occur in Multicore SoCs. End to End QoS adds another layer of predictability and scalability by guaranteeing bandwidth for each of the system elements while maintaining low latency.
- Practical GALS - Simplified timing closure, reduced power dissipation, and increased system flexibility are driving SoC designers to GALS approaches, SonicsLX provides a complete GALS architecture supporting asynchronous, dynamic divided synchronous, and fully synchronous clock domains, with optional voltage domain crossing. A complete

Sonics GALS solution, including SonicsLX, SonicsExpress, Sonics MemMax, and Sonics3220 delivers the benefits of GALS while maintaining full compatibility with standard design flows

Utilize Unprecedented Architecture Design Flexibility to drive Rapid Development with High Predictability

New product innovations built into SonicsLX provide architects, chip developers, and software developers with configuration options that ease system level design, IP core connectivity and fabric topology decisions.

- Advanced System Partitioning -SonicsLX uses socket based protocol management which decouples the IP core from the interconnect. This decoupling introduces a great level of modularity for any SoC design, facilitating late design changes with minimal re-design and verification.
- Universal IP core connectivity – Ensures any IP core supporting an OCP, AHB, or AXI interface can be attached to the interconnect seamlessly. Intelligent transport protocol management incorporated in SonicsLX guarantees high performance even when IP cores of different types are connected.

Advanced Configuration and Modeling Automation Accelerates Time-to-Market and Lowers System Verification Risks

Access to technology innovations supported in SonicsLX through the automated configuring and modeling capabilities of the StudioXE development suite facilitates rapid research and decision making with respect to the trade-offs between architecture choices:

- Tuned Performance – The ability to rapidly configure an array of topology choices and then model and verify protocols and data flow paths at the system level enables SoC developers to match the interconnect behavior exactly to the SoC requirements and achieve the highest performance possible.

- Low Latency – Combining intelligent point to point protocol management ensures that high performance data flows also maintain low latencies.
- Low power – The advanced design optimizations as well as coarse and fine grain clock gating that are part of SonicsLX offers orders of magnitude lower power than conventional computer bus designed interconnects.
- Minimal Area - Automated configuration and modeling enables SoC developers to utilize the high configurability of SonicsSX to rapidly iterate system level instantiations and minimize area while preserving performance and power.
- Rapid Performance Verification – As part of the advanced automation provided within Sonics suite of development tools, SystemC models and RTL netlists are generated from the same database for use in performance validation. By employing statistical modeling within StudioXE, SoC developers can analyze and verify performance of the interconnect configuration before the SoC design begins.
- Concurrent hardware and software development – Pre-verified data flows ensure performance is predictable, enabling design teams to focus on hardware execution, and gives software teams the ability to rely on predictable performance early in the design cycle to streamline software development.

Take Advantage of Data Flow Services to Improve Time to Market and Lower Design and System Verification Risks

Basic data flow services supported by SonicsLX enables engineering teams to conquer the system management challenges present in today's Multicore SoC design in rapid time and with less project risk:

- Power management - Available to address both active and standby power management. When operating the interconnect in conjunction with power management controllers the complete

design or specific portions of it can be shut down as needed. Internal coarse and fine grain clock gating are used to minimize the standby power consumed by the interconnect.

- Quality of service (QoS) – The ability to guarantee data flow in a complex heterogeneous distributed processing environment is paramount to the success of any multicore SoC design. The QoS data flow service built into SonicsLX ensures that SoC developers can manage any level of complexity.
- Security management - SonicsLX employs the latest innovations in security management, including firewalls, and regional isolation of portions of the SoC for conditional access. Security data flow services build on classical processor based security to provide SoC developers with a comprehensive scheme for addressing even the most stringent security requirements.
- Data width conversion – The ability to seamlessly connect any IP core to SonicsLX ensures that SoC design and verification is greatly accelerated. Data width conversion is a key data flow management service which further ensures that the connection of IP cores across the system is handled seamlessly and with optimal efficiency.

Improve Product Line Management through Advanced Architectural Automation

The combination of a highly configurable interconnect and the high degree of automation and technology innovation delivered as part of StudioXE ushers in a new methodology for managing product lines. By transitioning to an interconnect-centric, platform style architecture, entire product lines can be built from a single architecture. Taking advantage of the wealth of innovation provided by Sonics, many customers today have realized the compounding benefits associated with utilizing this methodology, including:

- Progressively declining development costs and risks as the product derivatives are re-engineered
- Transition of IP libraries at the pace most comfortable for the architecture and design teams
- Accelerating time to market with each derivative developed

SonicsLX features include:

On-chip network architectural Features

Natively supports OCP 3.x sockets, OCP 2.x sockets, AXI 3/4, and AMBA AHB-lite 2.0 sockets

- Support for up to 32 sockets in each SonicsLX instance. Each socket can connect to an initiator core, a target core or an instance of another on-chip network.
- Configurable to provide a full or partial crossbar topology.
- Implements dynamic, endianness-aware data width conversions.
- Configurable address widths up to 64 bits.
- Target address decoding to a granularity of 1 kilobyte.
- Support for configurable, run-time programmable protected regions within the address space.
- Configurable data path widths (at sockets and internally) of 16, 32, 64, or 128, or 256 bits. A 4:1 ratio of data widths is allowed within a SonicsLX instance.
- Accommodates synchronous and synchronous-divide clock rates for each socket.
- Permits clock rates of up to 300 MHz subject to technology and configuration choices.
- Flexible internal pipelining makes frequency independent of span.
- Supports zero cycle minimum latency paths.
- Supports differential quality of service (low latency, allocated bandwidth, and best effort).
- Supports BLCK burst sequences on OCP2 sockets.
- Supports two multi-channel target groups.

- Supports a software-visible global address map.
- Provides pipeline-point link exchanges.

Power Management Features

- Supports initiator sideband signaling for interrupts, errors, and power controls.
- Power management interface coordinates voltage and/or clock removal.
- Implements fine- and coarse-grained clock gating for low idle and active power.

Error Handling Features

- Monitors for software error conditions (unsupported commands, protection violations, and addressing errors) and protection violations.
- Monitors for failing cores (timeouts).
- Error logging and recovery support.
- Supports virtual debug ports to probe operation of internal paths during simulation.
- Supports optional physical debug ports to probe operation of internal paths during operation.

Description

SonicsLX can act as a global or local subsystem interconnect. The high degree of configurability built into SonicsLX ensures that optimal performance, low power, and minimal area are all achieved for either use model. The high degree of automation delivered through StudioXE also ensures that configuring SonicsSX can be accomplished rapidly with a completely modeled result that is fully optimized.

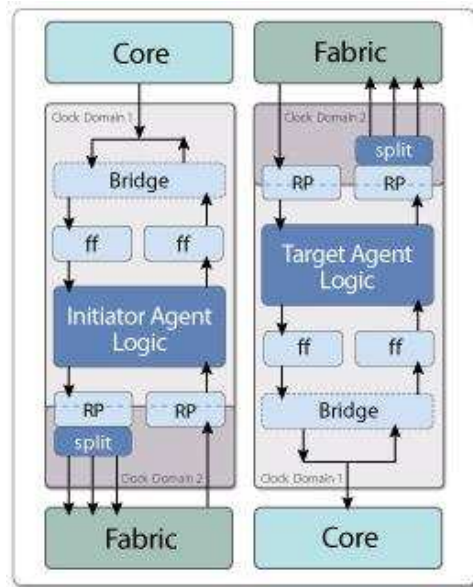
Up to 2 crossbars can be joined to form a single SonicsLX instance that supports up to 32 cores. SonicsLX supports SoC cores operating at different clock rates. Local clocks can be scaled (frequency divided) from a common source, and the scaling factor can change dynamically to minimize power demands. SonicsLX operates with power management controllers (external to the interconnect) to change voltage levels and clock rates for the SoC cores. SonicsLX interfaces

manage rapid power down transitions while preventing data loss.

SonicsLX provides a fully configurable SoC interconnect fabric that supports transport, routing, and arbitration and translation functions. To adapt to targets with long or unpredictable latency such as DRAM, SonicsLX establishes independent request and response networks that are configured with the overall topology.

Agents

Cores connect to SonicsLX through adaptive “Agents”, using standard socket interfaces that isolate the cores from one another. Both socket and internal data path widths can be configured as 16, 32 or 64 bits. Agents within SonicsLX fully decouple the functionality of each core from the rest of the system.



Agents support the various flavors of OCP, AXI or AHB cores. Agents handle any mismatches in data width, clock frequency, or protocol among the various core interfaces and the

interconnect while balancing the requirements of latency, physical span, clock frequency, die area and power consumption.

For targets and initiators, the state machines in their corresponding agents handle buffer and thread management, where a thread can create multiple paths on the same set of wires. To support ongoing (and outstanding) transfers for each thread, SonicsLX

handles arbitration for all initiator cores and address decoding and routing for all targets. Each initiator or target agent decouples its associated core from the switching fabric.

Exchanges

Agents are embedded in an exchange and provide sockets for the attached cores. The agents use “register points” (small FIFOs) as needed to break long combinatorial timing paths and maintain the required frequency over distance. A “pipeline point,” consisting of a configurable number of register points, connects two exchanges. A pipeline point is responsible for staging data transfers and flow control between the exchanges it connects, adjusting the data width as required, and supporting the crossing of clock domain boundaries. A special agent, the register target is embedded in an exchange and provides an access point to the internal configuration registers.

Crossbar Exchange (XB)

An XB exchange provides dedicated links connecting multiple initiators to multiple targets with minimum latency. Each XB exchange can connect up to 16 cores in an 8x8 configuration. With more than 8 initiators connected to any one target, the maximum achievable frequency may be low. Full crossbar connectivity is not required. The XB exchange provides arbitration for access to targets on the request side and initiators on the response side, while performing any data width conversion needed between initiators and targets.

Register Points

The Register Points breaks timing path between an agent and the fabric. It is also used for clock domain crossing, multi-path split and can be configured independently on request and response path. For designs need to achieve its highest possible frequency, setting both request and response Register Points and socket flop options (i.e. registered output) on all agents is desirable.

Pipeline Points

Pipeline points (PP) are required between exchanges and are used to stage transfers between exchanges, adjust data widths or cross clock boundaries. Pipeline points are composed of register points. Pipeline points permit the physical span from initiator to target to be increased without lowering the operating frequency of the connection. As needed, pipeline points permit frequency conversion (1:N or N:1), establishing distinct clock domains operating at different frequencies.

Clock Domains

SonicsLX supports multiple clock domains. Agents and the register target may be assigned to clock domains. An exchange can reside in only one clock domain, with clock domain crossings occurring in the pipeline points between exchanges or in the register points embedded in the agents. This allows the agent to reside in the same clock domain as the core it connects to. Clock domain crossings require the specification of a separate clock for each domain. Clock domain crossings may be used to control the frequency of the clock domain, dividing a fast base clock by an integer divisor. Either the exchange or one of the embedded cores can have the fastest clock. The ability to dynamically change divide ratios provides an additional level of power management control.

Topologies

Up to 2 XB exchanges can be joined to form a single SonicsLX instance, supporting up to 32 sockets. Each socket can connect to an initiator or target core, or another instance of a Sonics interconnect (either a SonicsLX or the Sonics3220 interconnect). The user determines the overall topology of a SonicsLX instance. A SonicsLX instance can occupy a portion of the SoC address space from 2^{10} ~ 2^{40} bytes. Some of that addressable space may reside in targets that are directly connected to the SonicsLX instance, while some may reside in targets connected to another instance to which this instance is chained.

Performance

SonicsLX provides a number of performance advantages associated with threading and thread mapping, bandwidth, latency and QoS arbitration. The flexibility inherent in the architecture easily allows trade-offs between the selected features through their associated parameters, and gate count or performance. A variety of parameters can be easily modified showing initiator agent performance parameters.

Threading and Thread Mapping

All requests on a connection start on a thread of the initiator core and end on a thread of the target core. Within the SonicsLX interconnect, initiator threads are mapped to target threads. If the target core is single-threaded, every thread from every connected initiator maps to the single target thread. If the target is multi-threaded, the SoC designer must define the mapping between each initiator thread and one of the target's threads. Reverse mapping occurs in the response network with the response on the same initiator thread on which the corresponding request was launched. Thread mapping can take place at agents and within pipeline points.

Pipeline points are subdivided into register points so that each register point represents a single initiator or target core. The breakdown of pipeline points into register points and the placement of the actual mapping point from initiator to target threads and back reduces overall buffering.

Because some multi-threaded initiator cores do not need the full capability of independent resources and flow control for each thread, SonicsLX supports thread collapsing at the initiator socket. For example, an initiator core may exhibit more concurrency at its interface (more threads) than an application can exploit in its thread map, or the initiator implementation may fail to ensure that its threads cannot block one another. In such cases, the ability to merge threads immediately at the entry point to the SonicsLX Interconnect can reduce the internal overhead needed without degrading

performance. SonicsLX allows configuration of the initiator agent to perform input thread collapsing as static N-to-1 mapping. In a similar manner, SonicsLX target agents may be configured to perform thread collapsing in the response path.

Bandwidth

The maximum bandwidth between an initiator and a target depends on the type of traffic and the components along the path. The type of traffic affects how the request and response networks are utilized, while the type of components along the path and how they are configured determine how many request and response transfers can be processed in a unit of time and the overall bandwidth that can be achieved.

The absolute maximum frequency supported by SonicsLX is specific to the targeted process. SonicsLX further limits the maximum frequency because of the multiple pipeline stages that its internal logic paths employ. The logic delay remaining in the slowest of these stages, including flip-flop and clock delays, determines the maximum operating frequency.

SonicsLX can be configured with a data width of 32 or 64 bits depending on what is necessary for an application, independent of the data width of any of the connected IP cores. Typical performance is on the order of 1.6 GBytes/sec per path, assuming a data width of 64-bit wide and conservative clock rate of 200 MHz. SonicsLX employs split packetized transactions that allow some concurrent use of the request and response paths. Threading maximizes the use of paths by permitting some connections to operate while other connections are temporarily blocked.

Since the crossbar topology further enables concurrent traffic, the SonicsLX bandwidth scales by the degree of concurrency. The actual bandwidth is the clock rate multiplied by the data path width, multiplied by the ratio of concurrent read/writes resulting from packetized transactions (a factor greater than 1 but less than 2) and the number of concurrent paths. Maximum bandwidth to a particular target may be reduced if there are

inadequate outstanding requests to cover round-trip latency or by the need to share a link or target among multiple connections.

Latency

Latency is a function of the distance between initiator and target cores, the clock rates of the cores, and whether clock rate conversion is needed between the cores. Latency is also affected by the amount of translation and arbitration required between the initiator and target. SonicsLX can perform simple translations on transactions to maintain semantic equivalence and to permit protocol conversion among the supported interface specifications, including endianness-aware data width conversion and simple address offset translation. SonicsLX arbitration mechanisms then resolve cases where multiple incoming transactions from different initiators address a common target core. The minimum latency along a request or response path between initiator and target is the sum of the minimum latency of the SonicsLX components along that path. The minimum latency of a component depends on its configuration.

Arbitration

The SonicsLX interconnect performs arbitration at all points of contention to resolve conflicts. Crossbar independent arbitration occurs for each target (requests) and each initiator (responses). Arbitration also occurs when an exchange exits to a pipeline point in either the request or response direction.

On the request side, arbitration is performed at transaction (burst) boundaries. If the target supports limited burst lengths, initiator bursts can be broken into smaller bursts. SonicsLX provides QoS modes that can be configured to govern the arbitration mechanism. Response arbitration uses a least-recently-served policy between the branches of each arbitration point, favoring the branch that has been without service for the longest time. Response arbitration is performed at transfer (word) boundaries.

Power Management

Fine and Coarse-grained clock gating mechanisms to reduce reduce idle and active power levels. Fine-grained clock gating can be used to remove the clock from those portions of the interconnect that are currently inactive. Coarse-grained power management uses power control logic external to the SonicsLX interconnects that coordinates power and clock-control state transitions. Each SonicsLX instance provides a single power management interface for the entire interconnect. Coarse-grained power management turns each SonicsLX instance into an explicitly managed power region. Power is managed by removing the clock or supply voltages from the entire interconnect.

The external power control logic and SonicsLX interact through a handshake protocol of power control request and acknowledgement signals. Power management interfaces at each core socket allow each socket's activity status to be observed, indicating whether requests are still pending (for initiator agents) or are waiting to be sent to the target (for target agents). Such activity status signals can be used to help coordinate activity-dependent power management. For example, the activity status signal can be used to let initiator cores know when all requests (including posted writes) are completed or wake up targets (or other SonicsLX instances) that are currently powered down.

Quality of Service (QoS)

QoS mechanisms impose selective flow control of multiple incoming threads to the target allowing control of latency and bandwidth on a per-target and per-thread basis.

Priority arbitration QoS mode governs the arbitration policy of points within cross bar and determine the types of thread arbitration priority levels that are available at the target. At a minimum, all initiating threads are non-blocking with respect to other initiating threads accessing targets within SonicsLX. Each target may be configured in one of two QoS modes, and each target

thread may be assigned a QoS arbitration priority level as allowed by the target's QoS mode:

Weighted Fairness

All threads going into the target are assigned a priority level of best-effort and are given access to the target according to their assigned weights.

Priority

Arbitration priority levels are either priority or best-effort and are fixed for each thread. Priority level threads share bandwidth with each other but always win in arbitration over best-effort threads. The bandwidth available to best-effort threads depends on the priority thread traffic and may be zero.

Access Protection

SonicsLX provides an access protection mechanism to designate protection regions within the address space of specified targets. The mechanism is static, with protection region sizes and location fixed at configuration generation. Initiator uses a single bit as indication of the transaction to be secure or non-secure.

Configuration Options

The configuration options for SonicsLX are structural (design-time) options. Structural configuration options must be defined as the interconnect is being created and are then fixed in the hardware.

Structural Configuration Options

The following provides an overview of the various SonicsLX parameters that can be configured as structural configuration options. Specific configurable SonicsLX mechanisms are first identified, followed by the configurable parameters per each core socket, exchange, register point, initiating or target thread, and connection, and finally the configurable parameters associated with sideband signaling.

Per socket: Option for OCP and AHB configuration, Timeout protection, Error logging, outstanding requests, activity status flags, inband and out of band error conversion, Address fill-ins for initiators, initiator ID fill-ins, flop options, response buffering, thread collapsing, QoS modes, error steering and memconID are all configurable per core socket.

Per exchange:, link widths and data paths.

Per register point: register depth

{ target thread: Arbitration priority level