

# BUK9K52-60E

Dual N-channel TrenchMOS logic level FET

23 July 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Dual logic level N-channel MOSFET in a LFPAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

### 1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

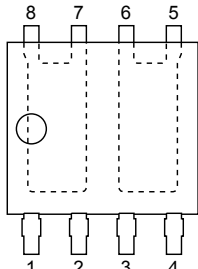
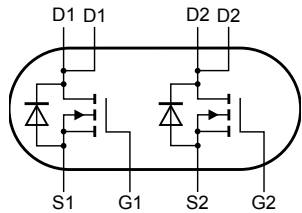
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	60	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	17	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	32	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	47.3	55	m $\Omega$
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	2.3	-	nC



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p><b>LFPAK56D (SOT1205)</b></p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9K52-60E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 4. Limiting values

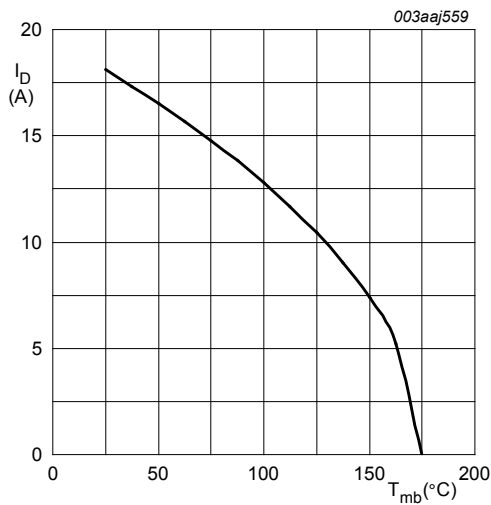
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega; T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
$V_{GS}$	gate-source voltage		-10	10	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}; \text{Fig. 1}$	-	17	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V}; \text{Fig. 1}$	-	12	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Fig. 4}$	-	68	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	32	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode FET1 and FET2</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	17	A

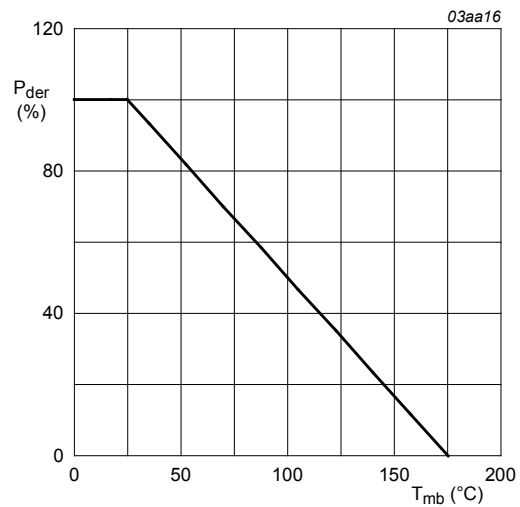
Symbol	Parameter	Conditions	Min	Max	Unit
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25^\circ C$	-	68	A
<b>Avalanche Ruggedness FET1 and FET2</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 18.1 A$ ; $V_{sup} \leq 60 V$ ; $V_{GS} = 10 V$ ; $T_{j(init)} = 25^\circ C$ ; <a href="#">Fig. 3</a>	[1][2]	-	11 mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 10V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

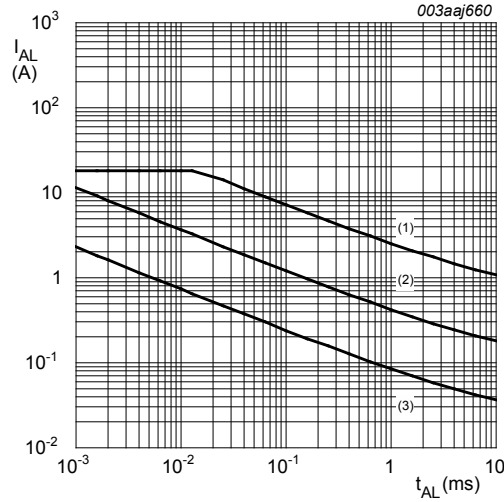


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse;  $T_j = 25^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 175^\circ\text{C}$ .
- (3) Repetitive.

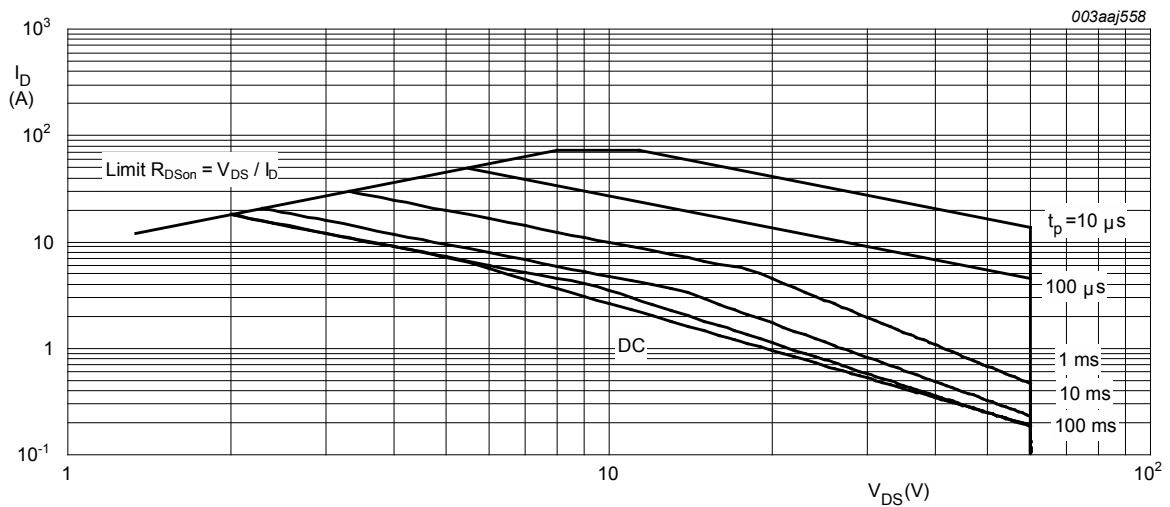


Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	4.68	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W



Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	47.3	55	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	106.9	124.3	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	41.4	49	m $\Omega$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14; Fig. 15	-	10	-	nC
$Q_{GS}$	gate-source charge		-	1.1	-	nC
$Q_{GD}$	gate-drain charge		-	2.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 5\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14; Fig. 15	-	0.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5\text{ A}; V_{DS} = 48\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14; Fig. 15	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	544	725	pF
$C_{oss}$	output capacitance		-	62	74	pF
$C_{rss}$	reverse transfer capacitance		-	40	55	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 48\text{ V}; R_L = 10\text{ }^\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$	-	3.7	-	ns
$t_r$	rise time		-	3.2	-	ns
$t_{d(off)}$	turn-off delay time		-	15.2	-	ns
$t_f$	fall time		-	8.1	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 48\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	17.7	-	ns
$Q_r$	recovered charge		-	11.6	-	nC

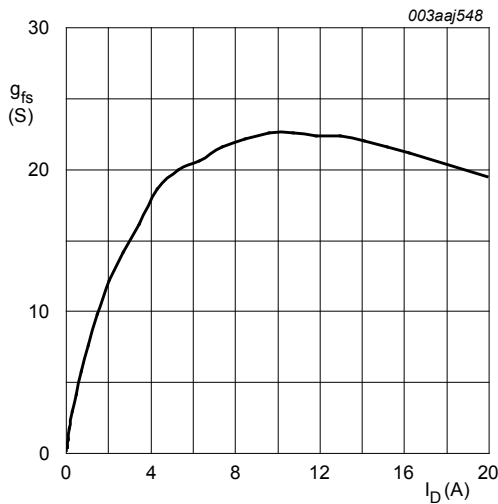


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$$

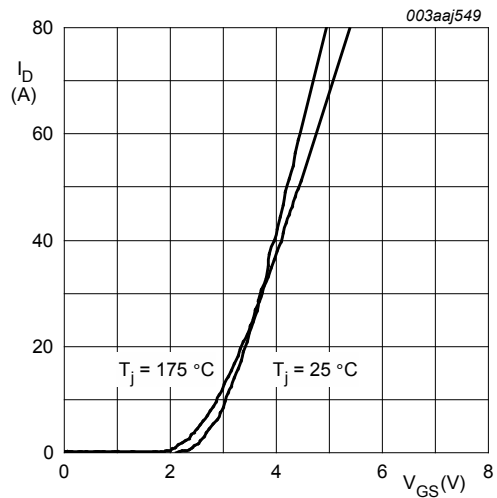


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DS(on)}$$

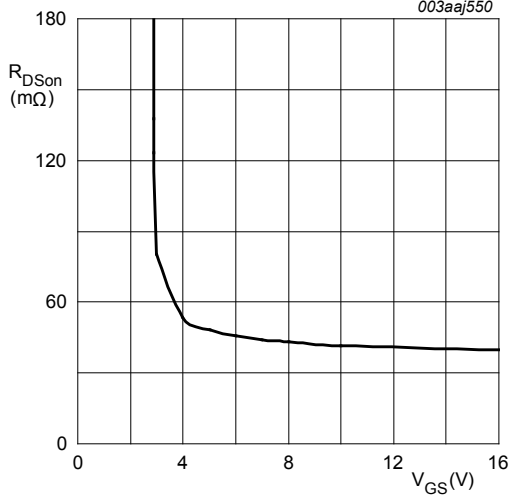


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 5 A$

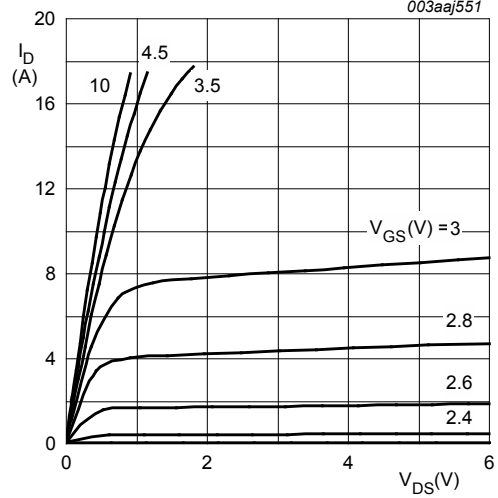


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

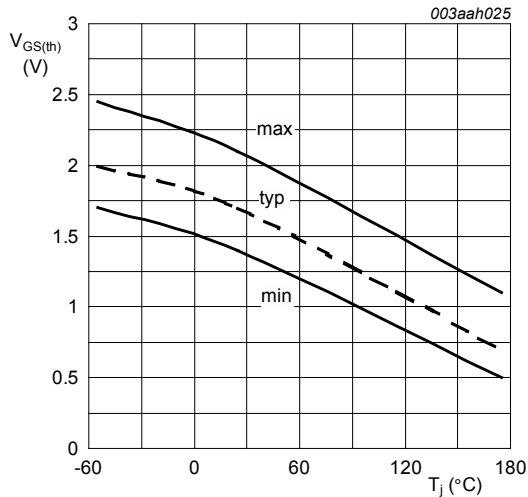


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 mA; V_{DS} = V_{GS}$

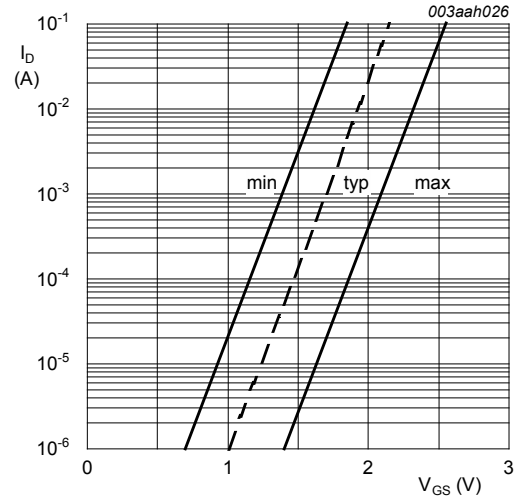


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5 V$

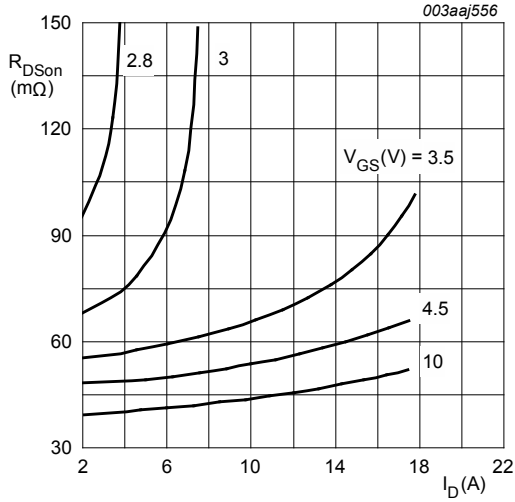


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

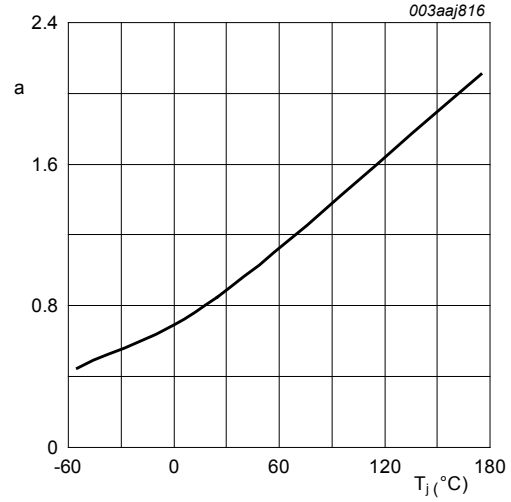


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

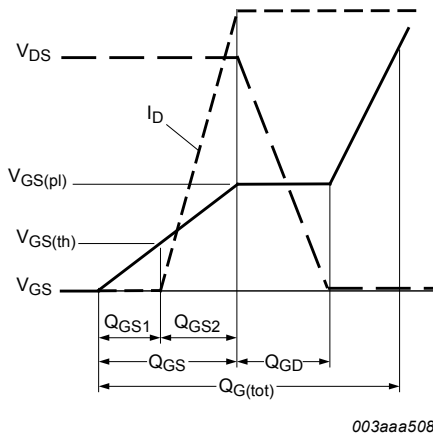


Fig. 14. Gate charge waveform definitions

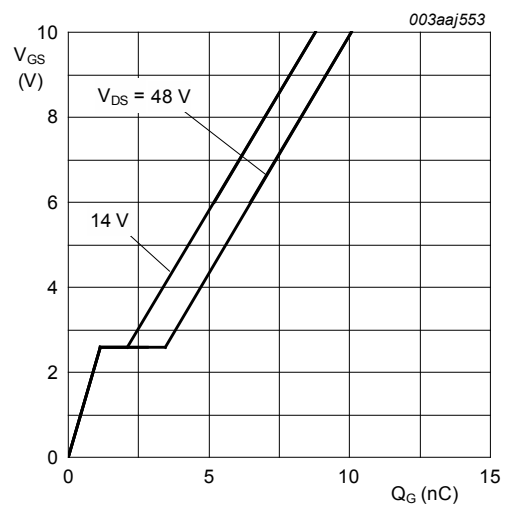


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

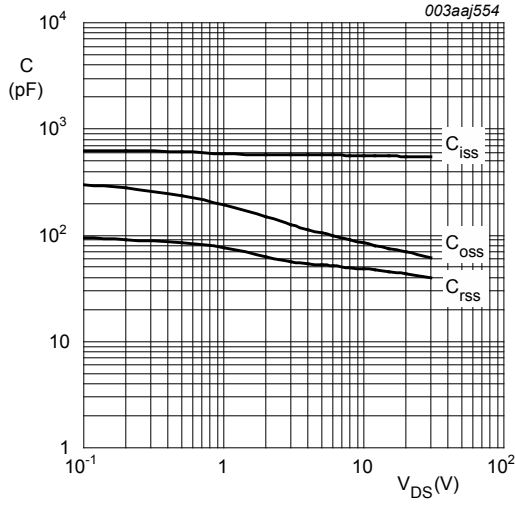


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

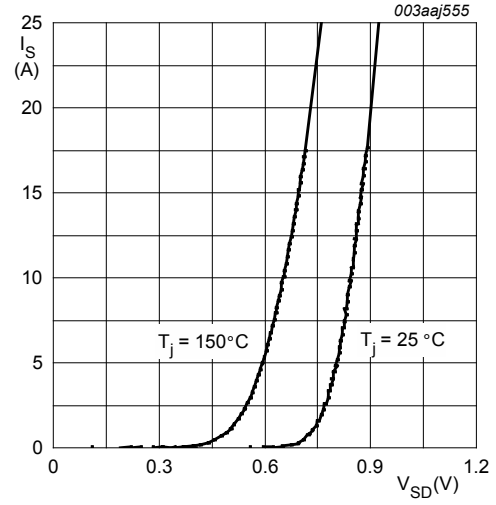
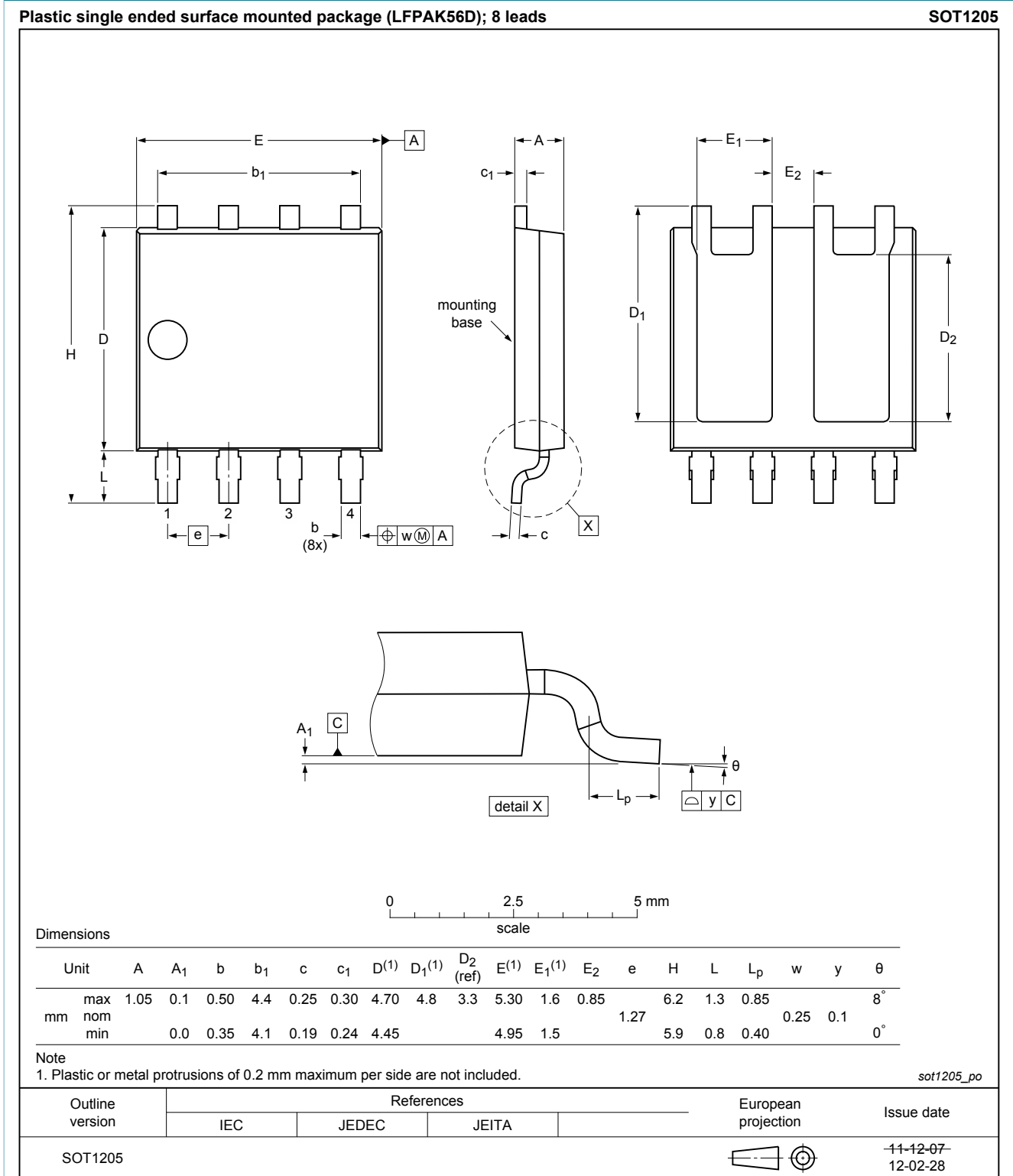


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0\text{ V}$$

**7. Package outline**



**Fig. 18. LPAK56D (SOT1205)**

## 8. Legal information

### 8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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