

CRD89C51RE

8-Bit Microcontroller with 128KB ISP Flash, 1KB RAM, TWSI & SPWM

Product List

CRD89C51RE-25

25MHz 128KB internal flash MCU with ISP

CRD89C51RE-40

40MHz 128KB internal flash MCU with ISP

Description

The CRD89C51RE 8-bit microcontroller features 128KB of on-chip In-System/Application Programmable (ISP) flash memory and 1KB of RAM. A derivative of the 8052 microcontroller family, the CRD89C51RE is a pin-compatible drop-in replacement for industry standard 8051s.

The device includes a TWSI (2-wire serial bus interface) that is compatible with the standard VESA DC/CI and a 4-channel SPWM (specific pulse width modulator). On-chip, expanded RAM can be easily accessed via 'bank mapping direct addressing mode'.

The CRD89C51RE is available in a 40-pin PDIP package with up to 32 general purposes I/Os (GPIO) and 44-pin PLCC/QFP packages with up to 36 GPIOs. The 128KB flash can be programmed in either parallel or serial interface mode using the on-chip ISP.

Its advanced hardware features and powerful instruction set make the CRD89C51RE a versatile and cost effective controller for applications that require a large amount of program/data memory with nonvolatile data storage and/or code/field based firmware upgrade capability coupled with comprehensive peripheral support.

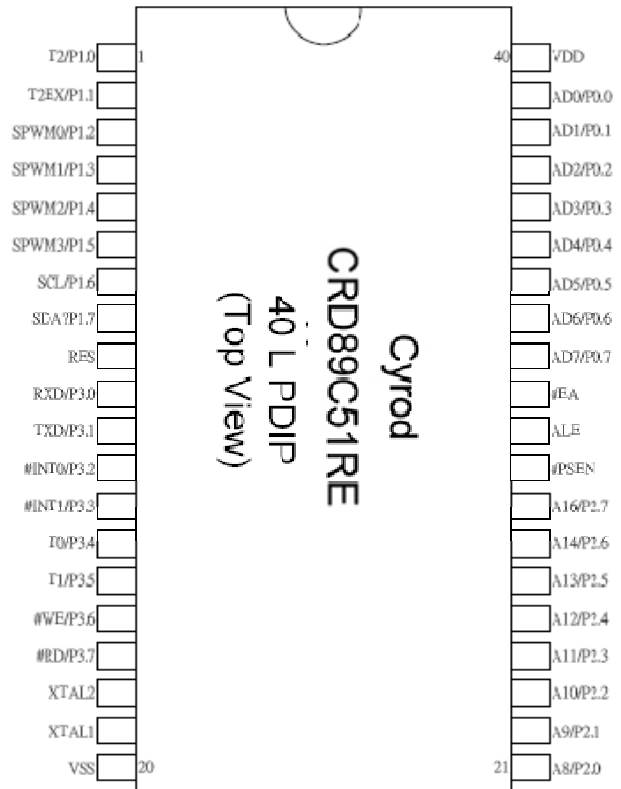
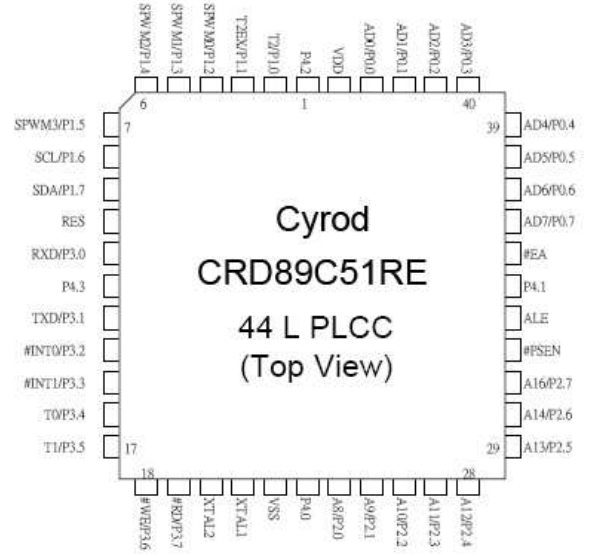
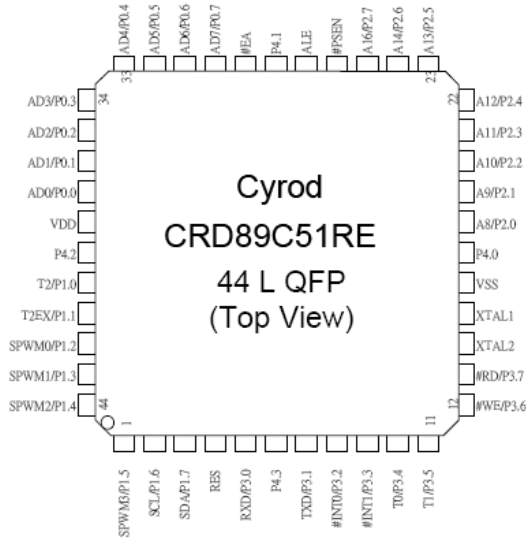
Features

- 128K byte on chip program ISP/IAP flash
- Default ISP service program pre-loaded
- 8051 compatible
- Code protection function
- Working Voltage: 4.5V through 5.5V
- 12 clocks per machine cycle
- TWSI compliant with VESA DDC 2B/2Bi/2B+ standard
- 4 SPWMs
- 1024 bytes on-chip RAM
- Three 16-bit Timers/Counters
- Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O port for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Industrial Level
- Direct and Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- Serial I/O port
- Power save modes: Idle Mode and Power Down Mode
- Low EMI (inhibit ALE)
- User ISP service program option for code size N*512 byte (N=0 to 8) (1K to 4K)

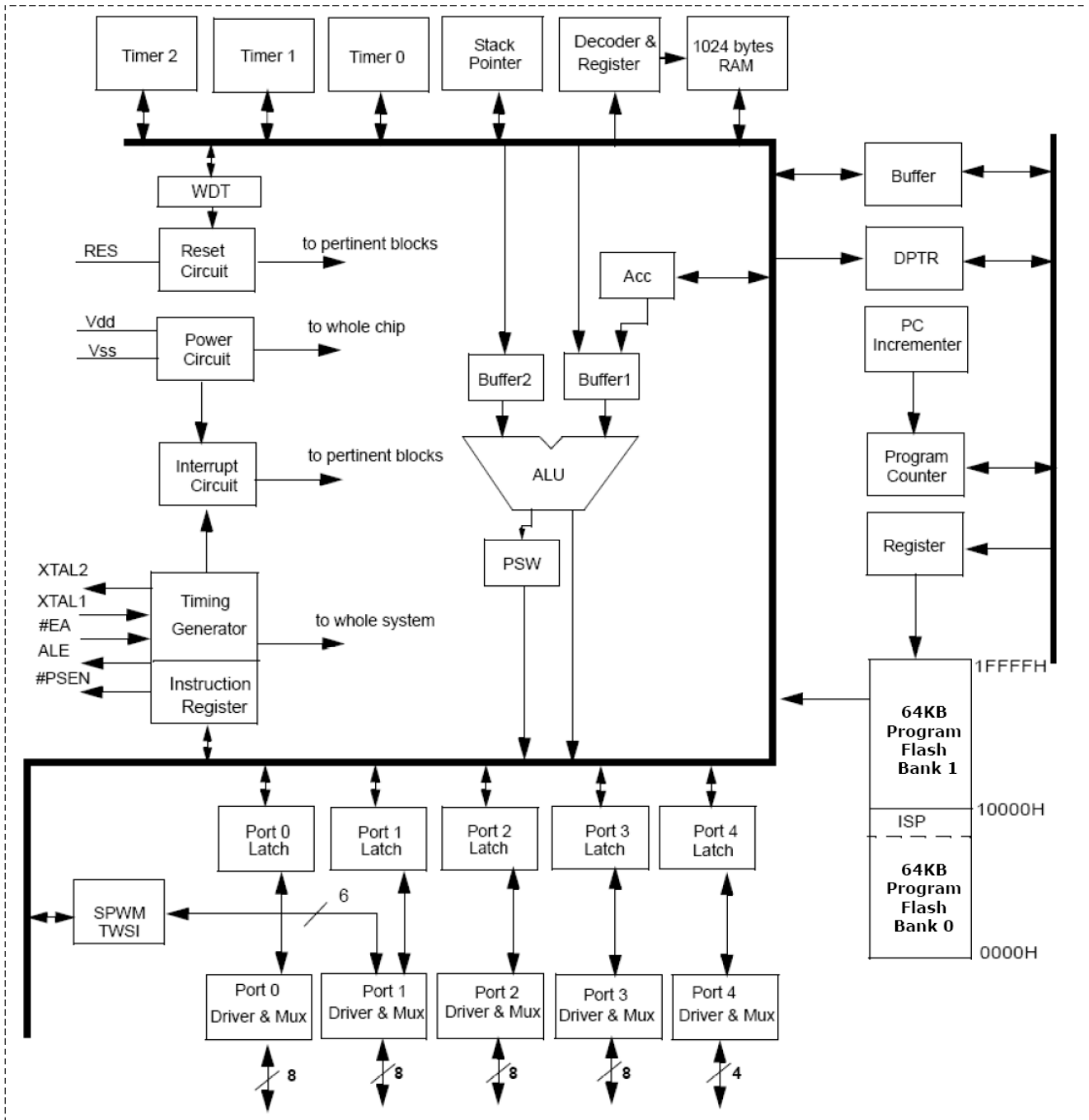
Ordering Information

CRD89C51RE-25-P 128KB Flash with ISP, 25 MHz 40-PDIP
CRD89C51RE-25-J 128KB Flash with ISP, 25 MHz 44-PLCC
CRD89C51RE-25-Q 128KB Flash with ISP, 25 MHz 44-QFP
CRD89C51RE-40-P 128KB Flash with ISP, 40 MHz 40-PDIP
CRD89C51RE-40-J 128KB Flash with ISP, 40 MHz 44-PLCC
CRD89C51RE-40-Q 128KB Flash with ISP, 40 MHz 44-QFP

Pin Configuration



Block Diagram



Pin Description

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0/T2		i/o	bit 0 of port 1 & timer 2 clock out
2	41	3	P1.1/T2EX		i/o	bit 1 of port 1 & timer 2 control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3/SPWM0		i/o	bit 3 of port 1 & SPWM channel 0
5	44	6	P1.4/SPWM1		i/o	bit 4 of port 1 & SPWM channel 1
6	1	7	P1.5/SPWM2		i/o	bit 5 of port 1 & SPWM channel 2
7	2	8	P1.6/SCL		i/o	bit 6 of port 1 & TWSI Bus Clock
8	3	9	P1.7/SDA		i/o	bit 7 of port 1 & TWSI Bus Data
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR		i/o	bit 6 of port 3 & ext. memory write
17	13	19	P3.7/#RD		i/o	bit 7 of port 3 & ext. mem. Read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN		o	program storage enable
30	27	33	ALE		o	address latch enable
31	29	35	#EA	L	I	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of port 4

Special Function Register (SFR)

Addresses \$80 to \$FF of the SFR address space can only be accessed in direct addressing mode. The following table lists the CRD89C51RE SFRs, which are identical to industry standards 8051 SFRs, as well as the CRD89C51RE Extension SFRs.

Special Function Register (SFR) Memory Map

\$F8										\$FF
\$F0	B				ISPFAH	ISPFAL	ISPFD	ISPC		\$F7
\$E8										\$EF
\$E0	ACC									\$E7
\$D8	P4									\$DF
\$D0	PSW									\$D7
\$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2				\$CF
\$C0	TWSIS	TWSIA	TWSIC1	TWSIC2	TWSITxD	TWSIRxD				\$C7
\$B8	IP	IP1							SCONF	\$BF
\$B0	P3									\$B7
\$A8	IE	IE1	IFR							\$AF
\$A0	P2				SPWMC	SPWMD0	SPWMD1	SPWMD2	SPWMD3	\$A7
\$98	SCON	SBUF			P1CON				WDTC	\$9F
\$90	P1								WDTKEY	\$97
\$88	TCON	TMOD	TL0	TL1	TH0	TH1				\$8F
\$80	P0	SP	DPL	DPH		RCON			PCON	\$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for the CRD89C51RE.

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	RCON	00H	RAMS7	RAMS6	RAMS5	RAMS4	RAMS3	RAMS2	RAMS1	RAMS0
97H	WDTKEY	00H	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0
9BH	P1CON	**0000**	TWSISDAE	TWSISCLE	SPWME3	SPWME2	SPWME1	SPWME0		
9FH	WDTC	0*0**000	WDTE		CLEAR				PS1	PS0
A3H	SPWMC	*****00							SPFS1	SPFS0
A4H	SPWMD0	00H	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
A5H	SPWMD1	00H	SPWMD14	SPWMD13	SPWMD12	SPWMD11	SPWMD10	BRM12	BRM11	BRM10
A6H	SPWMD2	00H	SPWMD24	SPWMD23	SPWMD22	SPWMD21	SPWMD20	BRM22	BRM21	BRM20
A7H	SPWMD3	00H	SPWMD34	SPWMD33	SPWMD32	SPWMD31	SPWMD30	BRM32	BRM31	BRM30
BFH	SCONF	0***0000	WDR				BANK	ISPE	OME	ALEI
C0H	TWSIS	0000*100	RXIF	TXIF	TFIF	NAKIF		RXAK	MASTER	TXAK
C1H	TWSIA	10100000	TWSIA7	TWSIA6	TWSIA5	TWSIA4	TWSIA3	TWSIA2	TWSIA1	EXT ADDR
C2H	TWSIC1	0***0001	TWSIE				Bus Busy	TWSIFS2	TWSIFS1	TWSIFS0
C3H	TWSIC2	00H	Match	SRW			RESTART			MRW
C4H	TWSITxD	FFH	TWSITxD7	TWSITxD6	TWSITxD5	TWSITxD4	TWSITxD3	TWSITxD2	TWSITxD1	TWSITxD0

C5H	TWSIRxD	00H	TWSIRxD7	TWSIRxD6	TWSIRxD5	TWSIRxD4	TWSIRxD3	TWSIRxD2	TWSIRxD1	TWSIRxD0
A9H	IE1	00						ETWSI		
AAH	IFR	00						TWSIF		
BAH	IP1	00							PTWSI	
C8H	T2CON	00H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9H	T2MOD	*****00	*	*	*	*	*	*	T2OE	DCEN
D8H	P4	****1111					P4.3	P4.2	P4.1	P4.0
F4H	ISPF AH	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	ISPF AL	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	ISPF D	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	ISPC	0*0***00	START		FAU0				F1	F0

Extension Function Description

1. Memory Structure

The CRD89C51RE has an 8051-based hardware core with 768 bytes of expanded data RAM and 128 Kbytes of Flash. It has a standard 8051 memory structure in addition to a proprietary external RAM structure.

1.1 Program Memory

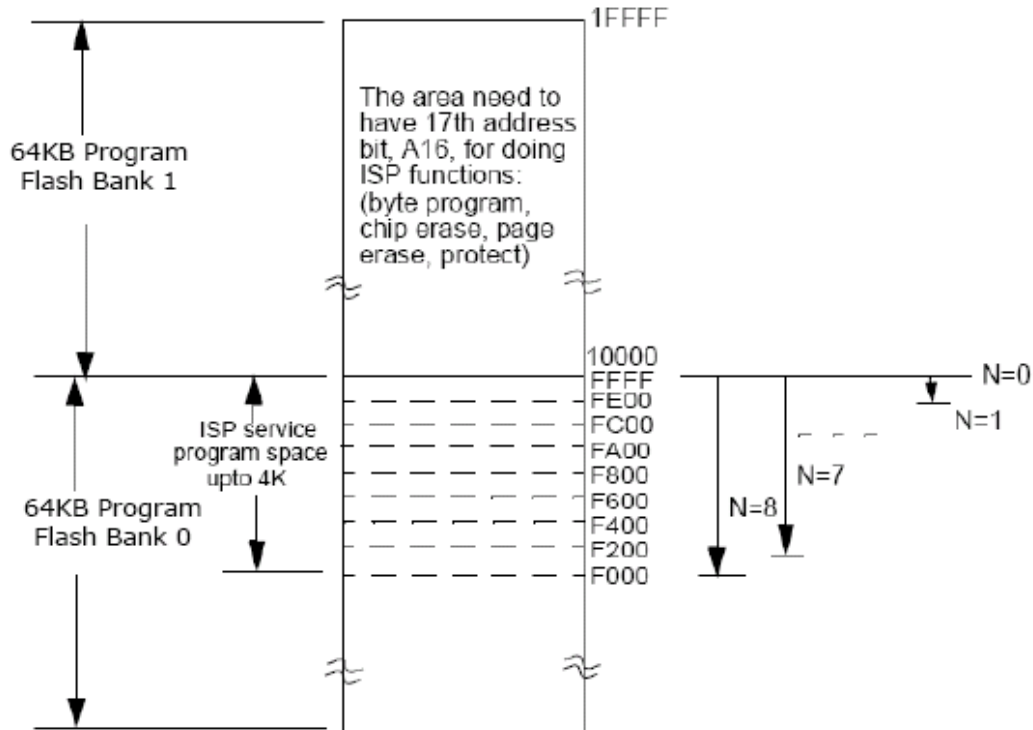
The CRD89C51RE has 128KB of ISP flash memory, 64KB located on bank0 and 64KB located on bank1. On bank0 there is space available for up to 4KB of user-specific ISP firmware. On the CRD89C51RE version, 1KB of the bank0 flash memory is reserved for the default Cyrod ISP service program. The address range for bank0 is \$0000 to \$FFFF.

For the CRD89C51RE versions, the address range for the ISP service program is \$F000 to \$FFFF. The user specified ISP service program size can be partitioned as N blocks of 512 bytes (N=0 to 8). When N=0, there is no ISP service program space available and the total 128K byte memory is allocated as program memory. When N=1 memory address \$FE00 to \$FFFF is reserved for the user defined ISP service program (512 bytes). When N=2, memory address \$FC00 to FFFF is reserved for the user defined ISP service program (1024 bytes), etc. Value N can be set and programmed into CRD89C51RE by the writer.

For the CRD89C51RE version, there is a default Cyrod ISP service program installed in the memory at address \$FC00 to FFFF (1024 bytes).

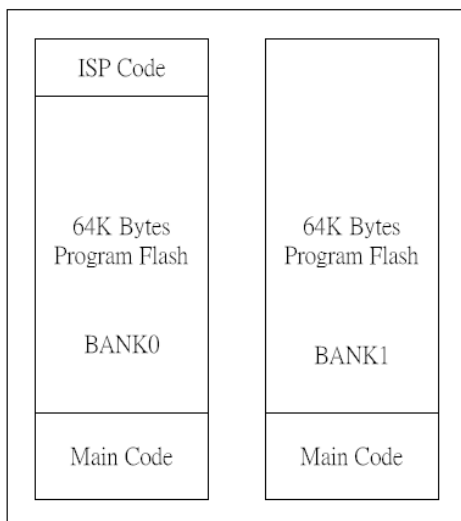
1.1.1 Program Code Security

MOVC instructions executed from the external program memory space will be unable to fetch internal code from the on-chip program memory after the chip is protected on the writer.



Note: The single flash block address structure for doing the ISP function to the on-chip data flash as well as program ROM flash.

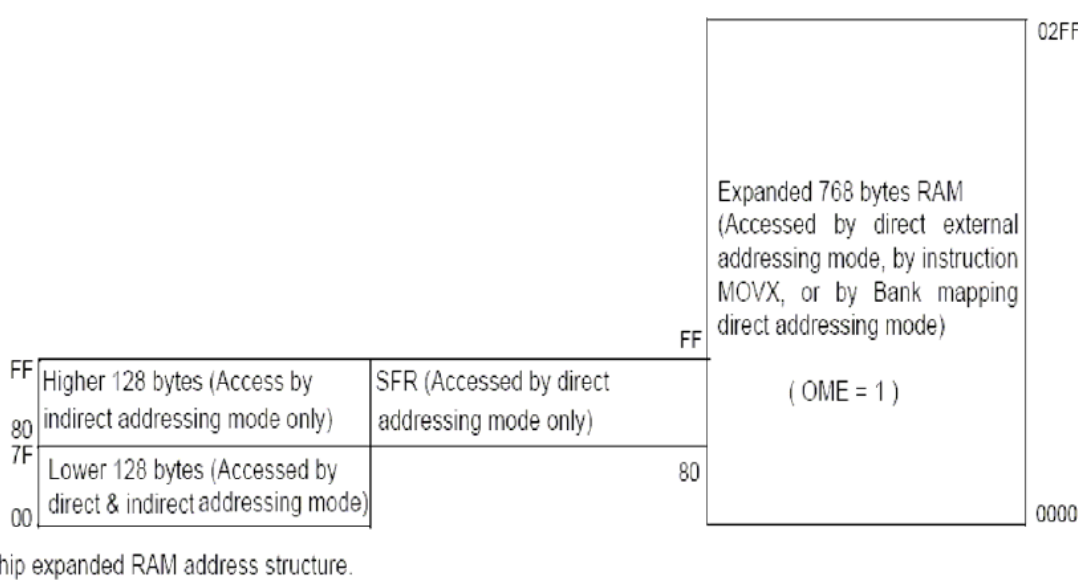
BANK	128K Program Flash
0	BANK0 (64K Flash)
1	BANK1 (64K Flash)



1.2 Data Memory

The CRD89C51RE has 1KB on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed using external memory addressing via the MOVX instruction. (See section on MOVX or by ‘bank mapping direct addressing mode’ on page 9).

User can use MOVX instruction to access internal RAM or external memory by setting OME. Different OME settings will map to different memory blocks.



OME	address of MOVX below 768	address of MOVX over 768
0	external memory	external memory
1	internal RAM	external memory

1.2.1 Data Memory - Lower 128 byte (\$00 to \$7F)

Data Memory \$00 to \$FF is the same as on standard 8052 MCUs. The address \$00 to \$7F can be accessed in both direct and indirect addressing modes.

Address \$00 to \$1F is a register area.

Address \$20 to \$2F is a memory bit area.

Address \$30 to \$7F is for general memory.

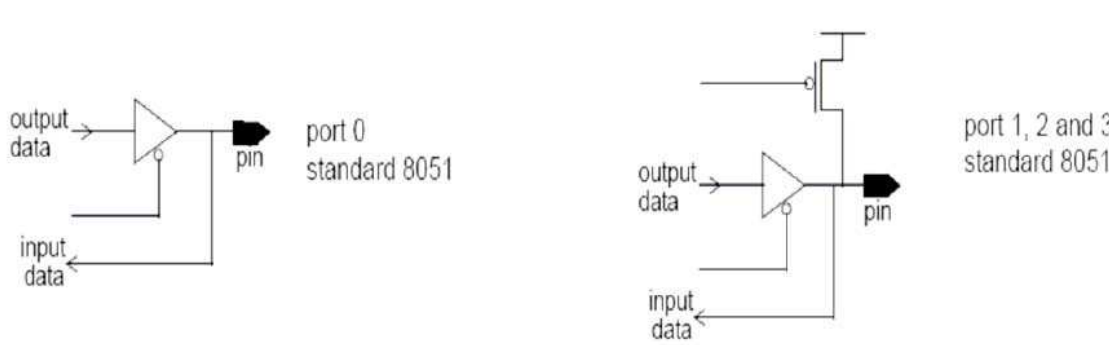
1.2.2 Data Memory - Higher 128 byte (\$80 to \$FF)

Address \$80 to \$FF can be accessed in indirect addressing mode or in bank mapping direct addressing mode. Address \$80 to \$FF is the data area.

1.3 I/O Pin Configuration

Ports 1, 2 and 3 are identical to the standard 8051 ports and have internal pull-up resistors. Port 0 has an open-drain output. Each I/O pin can be used independently as an input or an output. For I/O ports to be used as input, the port bit latch must contain a '1', which turns off the output driver FET. Then the port 1, 2 and 3 port pins are pulled high by a weak internal pull-up, and can be pulled low by an external source. Port 0 has an open-drain output which means its pull-ups are not active during normal port operation. Writing a '1' to the port 0 bit latch will cause the bit to float so that it can be used as a high-impedance input.

Port 4 used as GPIO will operate the same way as ports 1, 2 and 3.



2. Port 4 for PLCC or QFP package:

Bit-addressable port 4 is available with PLCC and QFP packages. Port 4 has only 4 pins and its port address is located at 0D8H. Port 4 functions like ports 1, port 2 and port 3.

bit-7

bit-0

	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

3. In-System Programming (ISP) Function

The CRD89C51RE can generate flash control signals via internal hardware circuitry. The CRD89C51RE provides the internal flash control signals required to do flash programming / chip erase / page erase / protect functions and has an on chip charge pump that develops the necessary flash programming voltage to accomplish this. The device comes with a pre-loaded ISP service program supplied by Cyrod. This program uses the top 1KB of the 128KB of flash program memory.

The user can also elect to develop their own ISP service program and overwrite the factory installed 1KB of ISP code.

3.1 ISP Service Program

All ISP service programs (user defined or the Cyrod default) reside in the ISP service program space. This space is able to accommodate various sizes of code allowing the user (if they so choose) the flexibility to design ISP firmware solutions between 512 B to 4KB. The benefit to the user is that they can customize the device's communication protocol between CRD89C51RE and host device which will output data to the CRD89C51RE.

Otherwise, users can make use of the pre-installed ISP service program (as indicated above uses 1KB of the flash memory space).

The ISP service program can be initiated under CRD89C51RE active or idle mode. It cannot be initiated under power down mode.

3.2 Lock Bit (N)

The Lock Bit N has two functions: one is to define the ISP service program size and the other is to lock the ISP service program space from the flash erase function. The address range for the ISP service program is \$F000 to \$FFFF. It is divided into blocks of N*512 bytes (N=0 to 8). When N=0 the ISP function is disabled and all of 128K byte flash memory can be used as program memory. When N=1 there is a reserved ISP service program area that occupies 512 bytes leaving a balance of 127.5K bytes of flash memory that can be used as program memory. When N=2 there is 1KB of ISP code space used and a balance of 127KB of flash program area available (this is the configuration that the CRD89C51RE is shipped). The maximum ISP service program allowed is 4K byte for N=8. Under this configuration, the usable program memory space is 124K byte.

If the user will use the Cyrod ISP code no action is required except to leave N=2 unaltered. If the user is to develop their own ISP service program, they must determine the size of their ISP code. After N is determined, the CRD89C51RE will reserve the ISP service program space downward from the top of the program address \$FFFF. The start address of the ISP service program is located at \$Fx00 while x is an even number, as determined by the lock bit N. Please see page 7, program memory diagram, for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The chip erase function can erase all of the flash memory space including 128KB program flash, except for the locked ISP service program space.

3.3 Program the ISP Service Program

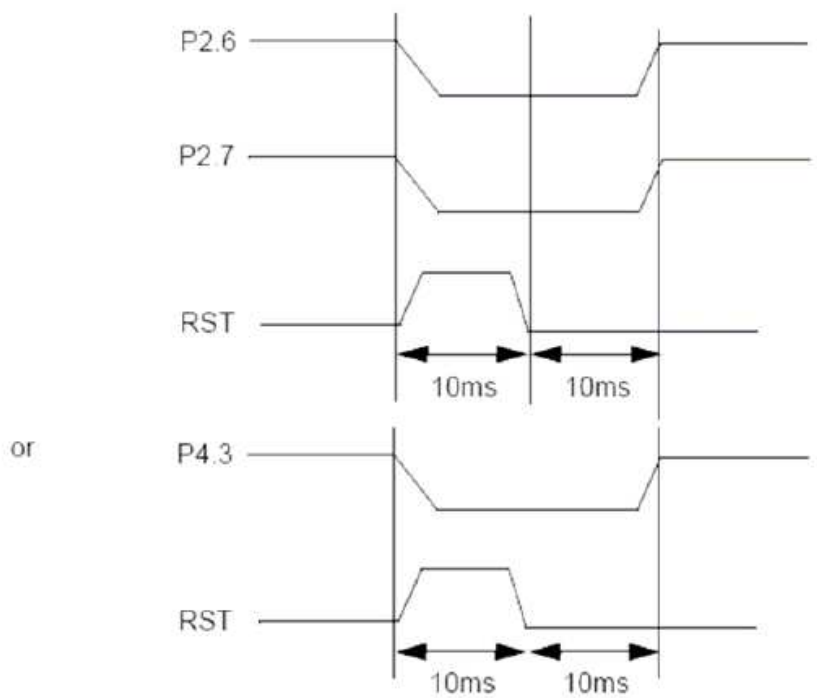
After the Lock Bit N is set and the ISP service program has been loaded, the ISP service program memory is protected (locked) automatically. The lock bit N has its own program/erase timing different from that of the flash memory program/erase timing. This allows the locked ISP service program not to be erased by the flash erase function. If the user needs to erase the locked ISP service program, they can accomplish this by writing directly to the device. The ISP service program cannot be changed in the system.

3.4 Initiate ISP Service Program

To initiate the ISP service program the program counter (PC) must be loaded with the start address of ISP service program. There are three ways to do this:

- (1) Blank reset. Hardware reset with first flash address blank (\$0000=#FFH) will load the PC with start address of ISP service program.
- (2) Execute a 'JUMP' instruction that can load the start address of the ISP service program to PC.
- (3) Use a hardware setting. The user can force the CRD89C51RE to enter the ISP service program by setting P2.6, P2.7 "low" or P4.3 "low" during a hardware reset period. In application system design, the user should take care of the setting of P2.6, P2.7 and P4.3 during reset periods to prevent the CRD89C51RE from unintentionally entering the ISP service program.

Entering the ISP service program by hardware setting:



The user can use a general 8051 UART function to initiate the ISP service program. After the ISP service program is executed, the user needs to reset the CRD89C51RE, either by a hardware reset or by a WDT, or by a jump to the address \$0000 to re-start the firmware program.

3.5 ISP Registers - System Control Register (SCONF, \$BF)

	bit-7							bit-0
	WDTE	Unused	Unused	Unused	BANK	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value:	0	*	*	*	0	0	0	0

The bit 2 (ISPE) of SCONF is the ISP enable bit. The user can enable overall ISP function by setting the ISPE bit to 1. Setting the ISPE bit to 0 will disable the overall ISP function. The function of ISPE behaves like a security key. The user can disable the overall ISP function to prevent the software program being erased accidentally.

3.6 ISP Registers: ISPF AH, ISPF AL, ISPF D and ISPF C registers

The ISPF AH & ISPF AL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPF AH & ISPF AL registers overlays with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect. When performing byte program ISP function, the content of ISPF D register will be programmed to the flash address, which is indicated by ISPF AH and ISPF AL registers.

ISP Registers- Flash Address-High Register (ISPF AH, \$F4)

	bit-7							bit-0
	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA15 ~ FA8: flash address-high for ISP function

ISP Registers - Flash Address-Low Register (ISPF AL, \$F5)

	bit-7							bit-0
	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA7 ~ FA0: flash address-low for ISP function

The ISPF AH & ISPF AL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPF AH & ISPF AL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISP Registers - Flash Data Register (ISPF, \$F6)

	bit-7							bit-0
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FD7 ~FD0: flash data for ISP function

The ISPF provide the 8-bit data for ISP function

ISP Registers -Flash Control Register (ISPC, \$F7)

	bit-7							bit-0
	START	Unused	FAUO	Unused	Unused	Unused	ISPF1	ISPF0
Read / Write:	R/W	-	R/W	-	-	-	R/W	R/W
Reset value:	0	*	0	*	*	*	0	0

ISPF [1:0]: ISP function select bit

ISPF [1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase (512Byte)
11	Chip erase

START: ISP function start bit

- = 1: start ISP function which indicated by bit 1, bit 0 (ISPF1, ISPF0)
- = 0: no operation

FAUO: 64K program Flash bank select bit (only in ISP mode used)

- = 1: selected 64K bank1 flash
- = 0: selected 64K bank0 flash

Note: The START bit is read-only by default. Software must write three specific values 55H, AAH and 55H sequentially to the ISPF register to enable the START bit write attribute. That is:

```
MOV ISPF, #55H
MOV ISPF, #0AAH
MOV ISPF, #55H
```

Any attempt to set the START bit will not be allowed without the procedure above. After the START bit set to 1 then the CRD89C51RE hardware will latch the flash address and the data bus and hold the program counter until the START bit is reset to 0 when the ISP function is finished. The program counter (PC) will point to next instruction after the START bit is reset to 0. The user does not need to check the START bit status by software.

To perform byte program/page erase ISP function, the user needs to first specify the flash address. When performing the page erase function, the CRD89C51RE will erase the entire page at the flash address indicated by ISPF AH & ISPF AL registers located within the page. For example:

- Flash address: \$XYMN
- Page erase function will erase from \$XY00 to \$X(Y+1)FF (Y: even number), or
- Page erase function will erase from \$X(Y-1)00 to \$XYFF (Y: odd number)

To perform the chip erase ISP function, the CRD89C51RE will erase all the flash program memory and data flash memory except the ISP service program space if the lock bit N has been configured. To perform chip protect ISP function, all the flash memory will be read #00H.

Example: ISP service program to do the byte program-to-program #22H to the address \$1005H

```
MOV ISPF D, #55H
MOV ISPF D, #0AAH
MOV ISPF D, #55H
MOV 0BFh, #04H ;enable CRD89C51RE ISP function
MOV 0F4h, #10H ;set flash address-high, 10H
MOV 0F5h, #05H ;set flash address-low, 05H
MOV 0F6h, #22H ;set flash data to be programmed, data = 22H
MOV 0F7h, #80H ;start to program #22H to the flash address $1005H
                ;after byte program finished, START bit of FCR will be reset to 0
                ;automatically
                ;program counter then point to the next instruction
```

4. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generates a reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or other electronics discharges which can cause software dead loop or runaway situations. The WDT function can help user software recover from these types of abnormal software conditions.

The WDT is different from Timer0, Timer1 and Timer2 of the general 8051. The WDT reset can be prevented by the user's software periodically clearing the WDT counter. The user's program therefore needs to check the WDR bit of the SCONF register whenever an un-predicted reset occurs. The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway. There is a 250 KHz RC oscillator embedded in chip. Set WDTE = "1" will enable the RC oscillator and the frequency is independent to the system frequency.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when CRD89C51RE been reset, either hardware reset or WDT reset. To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the contents of the 16-bit counter and let the counter re-start to count from the beginning.

4.1 Watch Dog Timer Registers:

Watch Dog Timer Registers - WDT Control Register (WDTC, \$9F)

	bit-7							bit-0
	WDTE	Reserve	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

WDTE : Watch Dog Timer enable bit
 CLEAR : Watch Dog Timer reset bit
 PS[2:0] : Overflow period select bits

PS [2:0]	Overflow Period (ms)
000	2.048
001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.144

Watch Dog Key Register – (WDTKEY, \$97H)

	bit-7							bit-0
	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
Read / Write:	W	W	W	W	W	W	W	W
Reset value:	0	0	0	0	0	0	0	0

By default, the WDTC is read only. User need to write values 1EH, E1H sequentially to the WDTKEY(\$97H) register to enable the WDTC write attribute, That is

```
MOV WDTKEY, # 1EH
MOV WDTKEY, # 0E1H
```

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY(\$97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # 0E1H
MOV WDTKEY, # 1EH
```

Watch Dog Timer Register - System Control Register (SCONF, \$BF)

	bit-7				bit-0			
	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value:	0	*	*	*	0	0	0	0

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened

5. Low EMI Function

The CRD89C51RE allows the user to reduce the EMI emissions by setting bit 0 (ALEI) of SCONF register to “1”. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

6. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module contains a PWM sub module: SPWM (Specific PWM). The SPWM has five 8-bit channels.

6.1 SPWM Function Description:

The 8-bit SPWM channel is composed of an 8-bit register, which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate an equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through the 5-bit SPWM clock speed. The SPFS[1:0] settings of SPWMC (\$A3) register are divided by Fosc to be SPWM clock, $F_{osc}/2^{(SPFS[1:0]+1)}$. The SPWM output cycle frame’s repetition rate (frequency) equals (SPWM clock)/32 which is $[F_{osc}/2^{(SPFS[1:0]+1)}/32$.

6.2 SPWM Registers - P1CON, SPWMC, SPWMD[3:0]

SPWM Registers - Port1 Configuration Register (P1CON, \$9B)

	bit-7						bit-0	
	TWSIDAE	TWSICLE	SPWME3	SPWME2	SPWME1	SPWME0	Unused	Unused
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value:	0	0	0	0	0	0	*	*

TWSIDAE: When the bit set to one ,the corresponding TWSIDA pin is active as TWSIDA function. When the bit reset to zero, the corresponding TWSIDA pin is active as I/O pin. Four bits are cleared upon reset.

TWSICLE: When the bit set to one ,the corresponding TWSICLE pin is active as TWSICLE function. When the bit reset to zero, the corresponding TWSICLE pin is active as I/O pin. Four bits are cleared upon reset.

SPWME[3:0]: When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Four bits are cleared upon reset.

SPWM Registers -SPWM Control Register (SPWMC, \$A3)

	bit-7						bit-0	
	Unused	Unused	Unused	Unused	Unused	Unused	SPFS1	SPFS0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

SPFS[1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

SPFS1	SPFS0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Registers -SPWM Data Register (SPWMD[4:0], \$AC, \$A7 ~\$A4)

	bit-7					bit-0		
	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [2:0]2	BRM [2:0]1	BRM [2:0]0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

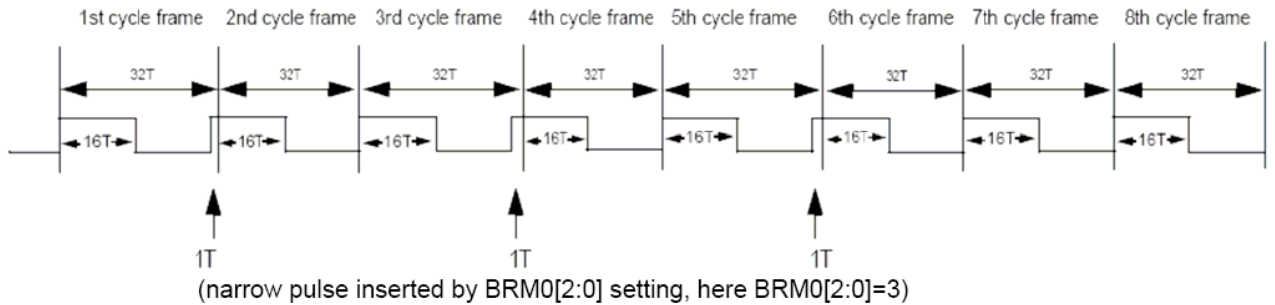
SPWMD[4:0] : content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[2:0] : will insert certain narrow pulses among an 8-SPWM-cycle frame

N = BRM[2:0]	Number of SPWM cycles inserted in an 8-cycle frame
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Example of SPWM timing diagram:

```
MOV SPWMD0 , #83H           ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM[2:0] = 3
MOV P1CON , #08H          ; Enable P1.3 as SPWM output pin
```



SPWM clock = $1 / T = F_{osc} / 2^{(SPFS[1:0]+1)}$
 The SPWM output cycle frame frequency = $SPWM \text{ clock} / 32 = [F_{osc}/2^{(SPFS[1:0]+1)}]/32$

If user use $F_{osc}=20\text{MHz}$, $SPFS[1:0]$ of $SPWMC=\#03\text{H}$, then
 SPWM clock = $20\text{MHz}/2^4 = 20\text{MHz}/16 = 1.25\text{MHz}$
 SPWM output cycle frame frequency = $(20\text{MHz}/2^4)/32=39.1\text{KHz}$

7. TWSI Interface (Two Wire Serial Interface)

The TWSI module uses the SCL (clock) and the SDA (data) line to communicate with external a TWSI interface. Its speed is software selectable from between 6.25K to ~400Kbps by setting the BR[2..0] control bit. The TWSI module provides 4 interrupts (Rx, Tx, NonAck, TxFail). It can generate and detect START, repeated START and STOP signals automatically in master mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

7.1 TWSI Registers

TWSI Status Register (TWSIS, \$C0)

	bit-7					bit-0		
	RXIF	TXIF	TFIF	NAKIF	-	RXAK	MASTER	TXAK
Read / Write:	Note1	Note1	Note1	Note1		Note2	Note3	Note3
Reset value:	0	0	0	0	Unused	1	0	0

Note1:Read and Writer'0' only

Note2:Read only

Note3:Read and Writer

RXIF: The data Receive Interrupt Flag (RXIF) is set after the TWSIRDB (TWSI Receive Data Buffer) is loaded with newly receive data. Once the IRDB is loaded with the received data, no more data can be loaded to the TWSIRDB register.

TXIF: The data Transmit Interrupt Flag is set when the data of the TWSITDB register is downloaded to the shift register or if in Master Transmit mode the IADR is downloaded to the shift register. It is the software's responsibility to fill the TWSITDB register with new data when this bit is set. This bit is cleared by writing a zero to it, writing data to TWSITDB or when a reset occurs.

TFIF: The Transmit Fail Interrupt Flag is set when data transmit fails, which as set MASTER bit when the BB has been set by detecting the start condition on the lines or when the module is transmitting a One to SDA line but detected a Zero from SDA line in master mode, which is also called arbitration loss. This bit is cleared by writing Zero to it or by reset.

NAKIF: The Non-Acknowledge Interrupt Flag is only set in the master transmit mode when there is no acknowledge bit detected after one byte of data or a calling address is transferred. This bit is cleared by writing Zero to it or by reset.

RXAK: If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. If RXAK is high, it indicates no acknowledge signal has been detected at the 9th clock. Then the module will release the SDA line for the master to generate Stop or Repeated Start condition. It is set upon reset.

MASTER: If the MASTER bit is set, the module will generate a start condition to the SDA and SCL lines and send out the calling address which is stored in the IADR register. But if the TFIF flag is set when a transmit fail occurs on the lines, the module will discard the master mode by clearing the MASTER bit and release both SDA and SCL lines immediately. This bit can also be cleared by writing zero to it or when the NAKIF is set. When the MASTER bit is cleared either by set NAKIF or software the module will generate a stop condition to the lines after the current byte transmission is done, and IGNORE the TWSITDB data during the next TWSI transmit cycle if this data had not been transmitted out. Reset clears this bit.

TXAK: The bit (TXAK) controls the acknowledge transmit in RECEIVE mode. If it is cleared, a low (Ack) will be generated at the 9th clock after receiving 8 bits data. When TXAK is set, a high (NoAck) will be generated at the 9th clock after receiving 8 bits data. Reset clears this bit.

TWSI Address Register (TWSIA, \$C1)

	bit-7							bit-0
Read:	TWSIA.7	TWSIA.6	TWSIA.5	TWSIA.4	TWSIA.3	TWSIA.2	TWSIA.1	EXTADDR
Write:								
Reset value:	1	0	1	0	0	0	0	0

TWSIA[7:1] : These 7 bits can be the chip address in slave mode or the calling address when in master mode. This register is set as \$A0 upon reset.

EXTADDR : The EXTAD bit is set to expand the chip address of this module. When it is “1”, the module will acknowledge the general call address \$00 and the address comparison circuit will only compare the 4 MSB bits in the LADR register. When it is “0”, the module will only acknowledge to the specific address which is stored in the IADR register. It is zero after reset.

TWSI Control Register (TWSIC1, \$C2)

	bit-7							bit-0
Read:	TWSIE	-	-	-	BB	TWSIFS2	TWSIFS1	TWSIFS0
Write:								
Reset value:	0	0	0	0	0	0	0	1

TWSIE: If this TWSI module Enable bit (IE1) is set, the TWSI module is enable. If the IE1 is clear, the interface is disable and all flags will restore its reset default states. Reset clears this bit.

BB: The Bus Busy Flag is set after a start condition is detected, and is reset when a stop condition is detected. Reset clears this bit.

TWSIFS[2:0] :The three Baud Rate select bits will select one of the eight clock rates as the master clock when the module is in master mode. The serial clock frequency is equal to the external clock divided by the divider. These bits are cleared upon reset.

TWSIFS[2:0]	Baud Rate
0:0:0	Unused
0:0:1	400K
0:1:0	200K
0:1:1	100K
1:0:0	50K
1:0:1	25K
1:1:0	12.5K
1:1:1	6.25K

Note: clock source is from external (12M Hz).

TWSI Control Register 2 (TWSIC2, \$C3)

	bit-7						bit-0	
Read/Write:	MATCH Note1	SRW Note1	-	-	RSTART Note2	-	-	MRW Note3
Reset value:	1	0	0	0	0	0	0	0

Note1: Read and Writer'0' only

Note2: Read only

Note3: Read and Writer

MATCH: The MATCH flag is set when the first received data (following a START signal) in the IRDB register which matches with the address or its extended addresses (EXTAD=1) specified in the IADR.

SRW: The Slave Rw bit will indicate the data direction of TWSI protocol. It is updated after the calling address is received in the SLAVE mode. When it is one, the master will read the data from TWSI module, so the module is in transmit mode. When it is zero, the master will send data to the TWSI module, the module, the module is in receiving mode. The reset clears it.

RESTART: If the RESTART bit is set in master mode (MASTER=1), the module will generate a start condition to the SDA and SCL lines (after current ACK bit) and send out the calling address which is stored in the TWSIADR register. But if the TFIF flag is set when transmit fail occurs on the lines, the module will discard the master mode by clearing the MASTER bit and release bit SDA and SCL lines immediately. This bit will clear automatically after a start condition on the SDA and SCL lines. Reset clears this bit.

MRW: The MRW bit will be transmitted out as bit 0 of the calling address when the module sets the MASTER bit to enter the master mode. It will also determine the transfer direction of the following data bytes. When it is one, the module is in master receive mode. When it is zero, the module is in master transmit mode. Reset clears this bit.

TWSI Transmit Data Buffer (TWSITxD, \$C4)

	Bit-7							bit-0
Read:	TWSI TxD.7	TWSITxD.6	TWSITxD.5	TWSITxD.4	TWSITxD.3	TWSITxD.2	TWSITxD.1	TWSITxD.0
Write:								
Reset value:	0	0	0	0	0	0	0	0

The data written into this register will be automatically downloaded to the shift register when the module detects a matching calling address and the bit 0 of the received data is one (Slave transmit mode) or when the data in the shift register has been transmitted with received acknowledge bit (RXAK) =0 in transmit mode. So if the program doesn't write the data into the TWSITDB register before the matched calling address is detected or the shift register has been transmitted out, the module will pull down the SCL line (after receive acknowledge bit). If data is written to the TWSITxD register, then the written data will be downloaded to the shift register immediately and the module will release the SCL line, and the TXIF flag is set to generate another interrupt request for the next data. Therefore, the S/W may need to write the next data to the TWSITxD register and for the auto downloading of data to the shift register after the data in the shift register is transmitted again with RXAK=0. If the module receives non-acknowledge (RXAK=1), the module will release the SDA line for master to generate Stop or Repeated Start conditions.

TWSI Receive Data Buffer (TWSIRxD, \$C5)

	Bit-7							bit-0
Read:	TWSIRD.7	TWSIRD.6	TWSIRD.5	TWSIRD.4	TWSIRD.3	TWSIRD.2	TWSIRD.1	TWSIRD.0
Write:								
Reset value:	0	0	0	0	0	0	0	0

The TWSI Receive Data Buffer (TWSIRxD) contains the last received data when the MATCH flag is “1” or the calling address from the master when the MATCH flag is “0”. The TWSIRxD register will be updated after a data byte is received and the previous received data had been read out, otherwise the DDC module will pull down the SCL line to inhabit the next data transfer. It is a read-only register. The read operation of this register will clear the RXIF flag. After the RXIF flag is cleared, the register can load the received data again and set the RXIF flag the venerate interrupt request for reading the newly received data.

7.2 TWSI Interrupt

The TWSI module will generate TWSI interrupt once the hardware circuit detects the START signal of TWSISDA and TWSISCL. The TWSI interrupt vector is located at \$3B. There are three SFRs for configuring TWSI interrupt: IP1, IE1 and IFR. To use TWSI interrupt is the same as to use other generic 8052 interrupts. That means using ETWSI of IE1 for enable/disable TWSI interrupt, using PTWSI for assign TWSI interrupt priority. Whenever TWSI interrupt occurs, TWSIIF will be set to 1. After TWSI interrupt subroutine (vector) been executed, TWSIIF will be cleared to 0.

	Bit-7							bit-0
Read:	R	R	R	R	R	R	PTWSI	R
Write:								
Reset value:	0	0	0	0	0	0	0	0

Interrupt priority bit PTWSI = 1 assigns high interrupt priority
 Interrupt priority bit PTWSI = 0 assigns low interrupt priority

Interrupt Enable I Register (IE1, \$A9)

	Bit-7							bit-0
Read:	R	R	R	R	R	R	ETWSI	R
Write:								
Reset value:	0	0	0	0	0	0	0	0

Interrupt enable bit ETWSI = 1 enables the TWSI interrupt
 Interrupt enable bit ETWSI = 0 disables the TWSI interrupt

Interrupt Flag Register (IFR, \$AA)

	Bit-7							bit-0
Read:	R	R	R	R	R	R	TWSIIF	R
Write:								
Reset value:	0	0	0	0	0	0	0	0

Interrupt flag bit TWSIIF will be set to 1 when TWSI interrupt occurs. Interrupt flag bit TWSIIF will be clear to 0 if TWSI interrupt subroutine executed.

7.2 PROGRAM ALGORITHM

When the TWSI module detects an arbitration loss in the master, it will release both SDA and SCL lines immediately. If there is no further Stop condition detected, the module will be hung up.

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 °C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1: Under steady state (non-transient) conditions, IOL must be externally

Limited as follows : Maximum IOL per port pin : 10mA

Maximum IOL per 8-bit port : port 0 :26mA

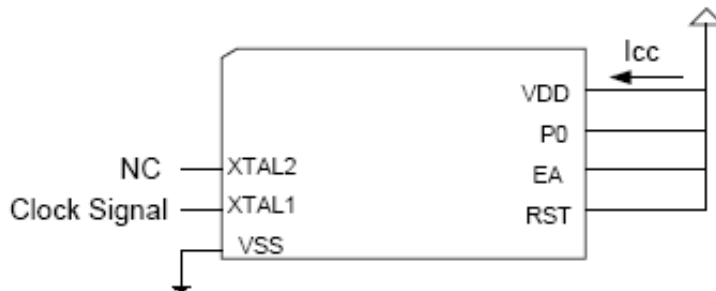
port 1,2,3 :15mA

Maximum total IOL for all output pins : 71mA

If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Note2 : Minimum VCC for Power-down is 2V.

Icc Active Mode Test Circuit



AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T I H I	A I F pulse width	RD/WRT	115			2xT - 10			nS	
T A V I	Address Valid to A I F low	RD/WRT	43			T - 20			nS	
T I I A X	Address Hold after A I F low	RD/WRT	53			T - 10			nS	
T I I I V	A I F low to Valid Instruction In	RD			240			4xT-10	nS	
T I I P I	A I F low to #PSEN low	RD	53			T - 10			nS	
T P I P H	#PSEN pulse width	RD	173			3xT - 15			nS	
T P I I V	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T P X I X	Instruction Hold after #PSEN	RD	0			0			nS	
T P X I 7	Instruction Float after #PSEN	RD			87			T + 25	nS	
T A V I V	Address to Valid Instruction In	RD			292			5xT -20	nS	
T P I A 7	#PSEN low to Address Float	RD			10			10	nS	
T R I R H	#RD pulse width	RD	365			6xT - 10			nS	
T W I W H	#WR pulse width	WRT	365			6xT - 10			nS	
T R I D V	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T R H D X	Data Hold after #RD	RD	0			0			nS	
T R H D 7	Data Float after #RD	RD			145			2xT+20	nS	
T I I D V	A I F low to Valid Data In	RD			590			8xT - 10	nS	
T A V D V	Address to Valid Data In	RD			542			9xT - 20	nS	
T I I Y I	A I F low to #WR High or #RD low	RD/WRT	178		197	3xT-10		3xT+10	nS	
T A V Y I	Address Valid to #WR or #RD low	RD/WRT	230			4xT-20			nS	
T Q V W H	Data Valid to #WR High	WRT	403			7xT-35			nS	
T Q V W X	Data Valid to #WR transition	WRT	38			T - 25			nS	
T W H O X	Data hold after #WR	WRT	73			T + 10			nS	
T R I A 7	#RD low to Address Float	RD						5	nS	
T Y A I H	#WR or #RD high to A I F high	RD/WRT	53		72	T -10		T + 10	nS	
T C H C I	clock fall time								nS	
T C I C X	clock low time								nS	
T C I C H	clock rise time								nS	
T C H C X	clock high time								nS	

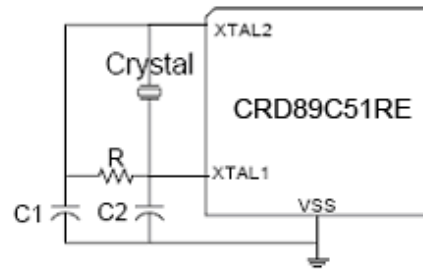
ISP Test Conditions

(40 MHz, typical operating conditions, valid for CRD89C51RE series)

Symbol	MAX	Remark
Chip erase	3000ms	Vcc = 5V
Page erase	10ms	"
Program	30us	"
Protect	400us	"

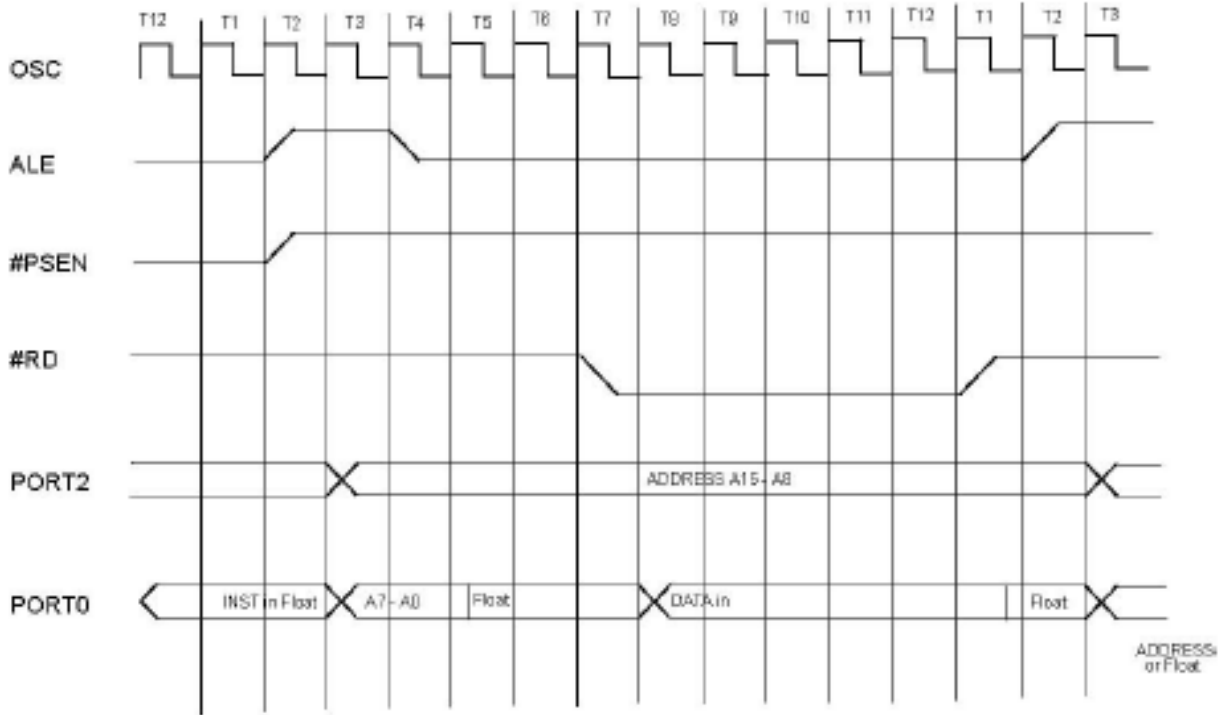
Application Reference

Valid for CRD89C51RE				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

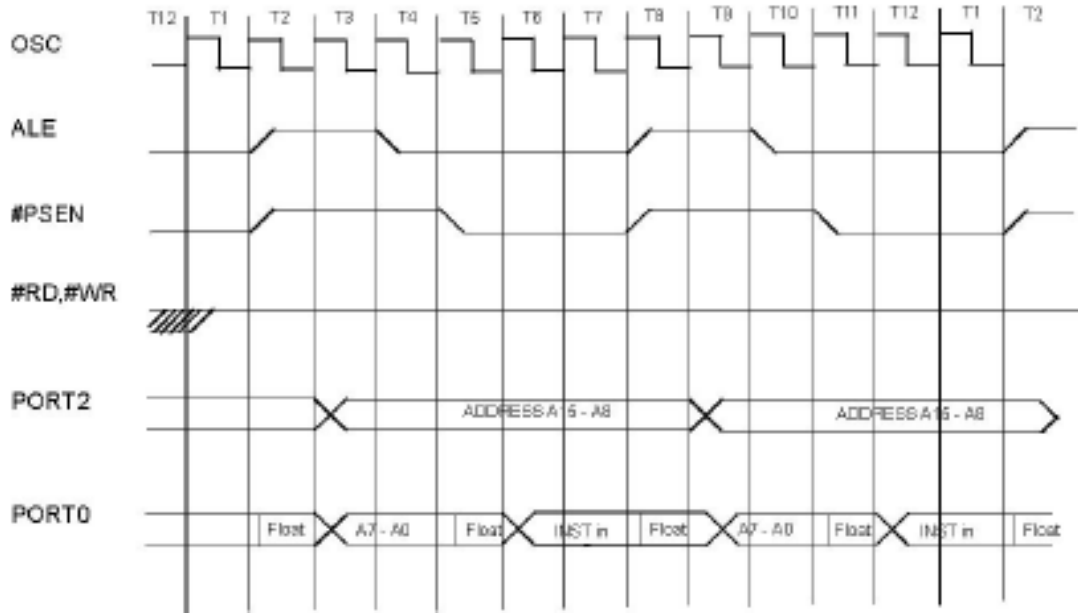


NOTE: Oscillation circuit may differ with different crystal or ceramic resonator in higher oscillation frequency, which was due to each crystal, or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacture for appropriate value of external components.

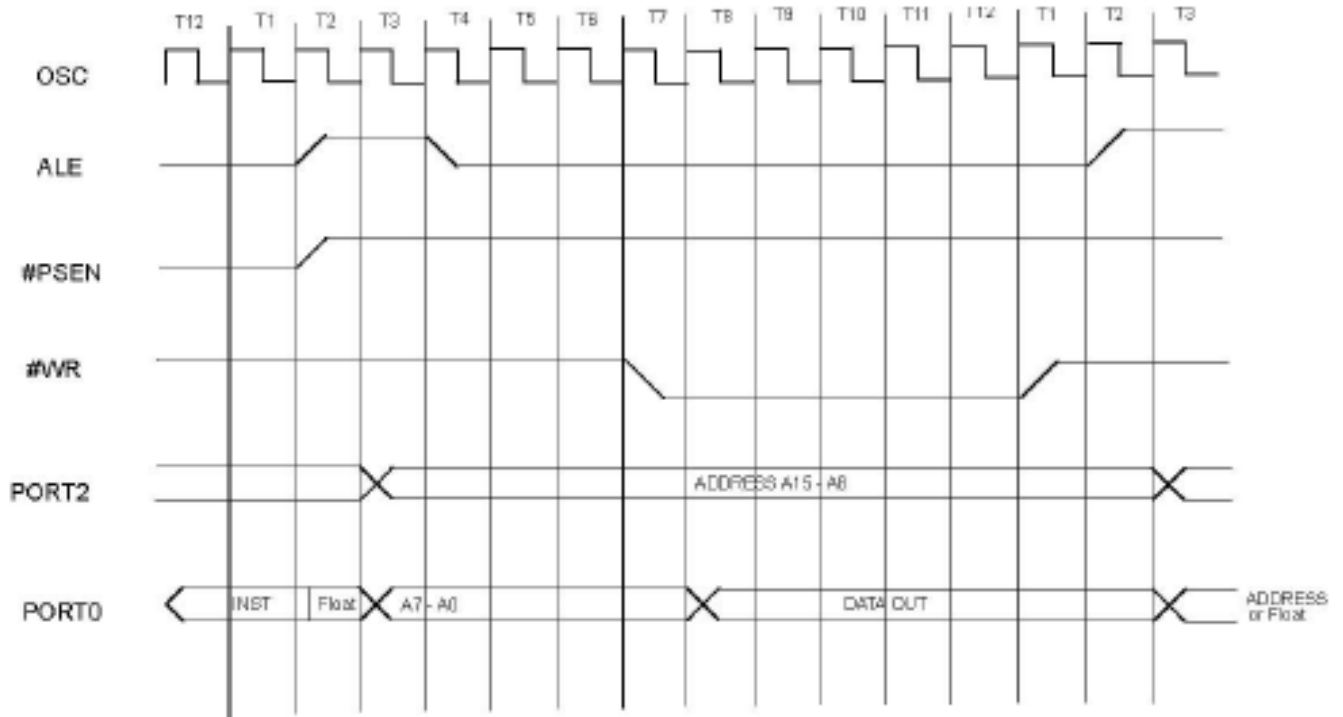
Data Memory Read Cycle Timing



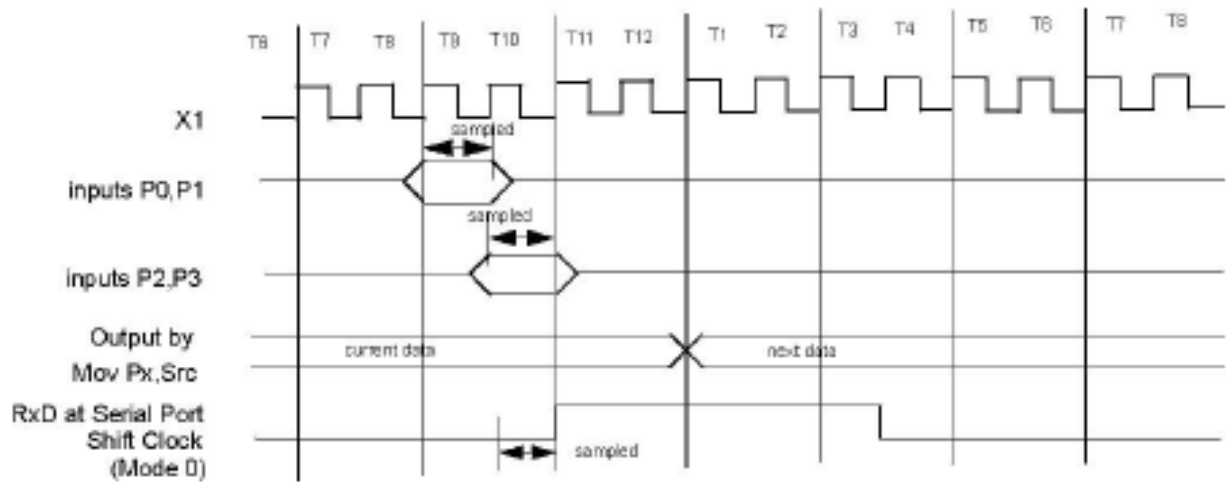
Program Memory Read Cycle Timing



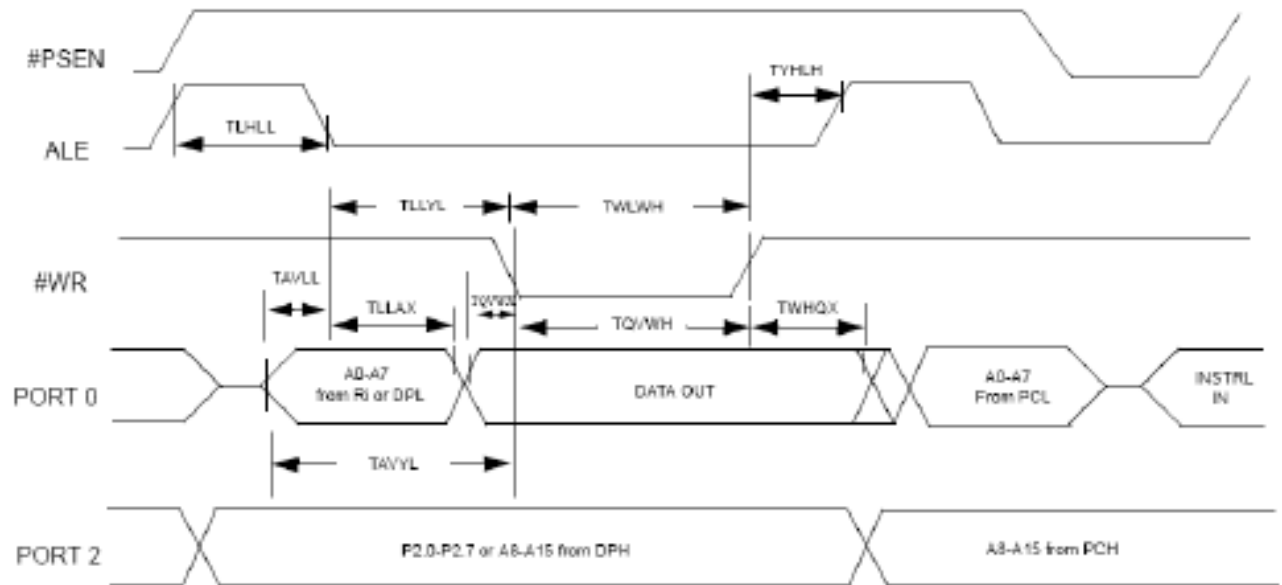
Data Memory Write Cycle Timing



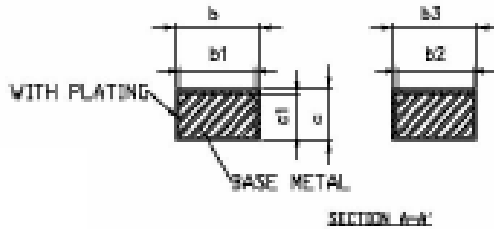
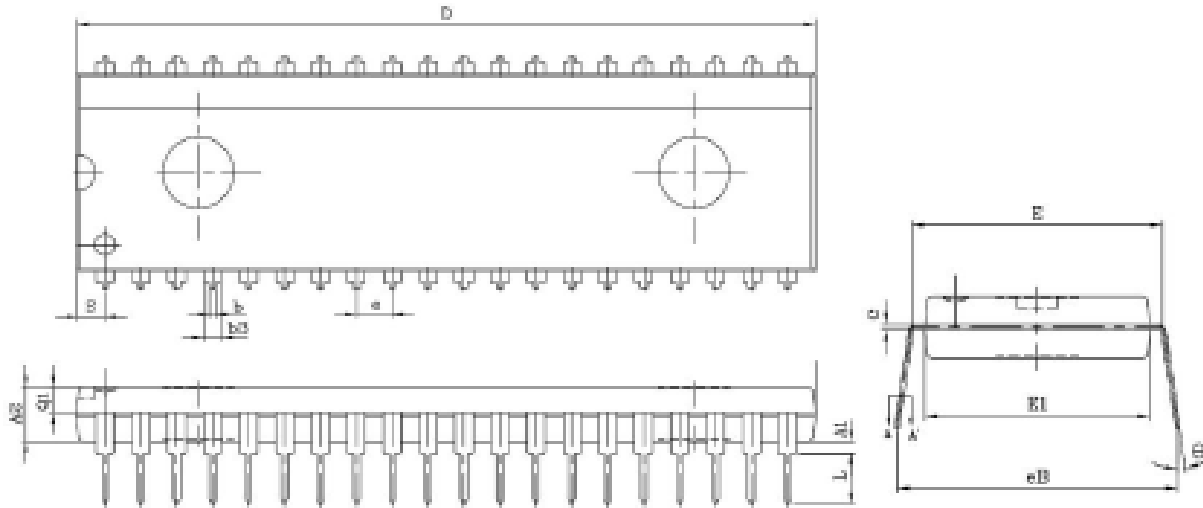
I/O Ports Timing



Tm.III External Data Memory Write Cycle



PDIP 40L (600mil) Package Information :

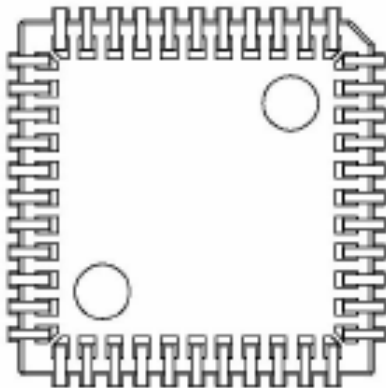
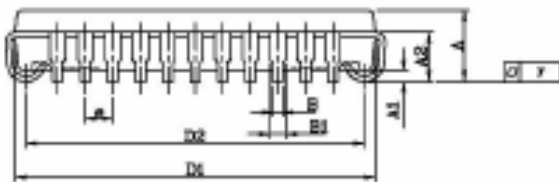
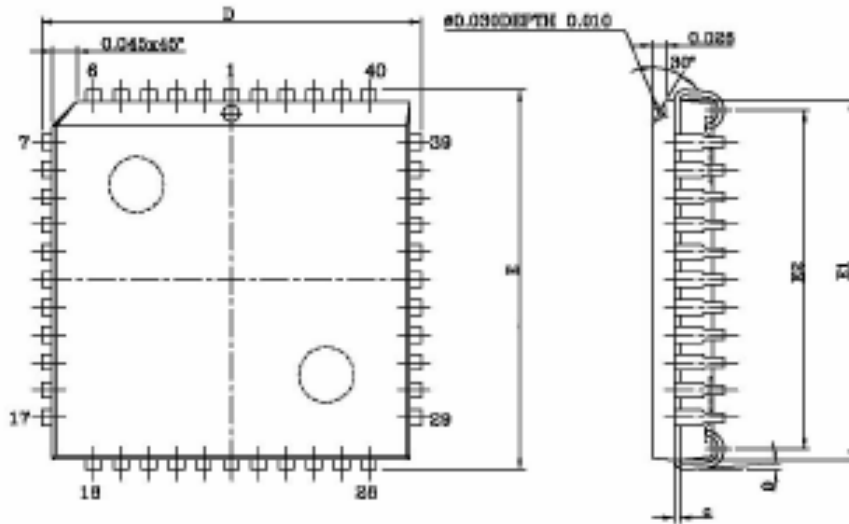


Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A1	0.254	—	—	10	—	—
A2	3.683	3.810	3.937	145	150	155
b	0.356	0.500	0.660	14	20	26
b1	0.356	0.457	0.508	14	18	22
b2	1.016	1.270	1.524	40	50	60
b3	1.016	1.321	1.626	40	52	64
c	0.203	0.254	0.432	8	10	17
c1	0.203	0.254	0.356	8	10	14
D	52.07	52.2	52.32	2050	2055	2060
E	14.99	15.24	15.49	590	600	610
E1	13.69	13.87	13.94	539	546	549
e	—	2.540	—	—	100	—
eB	15.75	16.26	16.76	620	640	660
L	2.921	3.302	3.683	115	130	145
S	1.727	1.981	2.235	68	78	88
Q1	1.651	1.778	1.905	65	70	75
theta	0°	—	10°	0°	—	10°

Note:

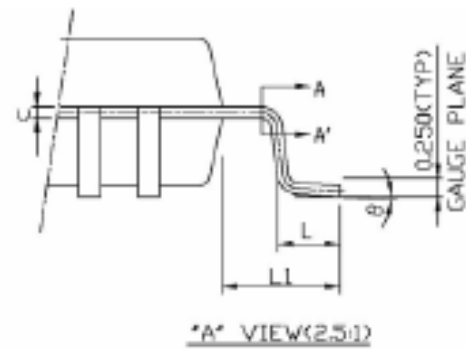
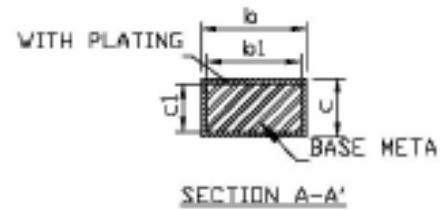
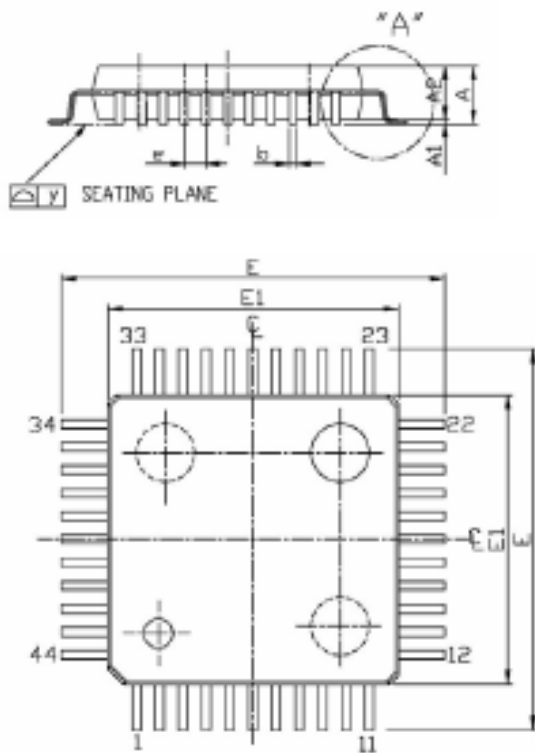
1. Refer to JEDEC STD.MS-011(AC).
2. Dimension D and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D and E1 are maximum plastic body size dimension include mold mismatch.
3. Dimension b3 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.2mm.

PLCC 44L Package Information :



UNIT SYMBOL	INCH(REF)	MM(BASE)
A	0.180(MAX)	4.572(MAX)
A1	0.024 ±0.005	0.52 ±0.14
A2	0.105 ±0.005	2.667 ±0.127
B	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
B1	0.028 + 0.004 - 0.002	0.711 + 0.102 - 0.051
c	0.010(TYP)	0.254(TYP)
D	0.690 ±0.010	17.526 ±0.254
D1	0.653 ±0.003	16.586 ±0.076
D2	0.610 ±0.020	15.494 ±0.508
E	0.690 ±0.010	17.526 ±0.254
E1	0.653 ±0.003	16.586 ±0.076
E2	0.610 ±0.010	15.494 ±0.254
e	0.050(TYP)	1.270(TYP)
y	0.003(MAX)	0.076(MAX)
θ	0~5°	0~5°

QFP 44L(10x10x2.0mm) Package Information :



Note:

1. Refer to JEDC STD.MS-022(AB).
2. Dimension E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.E1 are maximum plastic body size dimension Include mold mismatch .
3. Dimension b does not include dambar protrusion .Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.1 mm.

Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A	—	—	2.45	—	—	964
A1	0.05	0.15	0.25	2.1	6.0	9.6
A2	1.90	2.00	2.10	74.8	78.7	82.7
b	0.29	0.32	0.45	11.4	12.6	17.7
b1	0.29	0.30	0.41	11.4	11.8	16.1
c	0.11	0.17	0.23	4.3	6.7	9.1
c1	0.11	0.15	0.19	4.3	5.9	7.5
E	13.00	13.20	13.40	512	520	528
E1	9.90	10.00	10.10	390	394	398
[e]	—	0.800	—	—	31.5	—
L	0.73	0.88	1.03	28.7	34.6	40.6
L1	1.50	1.60	1.70	59.1	63.0	66.9
y	—	—	0.076	—	—	3
θ	0°	—	7°	0°	—	7°