CRD89C512RD

8-Bit Microcontroller with 2x64KB ISP Flash, 1KB of SRAM, PWMs

Product List

CRD89C512RD-40
5V, 40MHz 128KB ISP flash MCU

Description

The CRD89C512RD is based on the standard 8051 microcontroller architecture and is a pin compatible drop-in replacement for the 8051.

The CRD89C512RD is aimed at a diversity of applications that require a large amount of program/data memory with non-volatile data storage and/or code/field based firmware upgrade capability coupled with comprehensive peripheral support. It features 64KB of In-System/In-Application Programmable Flash memory, 64KB data Flash memory, 1KB of SRAM, 4 PWM outputs, a UART, three 16-bit timers/counters, a watchdog timer and power down features.

The CRD89C512RD is available with firmware that enables In-System Programming (firmware based boot-loader) of the Flash memory via the UART interface (ISPVx version). General Flash memory programming is supported by device programmers available from Cyrod or other 3rd party commercial programmer suppliers.

The CRD89C512RD is available in PLCC-44, QFP-44 and DIP-40 packages and functions over the industrial temperature range.

Feature Set

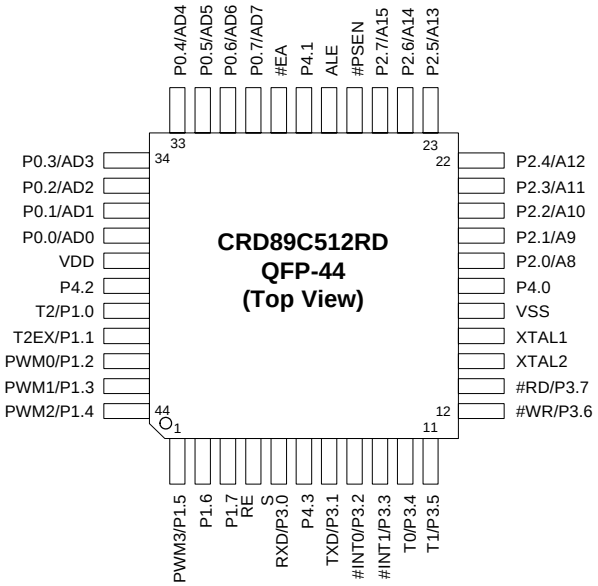
- 80C51/80C52 pin compatible
- 64KB Program + 64KB Data Flash memory
- In-System / In-Application Flash Programming (ISP/IAP)
- Program voltage: 5V
- 1024 Bytes on chip data SRAM
- Four 8-bit I/Os + one 4-bit I/O
- 4 PWM outputs on P1.3 to P1.7
- One Full Duplex UART serial port
- Three 16-bit Timers/Counters
- Watchdog Timer
- Bit operation instruction
- 8-bit Unsigned Multiply and Division instructions
- BCD arithmetic
- Direct and Indirect Addressing
- Two Levels of Interrupt Priority and Nested Interrupts
- Power saving modes
- Code protection function
- Low EMI (inhibit ALE)
- Operating Temperature Range -40ºC to +85ºC

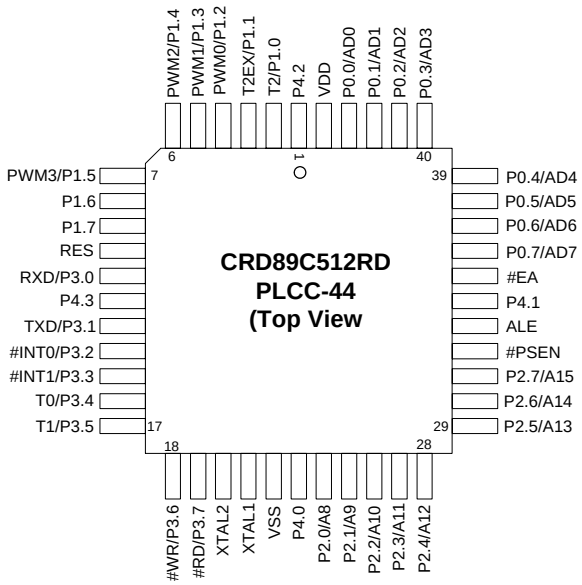
Ordering Information

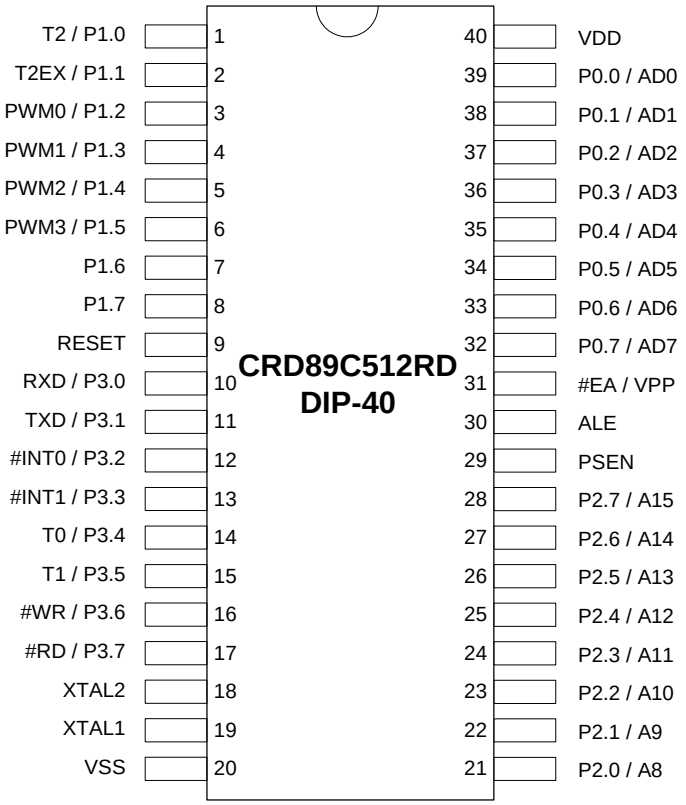
CRD89C512RD-40-P 5V, 2x64KB ISP flash, 40 MHz 40-PDIP
CRD89C512RD-40-J 5V, 2x64KB ISP flash, 40 MHz 44-PLCC
CRD89C512RD-40-Q 5V, 2x64KB ISP flash, 40 MHz 44-QFP

info@cyrod.com
www.cyrod.com
4261-A14 Hwy. #7 East, Unit 290
Markham, ON L3R 9W6
Canada

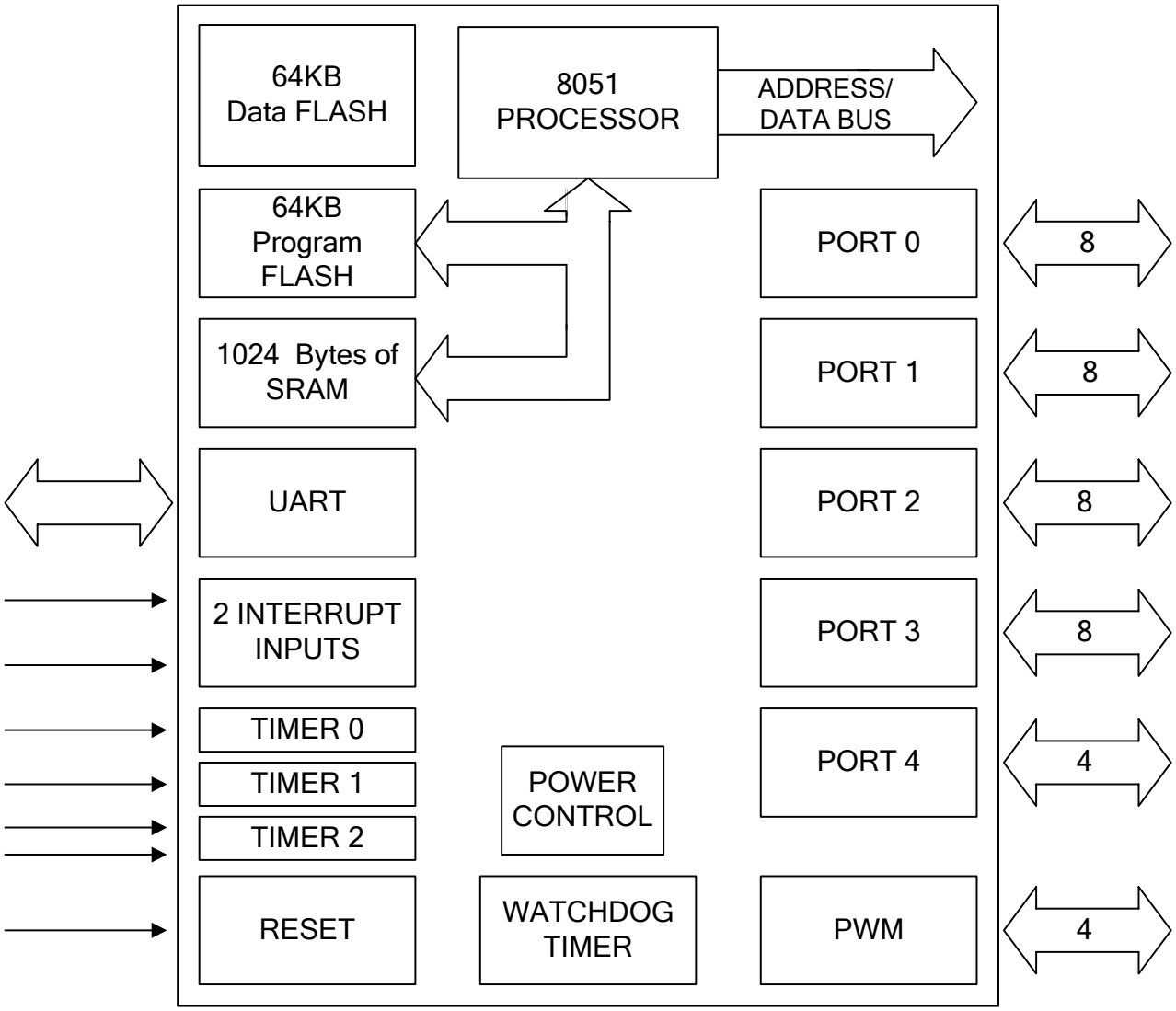
Pin Configuration







Block Diagram



Pin Descriptions for QFP-44/PLCC-44

TABLE 1: PIN DESCRIPTIONS FOR QFP-44/PLCC-44

QFP - 44	PLCC - 44	Name	I/O	Function
1	7	PWM3	O	PWM Channel 3
		P1.5	I/O	Bit 5 of Port 1
2	8	P1.6	I/O	Bit 6 of Port 1
3	9	P1.7	I/O	Bit 7 of Port 1
4	10	RES	I	Reset
5	11	RXD	I	Receive Data
		P3.0	I/O	Bit 0 of Port 3
6	12	P4.3	I/O	Bit 3 of Port 4
7	13	TXD	O	Transmit Data &
		P3.1	I/O	Bit 1 of Port 3
8	14	#INT0	I	External Interrupt 0
		P3.2	I/O	Bit 2 of Port 3
9	15	#INT1	I	External Interrupt 1
		P3.3	I/O	Bit 3 of Port 3
10	16	T0	I	Timer 0
		P3.4	I/O	Bit 4 of Port 3
11	17	T1	I	Timer 1 & 3
		P3.5	I/O	Bit 5 of Port
12	18	#WR	O	Ext. Memory Write
		P3.6	I/O	Bit 6 of Port 3
13	19	#RD	O	Ext. Memory Read
		P3.7	I/O	Bit 7 of Port 3
14	20	XTAL2	O	Oscillator/Crystal Output
15	21	XTAL1	I	Oscillator/Crystal In
16	22	VSS	-	Ground
17	23	P4.0	I/O	Bit 0 of Port 4
18	24	P2.0	I/O	Bit 0 of Port 2
		A8	O	Bit 8 of External Memory Address
19	25	P2.1	I/O	Bit 1 of Port 2
		A9	O	Bit 9 of External Memory Address
20	26	P2.2	I/O	Bit 2 of Port 2
		A10	O	Bit 10 of External Memory Address
21	27	P2.3	I/O	Bit 3 of Port 2 &
		A11	O	Bit 11 of External Memory Address
22	28	P2.4	I/O	Bit 4 of Port 2
		A12	O	Bit 12 of External Memory Address
23	29	P2.5	I/O	Bit 5 of Port 2
		A13	O	Bit 13 of External Memory Address
24	30	P2.6	I/O	Bit 6 of Port 2
		A14	O	Bit 14 of External Memory Address
25	31	P2.7	I/O	Bit 7 of Port 2
		A15	O	Bit 15 of External Memory Address
26	32	#PSEN	O	Program Store Enable
27	33	ALE	O	Address Latch Enable
28	34	P4.1	I/O	Bit 1 of Port 4
29	35	#EA	I	External Access
30	36	P0.7	I/O	Bit 7 Of Port 0
		AD7	I/O	Data/Address Bit 7 of External Memory
31	37	P0.6	I/O	Bit 6 of Port 0
		AD6	I/O	Data/Address Bit 6 of External Memory
32	38	P0.5	I/O	Bit 5 of Port 0
		AD5	I/O	Data/Address Bit 5 of External Memory
33	39	P0.4	I/O	Bit 4 of Port 0
		AD4	I/O	Data/Address Bit 4 of External Memory
34	40	P0.3	I/O	Bit 3 Of Port 0
		AD3	I/O	Data/Address Bit 3 of External Memory
35	41	P0.2	I/O	Bit 2 of Port 0
		AD2	I/O	Data/Address Bit 2 of External Memory
36	42	P0. 1	I/O	Bit 1 of Port 0 & Data
		AD1	I/O	Address Bit 1 of External Memory
37	43	P0.0	I/O	Bit 0 Of Port 0 & Data
		AD0	I/O	Address Bit 0 of External Memory
38	44	VDD	-	VCC
39	1	P4.2	I/O	Bit 2 of Port 4
40	2	T2	I	Timer 2 Clock Out
		P1.0	I/O	Bit 0 of Port 1
41	3	T2EX	I	Timer 2 Control
		P1.1	I/O	Bit 1 of Port 1
42	4	PWM0	O	PWM Channel 0
		P1.2	I/O	Bit 2 of Port 1
43	5	PWM1	O	PWM Channel 1
		P1.3	I/O	Bit 3 of Port 1
44	6	PWM2	O	PWM Channel 2
		P1.4	I/O	Bit 4 of Port 1

CRD89C512RD DIP40 Pin Descriptions

TABLE 2: CRD89C512RD PIN DESCRIPTIONS FOR DIP40 PACKAGE

DIP40	Name	I/O	Function
1	T2	I	Timer 2 Clock Out
	P1.0	I/O	Bit 0 of Port 1
2	T2EX	I	Timer 2 Control
	P1.1	I/O	Bit 1 of Port 1
3	PWM0	O	PWM Channel 0
	P1.2	I/O	Bit 2 of Port 1
4	PWM1	O	PWM Channel 1
	P1.3	I/O	Bit 3 of Port 1
5	PWM2	O	PWM Channel 2
	P1.4	I/O	Bit 4 of Port 1
6	PWM3	O	PWM Channel 3
	P1.5	I/O	Bit 5 of Port 1
7	P1.6	I/O	Bit 6 of Port 1
8	P1.7	I/O	Bit 7 of Port 1
9	RESET	I	Reset
10	RXD	I	Receive Data
	P3.0	I/O	Bit 0 of Port 3
11	TXD	O	Transmit Data &
	P3.1	I/O	Bit 1 of Port 3
12	#INT0	I	External Interrupt 0
	P3.2	I/O	Bit 2 of Port 3
13	#INT1	I	External Interrupt 1
	P3.3	I/O	Bit 3 of Port 3
14	T0	I	Timer 0
	P3.4	I/O	Bit 4 of Port 3
15	T1	I	Timer 1 & 3
	P3.5	I/O	Bit 5 of Port
16	#WR	O	Ext. Memory Write
	P3.6	I/O	Bit 6 of Port 3
17	#RD	O	Ext. Memory Read
	P3.7	I/O	Bit 7 of Port 3
18	XTAL2	O	Oscillator/Crystal Output
19	XTAL1	I	Oscillator/Crystal In
20	VSS	-	Ground
21	P2.0	I/O	Bit 0 of Port 2
	A8	O	Bit 8 of External Memory Address
22	P2.1	I/O	Bit 1 of Port 2
	A9	O	Bit 9 of External Memory Address
23	P2.2	I/O	Bit 2 of Port 2
	A10	O	Bit 10 of External Memory Address
24	P2.3	I/O	Bit 3 of Port 2 &
	A11	O	Bit 11 of External Memory Address
25	P2.4	I/O	Bit 4 of Port 2
	A12	O	Bit 12 of External Memory Address
26	P2.5	I/O	Bit 5 of Port 2
	A13	O	Bit 13 of External Memory Address
27	P2.6	I/O	Bit 6 of Port 2
	A14	O	Bit 14 of External Memory Address
28	P2.7	I/O	Bit 7 of Port 2
	A15	O	Bit 15 of External Memory Address
29	#PSEN	O	Program Store Enable
30	ALE	O	Address Latch Enable
31	#EA / VPP	I	External Access Flash programming voltage input
32	P0.7	I/O	Bit 7 Of Port 0
	AD7	I/O	Data/Address Bit 7 of External Memory
33	P0.6	I/O	Bit 6 of Port 0
	AD6	I/O	Data/Address Bit 6 of External Memory
34	P0.5	I/O	Bit 5 of Port 0
	AD5	I/O	Data/Address Bit 5 of External Memory
35	P0.4	I/O	Bit 4 of Port 0
	AD4	I/O	Data/Address Bit 4 of External Memory
36	P0.3	I/O	Bit 3 Of Port 0
	AD3	I/O	Data/Address Bit 3 of External Memory
37	P0.2	I/O	Bit 2 of Port 0
	AD2	I/O	Data/Address Bit 2 of External Memory
38	P0. 1	I/O	Bit 1 of Port 0 & Data
	AD1	I/O	Address Bit 1 of External Memory
39	P0.0	I/O	Bit 0 Of Port 0 & Data
	AD0	I/O	Address Bit 0 of External Memory
40	VDD	-	Supply input

Instruction Set

The following table describes the CRD89C512RD instruction set. The instructions are function and binary code compatible with industry standard 8051s.

TABLE 3: LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 4: CRD89C512RD INSTRUCTION SET

Mnemonic	Description	Size bytes	Instr. Cycles
Arithmetic instructions			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	1
ADD A, @Ri	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	1
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	1
ADDC A, @Ri	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	1
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	1
SUBB A, @Ri	Subtract data mem from A with borrow	1	1
SUBB A, #data	Subtract immediate from A with borrow	2	1
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @Ri	Increment data memory	1	1
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @Ri	Decrement data memory	1	1
INC DPTR	Increment data pointer	1	2
MUL AB	Multiply A by B	1	4
DIV AB	Divide A by B	1	4
DA A	Decimal adjust A	1	1
Logical Instructions			
ANL A, Rn	AND register to A	1	1
ANL A, direct	AND direct byte to A	2	1
ANL A, @Ri	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	1
ANL direct, A	AND A to direct byte	2	1
ANL direct, #data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to A	1	1
ORL A, direct	OR direct byte to A	2	1
ORL A, @Ri	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	1
ORL direct, A	OR A to direct byte	2	1
ORL direct, #data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	1
XRL A, @Ri	Exclusive-OR data memory to A	1	1
XRL A, #data	Exclusive-OR immediate to A	2	1
XRL direct, A	Exclusive-OR A to direct byte	2	1
XRL direct, #data	Exclusive-OR immediate to direct byte	3	2
CLR A	Clear A	1	1
CPL A	Compliment A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Mnemonic	Description	Size bytes	Instr. Cycles
Boolean Instruction			
CLR C	Clear Carry bit	1	1
CLR bit	Clear bit	2	1
SETB C	Set Carry bit to 1	1	1
SETB bit	Set bit to 1	2	1
CPL C	Complement Carry bit	1	1
CPL bit	Complement bit	2	1
ANL C,bit	Logical AND between Carry and bit	2	2
ANL C,#bit	Logical AND between Carry and not bit	2	2
ORL C,bit	Logical ORL between Carry and bit	2	2
ORL C,#bit	Logical ORL between Carry and not bit	2	2
MOV C,bit	Copy bit value into Carry	2	1
MOV bit,C	Copy Carry value into Bit	2	2
Data Transfer Instructions			
MOV A, Rn	Move register to A	1	1
MOV A, direct	Move direct byte to A	2	1
MOV A, @Ri	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	1
MOV Rn, A	Move A to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, #data	Move immediate to register	2	1
MOV direct, A	Move A to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	2
MOV direct, @Ri	Move data memory to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	2
MOV @Ri, A	Move A to data memory	1	1
MOV @Ri, direct	Move direct byte to data memory	2	2
MOV @Ri, #data	Move immediate to data memory	2	1
MOV DPTR, #data	Move immediate to data pointer	3	2
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	2
MOVC A, @A+PC	Move code byte relative PC to A	1	2
MOVX A, @Ri	Move external data (A8) to A	1	2
MOVX A, @DPTR	Move external data (A16) to A	1	2
MOVX @Ri, A	Move A to external data (A8)	1	2
MOVX @DPTR, A	Move A to external data (A16)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange A and register	1	1
XCH A, direct	Exchange A and direct byte	2	1
XCH A, @Ri	Exchange A and data memory	1	1
XCHD A, @Ri	Exchange A and data memory nibble	1	1

Mnemonic	Description	Size bytes	Instr. Cycles
Branching Instructions			
ACALL addr 11	Absolute call to subroutine	2	2
LCALL addr 16	Long call to subroutine	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr 11	Absolute jump unconditional	2	2
LJMP addr 16	Long jump unconditional	3	2
SJMP rel	Short jump (relative address)	2	2
JC rel	Jump on carry = 1	2	2
JNC rel	Jump on carry = 0	2	2
JB bit, rel	Jump on direct bit = 1	3	2
JNB bit, rel	Jump on direct bit = 0	3	2
JBC bit, rel	Jump on direct bit = 1 and clear	3	2
JMP @A+DPTR	Jump indirect relative DPTR	1	2
JZ rel	Jump on accumulator = 0	2	2
JNZ rel	Jump on accumulator 1= 0	2	2
CJNE A, direct, rel	Compare A, direct JNE relative	3	2
CJNE A, #d, rel	Compare A, immediate JNE relative	3	2
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	2
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	2
DJNZ Rn, rel	Decrement register, JNZ relative	2	2
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	2
Miscellaneous Instruction			
NOP	No operation	1	1

Rn: Any of the register R0 to R7
@Ri: Indirect addressing using Register R0 or R1
#data: immediate Data provided with Instruction
#data16: Immediate data included with instruction
bit: address at the bit level
rel: relative address to Program counter from +127 to –128
Addr11: 11-bit address range
Addr16: 16-bit address range
#d: Immediate Data supplied with instruction

Special Function Registers (SFR)

Addresses 80h to FFh of the SFR address space can be accessed in direct addressing mode only. The following table lists the CRD89C512RD special function registers.

TABLE 5: SPECIAL FUNCTION REGISTERS (SFR)

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
P0	80h	-	-	-	-	-	-	-	-	1111 1111b
SP	81h	-	-	-	-	-	-	-	-	0000 0111b
DPL	82h	-	-	-	-	-	-	-	-	0000 0000b
DPH	83h	-	-	-	-	-	-	-	-	0000 0000b
MPAGE	85h	-	-	-	-	-	-	-	-	0000 0000b
DBANK	86h	BSE	-	-	-	BS3	BS2	BS1	BS0	0000 0001b
PCON	87h	SMOD	-	-	-	GF1	GF0	PDOWN	IDLE	0000 0000b
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0010b
TMOD	89h	GATE1	C/T1	M1.1	M0.1	GATE0	C/T0	M1.0	M0.0	0000 0000b
TL0	8Ah	-	-	-	-	-	-	-	-	0000 0000b
TL1	8Bh	-	-	-	-	-	-	-	-	0000 0000b
TH0	8Ch	-	-	-	-	-	-	-	-	0000 0000b
TH1	8Dh	-	-	-	-	-	-	-	-	0000 0000b
P1	90h	-	-	-	-	-	-	-	-	1111 1111b
WDTKEY	97h	-	-	-	-	-	-	-	-	0000 0000b
SCON	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000b
SBUF	99h	-	-	-	-	-	-	-	-	0111 1111b
PWME	9Bh	-	-	PWM3E	PWM2E	PWM1E	PWM0E	-	-	0000 0000b
WDTCTRL	9Fh	WDTE	-	CLEAR	-	-	PS2	PS1	PS0	0000 0000b
P2	A0h	-	-	-	-	-	-	-	-	1111 1111b
PWMC	A3h	-	-	-	-	-	-	PDCK1	PDCK0	0000 0000b
PWMD0	A4h	PWMD0.4	PWMD0.3	PWMD0.2	PWMD0.1	PWMD0.0	NP0.2	NP0.1	NP0.0	0000 0000b
PWMD1	A5h	PWMD1.4	PWMD1.3	PWMD1.2	PWMD1.1	PWMD1.0	NP1.2	NP1.1	NP1.0	0000 0000b
PWMD2	A6h	PWMD2.4	PWMD2.3	PWMD2.2	PWMD2.1	PWMD2.0	NP2.2	NP2.1	NP2.0	0000 0000b
PWMD3	A7h	PWMD3.4	PWMD3.3	PWMD3.2	PWMD3.1	PWMD3.0	NP3.2	NP3.1	NP3.0	0000 0000b
IE	A8h	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0000 0000b
P3	B0h	-	-	-	-	-	-	-	-	1111 1011b
IP	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	0000 0000b
SYSCON	BFh	WDR	-	-	-	DATAFE	IAPE	XRAME	ALEI	0000 1010b
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	0000 0000b
RCAP2L	CAh	-	-	-	-	-	-	-	-	0000 0000b
RCAP2H	CBh	-	-	-	-	-	-	-	-	0000 0000b
TL2	CCh	-	-	-	-	-	-	-	-	0000 0000b
TH2	CDh									0000 0000b
PSW	D0h	CY	AC	F0	RS1	RS0	OV	-	P	0000 0001b
P4	D8h	-	-	-	-	P4.3	P4.2	P4.1	P4.0	****1111b
ACC	E0h	-	-	-	-	-	-	-	-	
B	F0h	-	-	-	-	-	-	-	-	0000 0000b
IAPFADHI	F4h	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8	0000 0000b
IAPFADLO	F5h	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0000 0000b
IAPFDATA	F6h	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	0000 0000b
IAPFCTRL	F7h	IAPSTART		FZONE				**IAPFCT**1	**IAPFCT**0	0000 0000b

info@cyrod.com
www.cyrod.com

CRD89C512RD Program + Data Flash Memory

The CRD89C512RD includes 64KB of on-chip Flash memory that can be used as program memory or as non-volatile data storage memory using the In-Application Programming feature (IAP). The CRD89C512RD also includes 64KB of data storage Flash memory that is also IAP programmable.

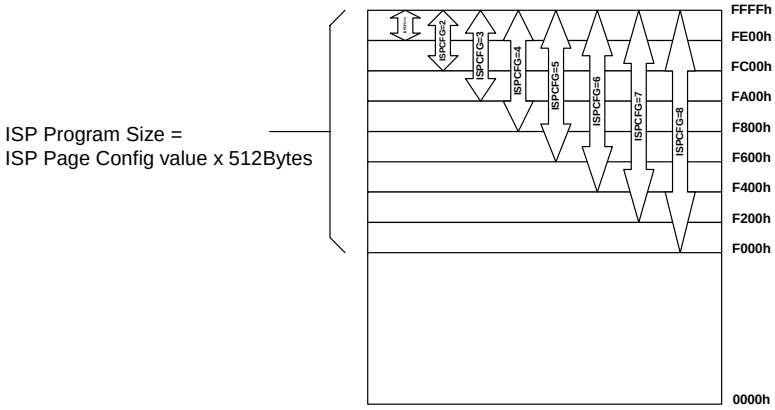
ISP Boot Program Memory Zone

The upper portion of the CRD89C512RD Flash program memory can be reserved to store an ISP (In-System Programmable) boot loader program.

This boot program can be used to program the Flash memory via the serial interface (or via any other method). by making use of the In-Application Programming (IAP) feature. This allows the processor to load the program or data from an external device or system, and to program it into the Flash memory (see the CRD89C512RD IAP feature section).

The size of the memory block reserved for the ISP boot loader program (when activated) is adjustable from 512 to 4KB bytes in increments of 512 bytes, using the ISP Page config parameter.

FIGURE1: CRD89C512RD-ISP PROGRAM SIZE VS ISP CONFIG. VALUE



Programming the ISP Boot Program

The ISP boot program is programmed into the device using a parallel programmer, such as the VERSAMCU-PPR, or a commercial parallel programmer that supports the CRD89C512RD. The Flash memory reserved for the ISP program is defined by the parallel programmer software (ISP Page Config) when the device is programmed.

When programming the ISP boot program into the CRD89C512RD, the "lock bit" option should be activated to protect the ISP Flash memory zone from being inadvertently erased, which can happen when Flash Erase operations are performed under the control of the ISP boot program, or to prevent the CRD89C512RD Flash memory from being read back using a parallel programmer.

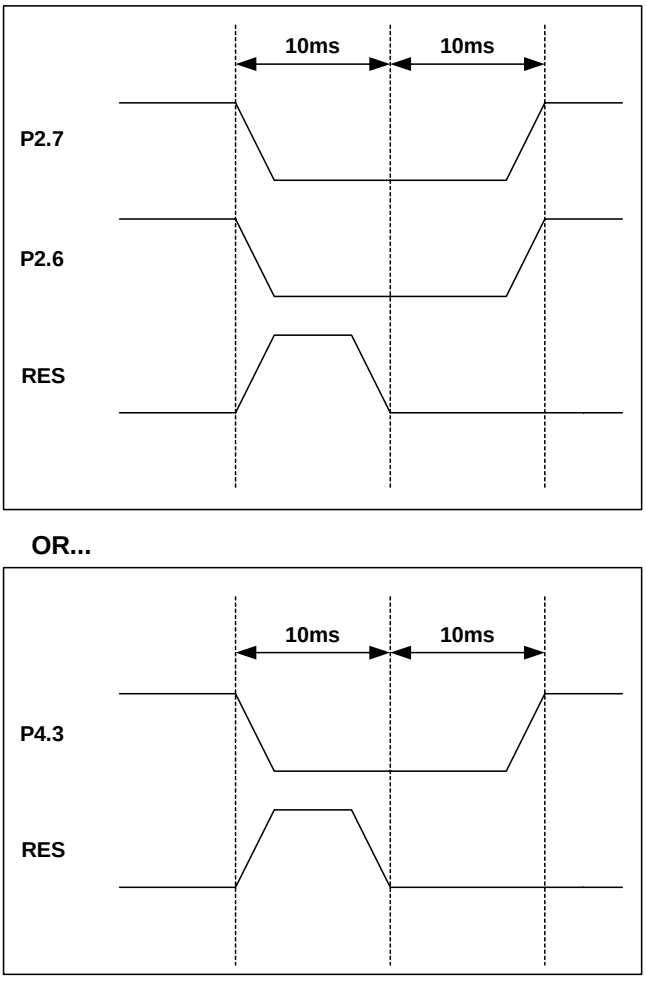
If an Erase operation is performed using a parallel programmer, the entire Flash memory, including the ISP Boot program memory zone, will be erased.

ISP Boot Program Start Conditions

Setting the ISP page configuration to a value other than 0 will cause the processor to jump to the base address of the ISP boot code when a hardware reset is performed (provided that the value FFh is present at program address 0000h).

An alternate way to force the CRD89C512RD to jump to the ISP boot program is to maintain pins P2.6 and P2.7 or pin P4.3 at a low logic level during a hardware reset, as shown in the diagram below:

FIGURE 2: CRD89C512RD ALTERNATE ISP BOOT PROGRAM ACCESS



The ISP boot program can also be accessed via the LJMP instruction.

When the ISP page configuration is set to 0 while the device is being programmed with a parallel programmer, the ISP boot feature will be disabled.

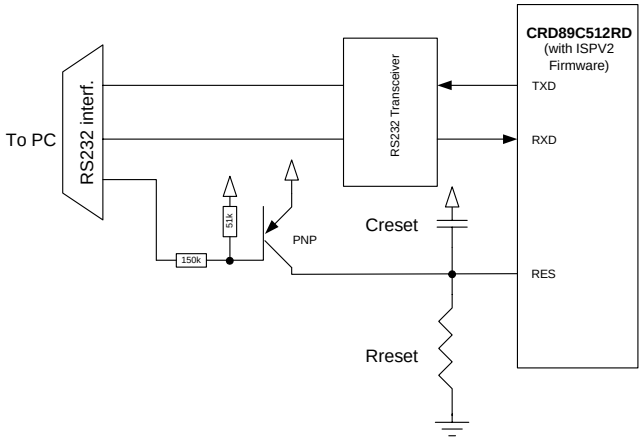
CRD89C512RD ISPVx Firmware Boot Program

An ISP boot loader program is available for the CRD89C512RD. (ISPVx Firmware, x = revision, see Cyrod website for latest revision) that resides in locations F200h to FFFFh in the upper 3.5KB of the CRD89C512RD Program Flash memory. The ISPVx Firmware enables In-System-Programming of the CRD89C512RD on the final application PCB using the UART interface.

The CRD89C512RD can be ordered with or without the ISPVx bootloader firmware (see the ordering information section of this datasheet for part number information).

See the following figure for a hardware configuration example. Other configurations are also possible.

FIGURE 3: CRD89C512RD INTERFACE FOR IN-SYSTEM PROGRAMMING



Visit the Cyrod web site to download the "Versa Ware ISP" Window™'s application, which enables communication with the ISPVx firmware.

The ISPVx bootloader firmware can also be programmed into the CRD89C512RD by the user. Source code is included with the Versa Ware ISP application software.

For more information on the ISPVx firmware, please consult the "CRD89C512RD ISPVx Firmware User Guide.pdf," available on the Cyrod web site.

Note: The current ISPVx firmware and Versa Ware software does not allow CRD89C512RD Data Flash programming. Future versions of both will provide support for CRD89C512RD Data Flash programming.

CRD89C512RD IAP Feature

The CRD89C512RD IAP feature allows the processor to self-program its program and data Flash memory from within the user program.

Five SFR registers serve to control the IAP operation. The description of these registers is provided below.

System Control Register

The system control register controls the activation of the data Flash and the expanded SRAM and serves to monitor the watchdog timer status.

TABLE 6: SYSTEM CONTROL REGISTER (SYSCON) – SFR BFH

7	6	5	4	3	2	1	0
WDR	Unused			DFLASHE	IAPE	XRAME	ALEI

Bit	Mnemonic	Description
7	WDR	This is the watchdog timer reset bit. It will be set to 1 when the reset signal generated by WDT overflows.
6	Unused	-
5	Unused	-
4	Unused	-
3	DFLASHE	Data Flash memory Enable 0: Data Flash is Disabled 1: Data Flash is Enabled
2	IAPE	IAP function enable bit 0: IAP is Disabled 1: ISP is Enabled
1	XRAME	768 byte on-chip enable bit
0	ALEI	ALE output inhibit bit, which is used to reduce EMI. 0: ALE active 1: ALE activity is inhibited

The WDR bit of the SYSCON register indicates whether the system has been reset due to the overflow of the watchdog timer. For this reason, users should check the WDR bit whenever an unexpected reset occurs.

Setting the DFLASHE bit of the SYSCON register to 1 activates the 64KB on-chip data Flash memory, which is disabled by default.

The IAPE bit is used to activate the IAP function.

When set to 1, the XRAME bit enables the expanded 768 bytes of SRAM. Bit 0 of this register is the ALE output inhibit bit. Setting this bit to 1 will inhibit the Fosc/6Hz clock signal output to the ALE pin.

IAP Flash Address and Data Registers

The IAPFADHI and IAPADLO registers are used to specify at which address the IAP function will be performed.

TABLE 7:IAP FLASH ADDRESS HIGH (IAPFADHI) - SFR F4H

7	6	5	4	3	2	1	0
IAPFADHI[15:8]							

TABLE 8:IAP FLASH ADDRESS LOW (IAPFADLO) - SFR F5H

7	6	5	4	3	2	1	0
IAPFADLO[15:8]							

The IAPFDATA SFR register contains the data byte required to perform the IAP function.

TABLE 9:IAP FLASH DATA REGISTER (IAPFDATA) - SFR F6H

7	6	5	4	3	2	1	0
IAPFDATA[7:0]							

IAP Flash Control Register

The CRD89C512RD's IAP function operation is controlled by the IAP Flash control register, IAPFCTRL.

TABLE 10:IAP FLASH CONTROL REGISTER (IAPFCTRL) - SFR F7H

7	6	5	4	3	2	1	0
IAPFCTRL[15:8]							

Bit	Mnemonic	Description
7	IAPSTART	IAP Selected operation Start sequence
6	Unused	-
5	FZONE	Flash zone select for IAP Flash operations: 0: Flash Program Zone 1: Flash Data Zone
4	Unused	-
3	Unused	-
2	Unused	-
1	IAPFCT[1:0]	Flash Memory IAP Function (see below)
0		

CRD89C512RD IAP operations can be performed in either the 64KB Flash program memory zone or the 64KB data Flash memory zone. The FZONE bit selects the area in which the IAP operations will be performed and acts as the 17th bit of the 128KB Flash address.

FZONE = 0: IAP functions target program Flash
FZONE = 1: IAP functions target data Flash

Setting the IAPSTART bit to 1 starts the execution of the IAP command specified by the IAPFCT[1:0] bits of the IAP Flash control register.

If the IAPSTART bits equal 0, no IAP operations will be performed.

The IAP subsystem handles four different functions. The IAP function performed is controlled by the IAPFCT bits, as shown below:

TABLE 11:IAP FUNCTIONS

IAPFCT[1:0] Bits value	IAP Function
00	Flash Byte Program
01	Flash Erase Protect
10	Flash Page Erase
11	Flash Erase

When activated, the Flash Erase function will erase the entire CRD89C512RD Flash memory except for the ISP boot program, if the ISP config bits (lock) have been activated. Be careful when performing Flash Erase under final application program control.
Note that for security reasons, the IAPSTART bit of the IAPFCTRL register is configured as read-only by default.

To set the IAPSTART to 1, the following operation sequence must be performed first:

```
MOV    IAPFDATA,#55h
MOV    IAPFDATA,#AAh
MOV    IAPFDATA,#55h
```

Once the start bit is set to 1, the IAP subsystem will read the contents of the IAP Flash address and data registers and hold the CRD89C512RD program counter at its current value until the IAP operation is complete. When the IAP operation is complete, the IAPSTART bit will be cleared and the program will continue executing.

IAP Byte Program in the CRD89C512RD Program Flash

The IAP byte program function is used to program a byte into a specified program memory location under the control of the IAP feature. See the following program example:

```
IAP_PROG:       MOV     IAPFDATA,#55H     ;Sequence to
Enable Writing
        MOV     IAPFDATA,#0AAH  ; the IAPSTART bit
        MOV     IAPFDATA,#55H

        MOV     SYSCON,#04H       ;ENABLE IAP
FUNCTION
        MOV     IAPFADHI, FADRSH          ;Set MSB of
address  to program
        MOV     IAPFADLO,FADRSL           ;Set LSB of
address  to program
        MOV     IAPFDATA,FDATA  ;Set Data to Program
        MOV     IAPFCTRL,#80H             ;Set the IAP
Start bit + Byte Program
        ;**The program Counter will stop until the IAP function is
completed
```

IAP Byte Program in the CRD89C512RD Data Flash

The IAP byte program function can also be used to program a byte into a specified data Flash memory location under the control of the IAP feature. See the following program example:

```
IAP_PROG:       MOV     IAPFDATA,#55H     ;Sequence to
Enable Writing
        MOV     IAPFDATA,#0AAH  ; the IAPSTART bit
        MOV     IAPFDATA,#55H

        MOV     SYSCON,#0CH       ;ENABLE IAP
                FUNCTION + Enable
                                  ;Data Flash
        MOV     IAPFADHI, FADRSH          ;Set MSB of
address  to program
        MOV     IAPFADLO,FADRSL           ;Set LSB of
address  to program
        MOV     IAPFDATA,FDATA  ;Set Data to Program
        MOV     IAPFCTRL,#A0H             ;Set the IAP
Start bit + FZONE bit
        ;**The program Counter will stop until the IAP function is
completed
```

IAP Page Erase Function

By using the IAP feature, it is possible to perform a page erase of the CRD89C512RD program or data Flash memory (note that the memory area occupied by the ISP boot program cannot be page erased). Each page is 512 bytes in size.

To perform a Flash page erase, the page address is specified by the XY (hex) value written into the IAPFADHI register. (The value 00h must be written into the IAPFADLO registers.)

If the "Y" portion of the IAPFADHI register represents an even number, the page that will be erased corresponds to the range XY00h to X(Y+1)FFh.

If the "Y" portion of the IAPFADHI register represents an odd number, the page that will be erased corresponds to the range X(Y-1)00h to XYFFh.

The following program example demonstrates how to erase the page corresponding to the address B000h-CFFFh in the program memory zone:

```
;** Erase Flash Program page located at address B000h to CFFFh.
PageErase:          MOV     IAPFDATA,#55H     ;Sequence to
Enable Writing
          MOV       IAPFDATA,#0AAH  ; the IAPSTART bit
          MOV       IAPFDATA,#55H

          MOV       SYSCON,#04H       ;Enable IAP
          MOV       IAPFADHI, #0B0h   ;Set MSB of  Page address
to erase
          MOV       IAPFADLO,#00h     ;Set LSB of address  = 00
          MOV       IAPFCTRL,#82H               ;Set the IAP
Start Bit
```

The following example shows how to erase the same page in the data Flash memory zone:

```
;** Erase Flash Data page located at address B000h to CFFFh.
PageErase:          MOV     IAPFDATA,#55H     ;Sequence to
Enable Writing
          MOV       IAPFDATA,#0AAH  ; the IAPSTART bit
          MOV       IAPFDATA,#55H

          MOV       SYSCON,#0CH       ;Enable IAP + Data Flash
          MOV       IAPFADHI, #0B0h   ;Set MSB of  Page address
to erase
          MOV       IAPFADLO,#00h     ;Set LSB of address  = 00
          MOV       IAPFCTRL,#A2H               ;Set The IAP
Start bit + FZONE bit
```

IAP Chip Erase Function

The IAP chip erase function will erase the entire Flash memory contents with the exception of the ISP boot program area. Running this function will also automatically unprotect the Flash memory.

IAP Chip Protect Function

When the chip protect function is enabled, values read back from Flash memory will be 00h.

ISP/AIP operation Durations

The following table shows the duration of the ISP/IAP operations for an oscillator clock of 40MHz.

Operation	Max Duration (Fosc = 40MHz)
Byte Program	30us
Page Erase	10ms
Chip Erase	3sec
Chip Protect	400us

All ISP/IAP operations require a supply voltage of 5V to be executed properly.

Program Status Word Register

The PSW register is a bit addressable register that contains the status flags (CY, AC, OV, P), user flag (F0) and register bank select bits (RS1, RS0) of the 8051 processor.

TABLE 12: PROGRAM STATUS WORD REGISTER (PSW) - SFR DOH

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	-	P

Bit	Mnemonic	Description
7	CY	Carry Bit
6	AC	Auxiliary Carry Bit from bit 3 to 4.
5	F0	User definer flag
4	RS1	R0-R7 Registers bank select bit 0
3	RS0	R0-R7 Registers bank select bit 1
2	OV	Overflow flag
1	-	-
0	P	Parity flag

RS1	RS0	Active Bank	Address
0	0	0	00h-07h
0	1	1	08h-0Fh
1	0	2	10h-17h
1	1	3	18-1Fh

Data Pointer

The CRD89C512RD has one 16-bit data pointer. The DPTR is accessed via two SFR addresses: DPL located at address 82h and DPH located at address 83h.

Stack Pointer

The stack pointer (SP) is a register located at address 81h of the SFR register area whose value corresponds to the address of the last item that was put on the processor stack. Each time new data is put on the SP, the value of the stack pointer is incremented.

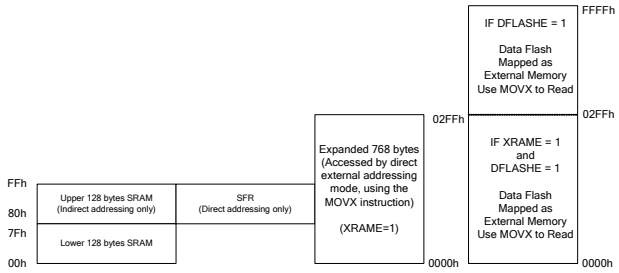
By default, the stack pointer value is 07h, but it is possible to program the processor stack pointer to point anywhere in the 00h to FFh range of SRAM memory. When a function call is performed or an interrupt is serviced, the 16-bit return address (2 bytes) is stored on the stack. Data can be placed manually on the stack by using the PUSH and POP functions.

Data Memory

The CRD89C512RD has 1KB of on-chip SRAM: 256 bytes are configured like the internal memory structure of a standard 8052, while the remaining 768 bytes can be accessed using external memory addressing (MOVX).

The CRD89C512RD also includes a large block of 64KB of data Flash that is mapped on the processor's external memory bus for read access.

FIGURE 4: CRD89C512RD DATA MEMORY STRUCTURE



By default, after reset the expanded SRAM area and the data Flash areas are disabled. They are enabled by setting the XRAME and the DFLASHE bits (respectively) of the SYSCON register located at address BFh in the SFR.

The DFLASHE and XRAME bits of the SYSCON register define which area the MOVX instruction will target:

DFLASHE	XRAME	MOVX <= 2FFh	MOVX > 2FFh
0	0	Ext. Memory	Ext. Memory
0	1	Int. SRAM	Ext. Memory
1	0	Int. Data Flash	Int. Data Flash
1	1	Int. SRAM	Int. Data Flash

Lower 128 bytes (00h to 7Fh, Bank 0 & Bank 1)
The lower 128 bytes of data memory (from 00h to 7Fh) is summarized as follows:

- Address range 00h to 7Fh can be accessed in direct and indirect addressing modes
- Address range 00h to 1Fh includes R0-R7 register areas
- Address range 20h to 2Fh is bit addressable
- Address range 30h to 7Fh is not bit addressable and can be used for general-purpose storage

Upper 128 bytes (80h to FFh, Bank 2 & Bank 3)
The upper 128 bytes of the data memory ranging from 80h to FFh can be accessed using indirect addressing or by using the bank mapping in direct addressing mode.

Expanded SRAM Access Using the MOVX @DPTR Instruction (0000-02FF, Bank4-Bank15)

The 768 bytes of expanded SRAM data memory occupies addresses 0000h to 02FFh. This can be accessed using external direct addressing (i.e. the MOVX instruction) or bank mapping direct addressing. When indirect addressing executes the *MOVX @DPTR* instruction, if the address is larger than 02FFh and the data Flash is disabled (DFLASHE=0), the CRD89C512RD will access off-chip memory in the external memory space using the external memory control signals.

MPAGE Register (Extra Read Data Pointer)

The CRD89C512RD features a second data pointer called MPAGE, which is dedicated to data Flash and external SRAM read access using the MOVX @Ri (I=0,1) instruction. The MPAGE register provides the high byte of the address, while the contents of the Ri register provides the low byte of the address. The operation of the MPAGE register resembles that of the MOVX @DPTR instruction, but is limited as a read function. The MPAGE register default setting is 00h.

TABLE 13: MPAGE REGISTER (MPAGE) - SFR 85H

7	6	5	4	3	2	1	0
MPAGE[7:0]							

Data Bank Control Register

The DBANK register enables the data bank select function to map the entire contents of the SRAM memory in the range of 40h to 7Fh for applications that require direct addressing of the expanded SRAM contents.

The data bank select function is activated by setting the data bank select enable bit (BSE) to 1. Setting this bit to zero disables the function. The lower nibble of this register controls the mapping of the entire 1KB bytes on-chip SRAM space into the 040h-07Fh range.

TABLE 14: DATA BANK CONTROL REGISTER (DBANK) – SFR 86H

7	6	5	4	3	2	1	0
BSE	Unused			BS3	BS2	BS1	BS0

Bit	Mnemonic	Description
7	BSE	Data Bank Select Enable Bit BSE=1, Data Bank Select enabled BSE=0, Data Bank Select disabled
6	Unused	-
5	Unused	-
4	Unused	-
3	BS3	Allows the mapping of the 1KB SRAM into the 040h - 07Fh SRAM space
2	BS2	
1	BS1	
0	BS0	

Windowed access to the entire 1KB of on-chip SRAM in the range of 40h-7Fh is described in the following table.

TABLE 15: BANK MAPPING DIRECT ADDRESSING MODE

BS3	BS2	BS1	BSO	040h~07fh mapping address	Note
0	0	0	0	000h-03Fh	Lower 128 bytes SRAM
0	0	0	1	040h-07Fh	Lower 128 bytes SRAM
0	0	1	0	080h-0BFh	Upper 128 bytes SRAM
0	0	1	1	0C0h-0FFh	Upper 128 bytes SRAM
0	1	0	0	0000h-003Fh	On-chip expanded 768 bytes SRAM
0	1	0	1	0040h-007Fh	On-chip expanded 768 bytesRAM
0	1	1	0	0080h-00BFh	On-chip expanded 768 bytes SRAM
0	1	1	1	00C0h-00FFh	On-chip expanded 768 bytes SRAM
1	0	0	0	0100h-013Fh	On-chip expanded 768 bytes SRAM
1	0	0	1	0140h-017Fh	On-chip expanded 768 bytes SRAM
1	0	1	0	0180h-01BFh	On-chip expanded 768 bytes SRAM
1	0	1	1	01C0h-01FFh	On-chip expanded 768 bytes SRAM
1	1	0	0	0200h-023Fh	On-chip expanded 768 bytes SRAM
1	1	0	1	0240h-027Fh	On-chip expanded 768 bytes SRAM
1	1	1	0	0280h-02BFh	On-chip expanded 768 bytes SRAM
1	1	1	1	02C0h-02FFh	On-chip expanded 768 bytes SRAM

Example: User writes #55h to address 203h:

```
MOV   DBANK, #8CH      ;Set bank mapping 40h-07Fh to 0200h-023Fh
MOV   A, #55H          ;Store #55H to A
MOV   43H, A           ;Write #55H to 0203h address
```

Power Control Register

The CRD89C512RD provides two power saving modes: Idle and Power Down, which are controlled by the PDOWN and IDLE bits of the PCON register at address 87h.

TABLE 16: POWER CONTROL REGISTER (PCON) - SFR 87H

7	6	5	4	3	2	1	0
Unused						RAMS1	RAMS0

Bit	Mnemonic	Description
7	SMOD	1: Double the baud rate of the serial port frequency that was generated by Timer 1. 0: Normal serial port baud rate generated by Timer 1.
6		
5		
4		
3	GF1	General Purpose Flag
2	GF0	General Purpose Flag
1	PDOWN	Power Down mode control bit
0	IDLE	Idle mode control bit

In Idle mode, the processor is stopped but the oscillator continues to run. The content of the SRAM, I/O state and SFR registers are maintained and the Timer and external interrupts are left operational. The processor will be woken up when an external event, triggering an interrupt, occurs.

In Power Down mode, the oscillator and the peripherals are disabled. The contents of the SRAM and the SFR registers, however, are maintained. The only way to exit from the Power Down mode is via a hardware reset (note that the watchdog timer is stopped in Power Down).

When the CRD89C512RD is in Power Down, its current consumption drops to about 50uA.

The SMOD bit of the PCON register controls the oscillator divisor applied to Timer 1 when used as a baud rate generator for the UART. Setting this bit to 1 doubles the UART's baud rate generator frequency.

Input/Output Ports

The CRD89C512RD has 36 bi-directional lines grouped into four 8-bit I/O ports and one 4-bit I/O port. These I/Os can be individually configured as inputs or outputs.

With the exception of the P0 I/Os, which are of the open drain type, each I/O consists of a transistor connected to ground and a weak, transistor-based pull-up resistor.

Writing a 0 in a given I/O port bit register will activate the transistor connected to Vss and bring the I/O to a low level.

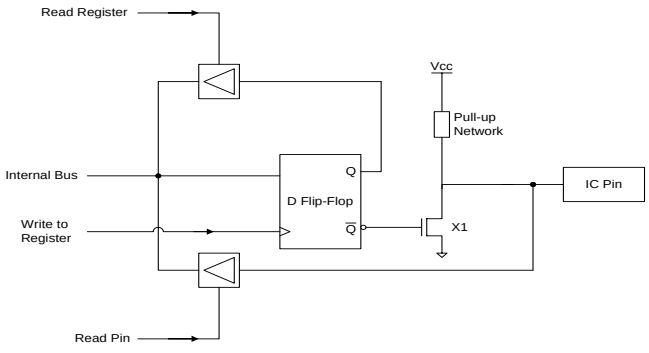
Writing a 1 into a given I/O port bit register deactivates the transistor between the pin and ground. In this case, an internal weak pull-up resistor will bring the pin to a high level (except for Port 0, which is open-drain).

To use a given I/O as an input, a 1 must be written into its associated port register bit. By default, upon reset all the I/Os are configured as inputs. The CRD89C512RD I/O ports are not designed to source current.

Structure of the P1, P2, P3 and P4 Ports

The following figure demonstrates the general structure of the P1, P2, P3 and P4 port I/Os. For these ports, the output stage is composed of a transistor (X1) and a transistor set configured as a weak pull-up. Note that the figure below does not show the intermediary logic that connects the register's output and the output stage because this logic varies with the auxiliary function of each port.

FIGURE 5: GENERAL STRUCTURE OF THE OUTPUT STAGE OF P1, P2, P3 AND P4



Each line may be used independently as a logical input or output. When used as an input, the corresponding bit register must be high.

The transistor would be off (open-circuited) and current would flow from the VCC to the pin, generating a logical high at the output. Note that if an external device with a logical low value is connected to the pin, the current will flow out of the pin.

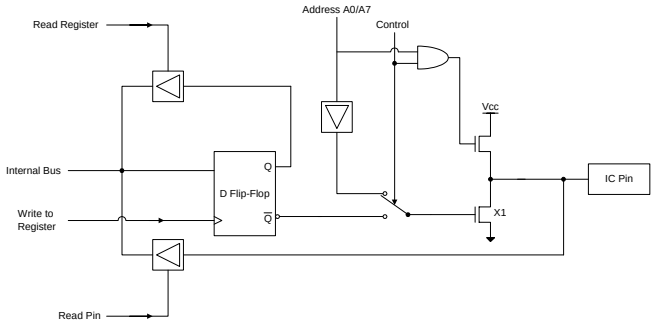
The presence of the pull-up resistance, even when the I/O's are configured as inputs, means that a small current is likely to flow from the CRD89C512RD I/O's pull-up resistors to the driving circuit when the inputs are driven low. For this reason, the CRD89C512RD I/O ports P1, P2, P3 and P4 are called "quasi bi-directional".

Structure of Port 0

The internal structure of P0 is shown in the next figure. The auxiliary function of this port requires a particular logic. As opposed to the other ports, P0 is truly bi-directional. In other words, when used as an input, it is considered to be in a floating logical state (high impedance state). This arises from the absence of the internal pull-up resistance. The pull-up resistance is actually replaced by a transistor that is only used when the port is configured to access external memory/data bus (EA=0).

When used as an I/O port, P0 acts as an open drain port and the use of an external pull-up resistor is likely to be required for most applications.

FIGURE 6: PORT P0'S PARTICULAR STRUCTURE



When P0 is used as an external memory bus input (for a MOVX instruction, for example), the outputs of the register are automatically forced to 1.

The bit addressable P0 register, located at address 80h, controls the P0 individual pin directions when used as I/Os (see the following table).

TABLE 17: PORT 0 REGISTER (P0) - SFR 80H

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Bit	Mnemonic	Description
7	P0.7	For each bit of the P0 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V.
6	P0.6	
5	P0.5	
4	P0.4	
3	P0.3	
2	P0.2	
1	P0.1	
0	P0.0	

Port 2

Port P2 is similar to ports 1 and 3, the difference being that P2 is used to drive the A8-A15 lines of the address bus when the EA line of CRD89C512RD is held low at reset time or when a MOVX instruction is executed.

Like the P0, P1 and P3 registers, the P2 register is bit addressable.

TABLE 18: PORT 2 REGISTER (P2) - SFR A0H

7	6	5	4	3	2	1	0
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

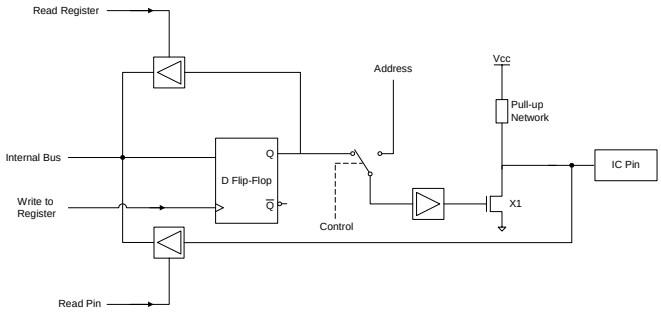
Bit	Mnemonic	Description
7	P2.7	For each bit of the P2 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V.
6	P2.6	
5	P2.5	
4	P2.4	
3	P2.3	
2	P2.2	
1	P2.1	
0	P2.0	

Port P0 and P2 as Address and Data Bus

The output stage may receive data from two sources:

- The outputs of register P0 or the bus address itself multiplexed with the data bus for P0
- The outputs of the P2 register or the high byte (A8 through A15) of the bus address for the P2 port

FIGURE 7: P2 PORT STRUCTURE



When the ports are used as an address or data bus, special function registers P0 and P2 are disconnected from the output stage, the 8 bits of the P0 register are forced to 1 and the contents of the P2 register remains constant.

Port 1

The P1 register controls the direction of the Port 1 I/O pins. Writing a 1 into the P1.x bit (see the following table) of the P1 register configures the bit as an output, presenting a logic 1 to the corresponding I/O pin or enables use of the I/O pin as an input. Writing a 0 activates the output "pull-down" transistor, which will force the corresponding I/O line to a logic low.

TABLE 19: PORT 1 REGISTER (P2) - SFR 90H

7	6	5	4	3	2	1	0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Bit	Mnemonic	Description
7	P1.7	For each bit of the P1 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up bring the I/O to 5V.
6	P1.6	
5	P1.5	
4	P1.4	
3	P1.3	
2	P1.2	
1	P1.1	
0	P1.0	

Auxiliary Port 1 Functions

The Port 1 I/O pins are shared with the PWM outputs, Timer 2 EXT and T2 inputs, as shown below:

Pin	Mnemonic	Function
P1.0	T2	Timer 2 counter input
P1.1	T2EX	Timer 2 Auxiliary input
P1.2		
P1.3	PWM0	PWM0 output
P1.4	PWM1	PWM1 output
P1.5	PWM2	PWM2 output
P1.6	PWM3	PWM3 output
P1.7	PWM4	PWM4 output

Port 3

The Port 3 structure is similar that of Port 1.

TABLE 20: PORT 3 REGISTER (P3) - SFR B0H

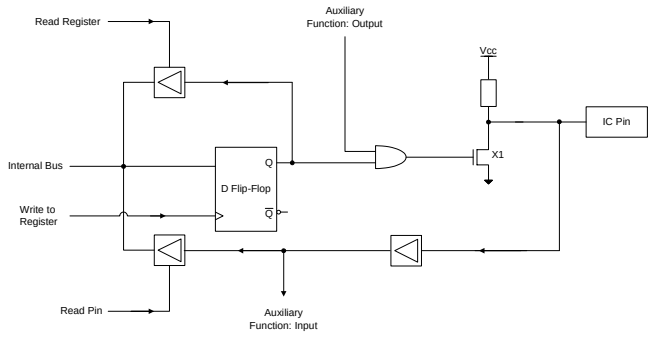
7	6	5	4	3	2	1	0
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Bit	Mnemonic	Description
7	P3.7	For each bit of the P3 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V. To configure P3 pins as input or use alternate P3 function the corresponding bit must be set to 1.
6	P3.6	
5	P3.5	
4	P3.4	
3	P3.3	
2	P3.2	
1	P3.1	
0	P3.0	

Auxiliary P3 Port Functions

The Port 3 I/O pins are shared with the UART interface, INT0 and INT1 interrupts, Timer 0 and Timer 1 inputs and the #WR and #RD lines when external memory accesses are performed.

FIGURE 8: P3 PORT STRUCTURE



The following table describes the auxiliary functions of the Port 3 I/O pins.

TABLE 21: P3 AUXILIARY FUNCTION TABLE

Pin	Mnemonic	Function
P3.0	RXD	Serial Port: Receive data in asynchronous mode. Input and output data in synchronous mode.
P3.1	TXD	Serial Port: Transmit data in asynchronous mode. Output clock value in synchronous mode.
P3.2	$\overline{\text{INT0}}$	External Interrupt 0 Timer 0 Control Input
P3.3	$\overline{\text{INT1}}$	External Interrupt 1 Timer 1 Control Input
P3.4	T0	Timer 0 Counter Input
P3.5	T1	Timer 1 Counter Input
P3.6	$\overline{\text{WR}}$	Write signal for external memory
P3.7	$\overline{\text{RD}}$	Read signal for external memory

Port 4

Port 4 has four related I/O pins and its port address is located at 0D8H.

TABLE 22: PORT 4 (P4) - SFR D8H

7	6	5	4	3	2	1	0
Unused				P4.3	P4.2	P4.1	P4.0

Bit	Mnemonic	Description
7	Unused	-
6	Unused	-
5	Unused	-
4	Unused	-
3	P4.3	Used to output the setting to pins P4.3, P4.2, P4.1, P4.0 respectively.
2	P4.2	
1	P4.1	
0	P4.0	

Software Port Control

Some instructions allow the user to read the logic state of the output pin, while others allow the user to read the contents of the associated port register. These instructions are called *read-modify-write* instructions. A list of these instructions is found in the following table.

Upon execution of these instructions, the content of the port register (at least 1 bit) is modified. The other read instructions take the present state of the inputs into account. For example, instruction ANL P3,#01h obtains the value in the P3 register; performs the desired logic operation with the constant 01h; and recopies the result into the P3 register. When users want to take the present state of the inputs into account, they must first read these states and perform an AND operation between the read value and the constant.

```
MOV A, P3; State of the inputs in the accumulator
ANL A, #01; AND operation between P3 and 01h
```

When the port is used as an output, the register contains information on the state of the output pins. Measuring the state of an output directly on the pin is inaccurate because the electrical level depends mostly on the type of charge that is applied to it. The functions shown next take the value of the register rather than that of the pin.

TABLE 23: LIST OF INSTRUCTIONS THAT READ AND MODIFY THE PORT USING REGISTER VALUES

Instruction	Function
ANL	Logical AND ex: ANL P0, A
ORL	Logical OR ex: ORL P2, #01110000B
XRL	Exclusive OR ex: XRL P1, A
JBC	Jump if the bit of the port is set to 0
CPL	Complement one bit of the port
INC	Increment the port register by 1
DEC	Decrement the port register by 1
DJNZ	Decrement by 1 and jump if the result is not equal to 0
MOV P.,C	Copy the held bit C to the port
CLR P.x	Set the port bit to 0
SETB P.x	Set the port bit to 1

Port Operation Timing

Writing to a Port (Output)

When an operation results in a modification of the content in a port register, the new value is placed at the output of the D flip-flop during the last machine cycle that the instruction needed to execute.

Reading a Port (Input)

To be sampled, the signal duration present on the I/O inputs must be longer than Fosc/12.

I/O Ports Driving Capability

The maximum allowable continuous current that the device can sink on an I/O port is described in the following table:

Maximum sink current on one given I/O	10mA
Maximum total sink current for P0	26mA
Maximum total sink current for P1, 2, 3	15mA
Maximum total sink current on all I/O	71mA

It is not recommended to exceed the sink currents outlined in the above table. Doing so will likely make the low-level output voltage exceed device specifications and affect device reliability.

The CRD89C512RD I/O ports are not designed to source current.

CRD89C512RD Timers

The CRD89C512RD includes three 16-bit timers: Timer 0, Timer 1 and Timer 2.

The Timers can operate in two modes:

- Event counting mode
- Timer mode

When operating in event counting mode, the counter is incremented each time an external event, such as a transition in the logical state of the timer input (T0, T1, T2 input), is detected. When operating in timer mode, the counter is incremented by the microcontroller's system clock (Fosc/12) or by a divided version of it.

Timer 0 and Timer 1

Timers 0 and 1 have four modes of operation. These modes allow the user to change the size of the counting register or to authorize an automatic reload when provided with a specific value. Timer 1 can also be used as a baud rate generator to generate communication frequencies for the serial interface.

Timers 1 and 0 are configured by the TMOD and TCON registers.

TABLE 24: TIMER MODE CONTROL REGISTER (TMOD) – SFR 89H

7	6	5	4	3	2	1	0
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0

Bit	Mnemonic	Description
7	GATE1	1: Enables external gate control (pin INT1 for Counter 1). When INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T1IN input pin.
6	C/T1	Selects timer or counter operation (Timer 1). 1 = A counter operation is performed 0 = The corresponding register will function as a timer.
5	T1M1	Selects the operating mode of Timer/Counter 1
4	T1M0	
3	GATE0	If set, enables external gate control (pin INT0 for Counter 0). When INT0 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T0IN input pin.
2	C/T0	Selects timer or counter operation (Timer 0). 1 = A counter operation is performed 0 = The corresponding register will function as a timer.
1	T0M1	Selects the operating mode of Timer/Counter 0.
0	T0M0	

The table below summarizes the four modes of operation of timers 0 and 1. The timer operating mode is selected by bits T1M1/T1M0 and T0M1/T0M0 of the TMOD register.

TABLE 25: TIMER/COUNTER MODE DESCRIPTION SUMMARY

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter
0	1	Mode 1	16-bit Counter
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, the value of THx is copied to TLx.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops.

Timer 0, Timer 1 Counter / Timer Functions

Timing Function

When Timer 1 or Timer 0 is configured to operate as a timer, its value is automatically incremented at every machine cycle. Once the timer value rolls over, a flag is raised and the counter acquires a value of zero. The overflow flags (TF0 and TF1) are located in the TCON register.

The TR0 and TR1 bits of the TCON register gate the corresponding timer operation. In order for the timer to run, the corresponding TRx bit must be set to 1.

The IT0 and IT1 bits of the TCON register control the event that will trigger an external interrupt as follows:

IT0 = 0: The INT0, if enabled, occurs if a low level is present on P3.2
IT0 = 1: The INT0, if enabled, occurs if a high to low transition is detected on P3.2
IT1 = 0: The INT1, if enabled, occurs if a low level is present on P3.3
IT1 = 1: The INT1, if enabled, occurs if a high to low transition is detected on P3.3

The IE0 and IE1 bits of the TCON register are external flags that indicate whether a transition has been detected on the INT0 and INT1 interrupt pins, respectively.

If the external interrupt is configured as edge sensitive, the corresponding IE0 and IE1 flags are automatically cleared when the corresponding interrupt is serviced.

If the external interrupt is configured as level sensitive, the corresponding flag must be cleared by the software.

TABLE 26: TIMER 0 AND 1 CONTROL REGISTER (TCON) –SFR 88H

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Mnemonic	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
6	TR1	Timer 1 Run Control Bit. Set/cleared by software to turn Timer/Counter on or off.
5	TF0	Timer 0 Overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
4	TR0	Timer 0 Run Control Bit. Set/cleared by software to turn Timer/Counter on or off.
3	IE1	Interrupt Edge Flag. Set by hardware when external interrupt edge is detected. Cleared when interrupt processed.
2	IT1	Interrupt 1 Type Control Bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
1	IE0	Interrupt 0 Edge Flag. Set by hardware when external interrupt edge is detected. Cleared when interrupt processed.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Counting Function

When operating as a counter, the timer's register is incremented at every falling edge of the T0 and T1 signals located at the input of the timer.

When the sampling circuit sees a high immediately followed by a low in the next machine cycle, the counter is incremented. Two machine cycles are required to detect and record an event. In order to be properly sampled, the duration of the event presented to the timer input should be greater than 1/24 of the oscillator frequency.

Timer 0 / Timer 1 Operating Modes

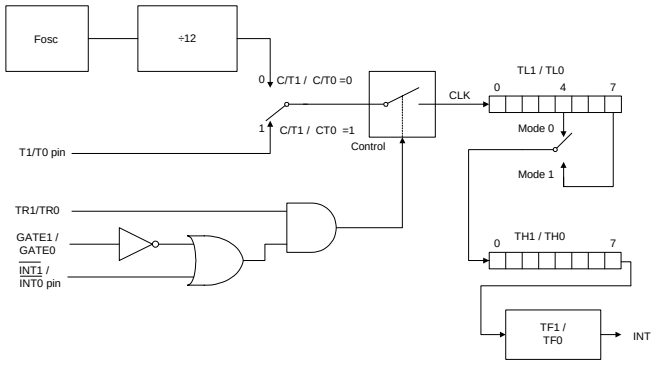
The user may change the operating mode by setting the M1 and M0 bits of the TMOD SFR.

Mode 0

A schematic representation of this mode of operation is presented in the following figure. In Mode 0, the timer operates as a 13-bit counter made up of 5 LSBs of the TLx register and the 8 upper bits of the THx register. When an overflow causes the value of the register to rollover to 0, the TFx interrupt signal goes to 1. The

count value is validated as soon as TRx goes to 1 and the GATE bit is 0, or when INTx is 1.

FIGURE 9: TIMER/COUNTER 1 MODE 0: 13-BIT COUNTER



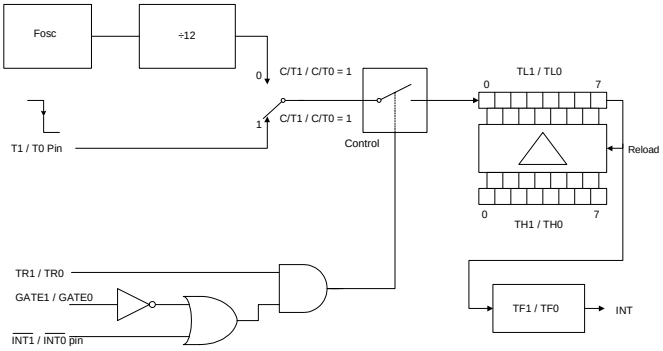
Mode 1

Mode 1 is almost identical to Mode 0, the difference being that in Mode 1, the counter/timer uses the full 16-bits of the timer.

Mode 2

In this Mode, the register of the timer is configured as an 8-bit automatically re-loadable counter/timer. In Mode 2, the lower byte TLx is used as the counter. In the event of a counter overflow, the TFx flag is set to 1 and the value contained in THx, which is preset by software, is reloaded into the TLx counter. The value of THx remains unchanged.

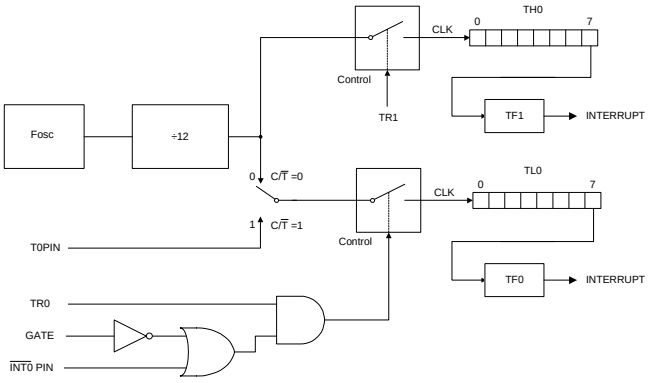
FIGURE 10: TIMER/COUNTER 1 MODE 2: 8-BIT AUTOMATIC RELOAD



Mode 3

In Mode 3, Timer 1 is blocked as if its control bit, TR1, was set to 0. In this mode, Timer 0's registers, TL0 and TH0, are configured as two separate 8-bit counters. The TL0 counter uses Timer 0's control bits (C/T, GATE, TR0, INT0, TF0), and the TH0 counter is held in timer mode (counting machine cycles) and gains control over TR1 and TF1 from Timer 1. At this point, TH0 controls the Timer 1 interrupt.

FIGURE 11: TIMER/COUNTER 0 MODE 3



Timer 2

Timer 2 of the CRD89C512RD is a 16-bit timer/counter and is similar to timers 0 and 1 in that it can operate as either an event counter or a timer. This is controlled by the C/T2 bit in the T2CON special function register. Timer 2 has three operating modes: Auto-Load, Capture, and Baud Rate Generator. These modes are selected via the T2CON. The following table describes the T2CON special function register bits.

TABLE 27: TIMER 2 CONTROL REGISTER (T2CON) –SFR C8H

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Bit	Mnemonic	Description
7	TF2	Timer 2 Overflow Flag: Set by an overflow of Timer 2 and must be cleared by software. TF2 will not be set when either RCLK =1 or TCLK =1.
6	EXF2	Timer 2 external flag change in state occurs when either a capture or reload is caused by a negative transition on T2EX and EXEN2=1. When Timer 2 is enabled, EXF=1 will cause the CPU to Vector to the Timer 2 interrupt routine. Note that EXF2 must be cleared by software.
5	RCLK	Serial Port Receive Clock Source. 1: Causes Serial Port to use Timer 2 overflow pulses for its receive clock in Modes 1 and 3. 0: Causes Timer 1 overflow to be used for the Serial Port receive clock.
4	TCLK	Serial Port Transmit Clock. 1: Causes Serial Port to use Timer 2 overflow pulses for its transmit clock in Modes 1 and 3. 0: Causes Timer 1 overflow to be used for the Serial Port transmit clock.
3	EXEN2	Timer 2 External Mode Enable. 1: Allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the Serial Port. 0: Causes Timer 2 to ignore events at T2EX.
2	TR2	Start/Stop Control for Timer 2. 1: Start Timer 2 0: Stop Timer 2
1	C/$\overline{T2}$	Timer or Counter Select (Timer 2) 1: External event counter falling edge triggered. 0: Internal Timer (OSC/12)
0	CP/$\overline{RL2}$	Capture/Reload Select. 1: Capture of Timer 2 value into RCAP2H, RCAP2L is performed if EXEN2=1 and a negative transitions occurs on the T2EX pin. The capture mode requires RCLK and TCLK to be 0. 0: Auto-reload reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2=1. When either RCK =1 or TCLK =1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

The Timer 2 mode selection bits and their functions are described in the following table:

TABLE 28: TIMER 2 MODE SELECTION BITS

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload Mode
0	1	1	16-bit Capture Mode
1	X	1	Baud Rate Generator Mode
X	X	0	Timer 2 stops

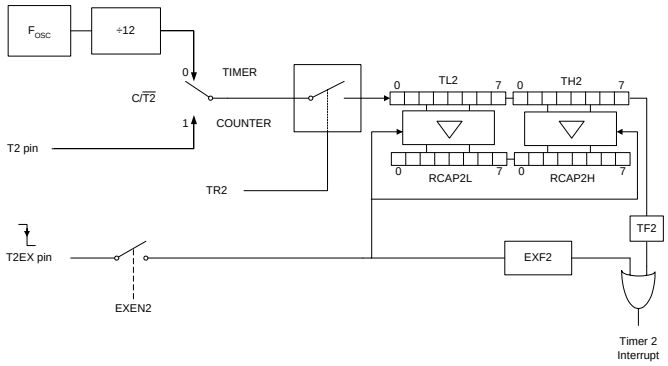
The details of each mode are described in the following sections.

Timer 2 Capture Mode

In capture mode, the EXEN2 bit of the T2CON register controls whether an external transition on the T2EX pin will trigger the capture of the timer value.

When EXEN2 = 0, the Timer 2 acts as a 16-bit timer/counter, which, upon overflowing, will set the TF2 bit (Timer 2 overflow bit). This overflow can be used to generate an interrupt.

FIGURE 12: TIMER 2 IN CAPTURE MODE



When EXEN2 = 1, the above still applies, however, in addition, it is possible to allow a 1 to 0 transition at the T2EX input to cause the current value stored in the Timer 2 registers (TL2 and TH2) to be captured into the RCAP2L and RCAP2H registers. Furthermore, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Note that both EXF2 and TF2 share the same interrupt vector.

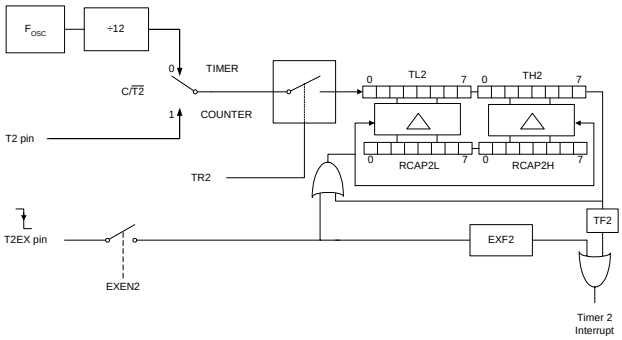
Timer 2 Auto-Reload Mode

In this mode, there are also two options controlled by the EXEN2 bit in the T2CON register.

If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2, but also causes the Timer 2 registers to be reloaded with the 16-bit value in the RCAP2L and RCAP2H registers previously initialised. In this mode, Timer 2 can be used as a baud rate generator source for the serial port.

If EXEN2=1, then Timer 2 still performs the above operation, but a 1 to 0 transition at the external T2EX input will also trigger an anticipated reload of Timer 2 with the value stored in RCAP2L, RCAP2H and set EXF2.

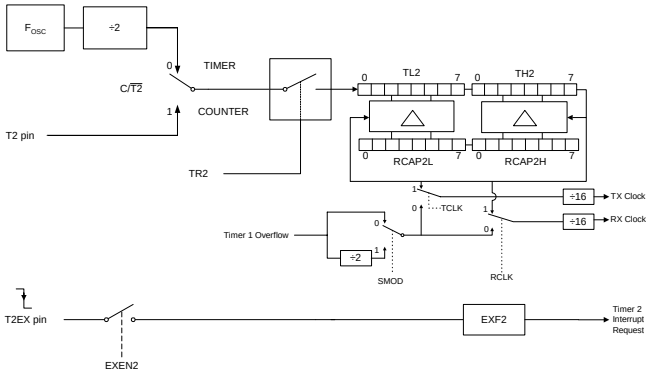
FIGURE 13: TIMER 2 IN AUTO-RELOAD MODE



Timer 2 Baud Rate Generator Mode

Timer 2 can be used for UART Baud Rate generation. This mode is activated when RCLK is set to 1 and/or TCLK is set to 1. This mode is described further in the serial port section.

FIGURE 14: TIMER 2 IN AUTOMATIC BAUD GENERATOR MODE



UART Serial Port

The serial port on the CRD89C512RD can operate in full duplex (it can transmit and receive data simultaneously.) This occurs at the same speed if one timer is assigned as the clock source for both transmission and reception, and at different speeds if transmission and reception are each controlled by their own timer.

The CRD89C512RD serial port includes a double buffer for the receiver, which allows reception of a byte even if the previously received byte has not been retrieved from the receive register by the processor. However, if the first byte still has not been read by the time reception of the second byte is complete, the byte present in the receive buffer will be lost.

The SBUF register provides access to the transmit and receive registers of the serial port. Reading from the SBUF register will access the receive register, while a write to the SBUF loads the transmit register.

Serial Port Control Register

The SCON (serial port control) register contains control and status information, and includes the 9th data bit for transmit/receive (TB8/RB8 if required), mode selection bits and serial port interrupt bits (TI and RI).

TABLE 29: SERIAL PORT CONTROL REGISTER (SCON) – SFR 98H

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit	Mnemonic	Description
7	SM0	Bit to select mode of operation (see next table)
6	SM1	Bit to select mode of operation (see next table)
5	SM2	Multiprocessor communication is possible in Modes 2 and 3. In Modes 2 or 3 if SM2 is set to 1, RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received.
4	REN	Serial Reception Enable Bit This bit must be set by software and cleared by software. 1: Serial reception enabled 0: Serial reception disabled
3	TB8	9th data bit transmitted in Modes 2 and 3 This bit must be set by software and cleared by software.
2	RB8	9th data bit received in modes 2 and 3. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, this bit is not used. This bit must be cleared by software.
1	TI	Transmission Interrupt flag. Automatically set to 1 when: • The 8th bit has been sent in Mode 0. • Automatically set to 1 when the stop bit has been sent in the other modes. This bit must be cleared by software.
0	RI	Reception Interrupt flag Automatically set to 1 when: • The 8th bit has been received in Mode 0. • Automatically set to 1 when the stop bit has been sent in the other modes (see SM2 exception). This bit must be cleared by software.

TABLE 30: SERIAL PORT MODES OF OPERATION

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift Register	$F_{osc}/12$
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	$F_{osc}/64$ or $F_{osc}/32$
1	1	3	9-bit UART	Variable

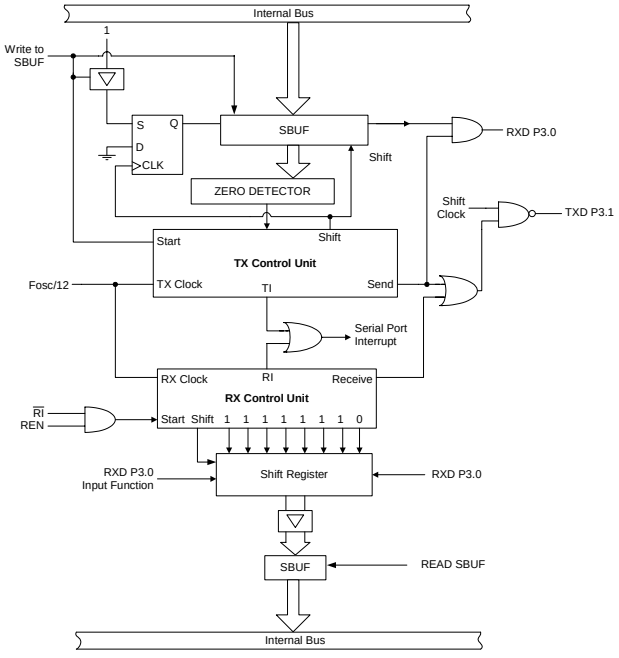
UART Operating Modes

The CRD89C512RD's serial port can operate in four different modes. In all four modes, a transmission is initiated by an instruction that uses the SBUF register as a destination register. In Mode 0, reception is initiated by setting RI to 0 and REN to 1. An incoming start bit initiates reception in the other modes, provided that REN is set to 1. The following paragraphs describe these four modes.

UART Operation in Mode 0

In this mode, the serial data exits and enters through the RXD pin. TXD is used to output the shift clock. The signal is composed of 8 data bits starting with the LSB. The baud rate in this mode is 1/12 the oscillator frequency.

FIGURE 15: SERIAL PORT MODE 0 BLOCK DIAGRAM



UART Transmission in Mode 0

Any instruction that uses SBUF as a destination register may initiate a transmission. The "write to SBUF" signal also loads a 1 into the 9th position of the transmit shift register and informs the TX control block to begin a transmission. The internal timing is such that one full machine cycle will elapse between a write to SBUF instruction and the activation of SEND.

The SEND signal enables the output of the shift register to the alternate output function line of P3.0 and enables SHIFT CLOCK to the alternate output function line of P3.1.

At every machine cycle in which SEND is active, the contents of the transmit shift register are shifted to the right by one position.

Zeros come in from the left as data bits shift out to the right. The TX control block sends its final shift and deactivates SEND while setting T1 after one condition is fulfilled: When the MSB of the data byte is at the output position of the shift register; the 1 that was initially loaded into the 9th position is just to the left of the MSB; and all positions to the left of that contain zeros. Once these conditions are met, the deactivation of SEND and the setting of T1 occur at T1 of the 10th machine cycle after the "write to SBUF" pulse.

UART Reception in Mode 0

When REN and R1 are set to 1 and 0, respectively, reception is initiated. The bits 11111110 are written to the receive shift register at the end of the next machine cycle by the RX control unit. In the following phase, the RX control unit will activate RECEIVE.

The contents of the receive shift register are shifted one position to the left at the end of every machine cycle during which RECEIVE is active. The value that comes in from the right is the value that was sampled at the P3.0 pin.

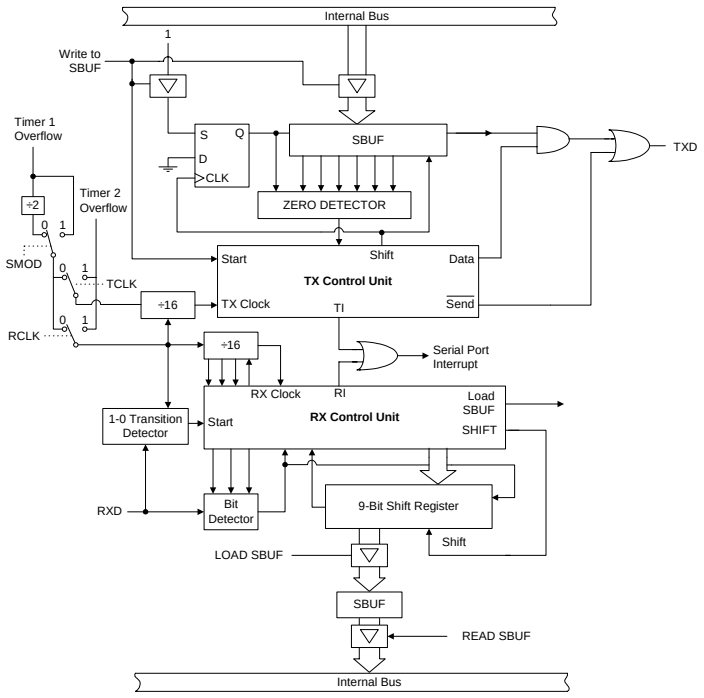
1's are shifted out to the left as data bits are shifted in from the right. The RX control block is flagged to do one last shift and load the SBUF when the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register.

UART Operation in Mode 1

In a Mode 1 operation, 10 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (Low); 8 data bits (LSB first) and a Stop bit (high). The reception is completed once the Stop bit sets the RB8 flag in the SCON register. Either Timer 1 or Timer 2 controls the baud rate in this mode.

The following diagram demonstrates the serial port structure when configured in Mode 1.

FIGURE 16: SERIAL PORT MODE 1 AND 3 BLOCK DIAGRAM



UART Transmission in Mode 1

Transmission in this mode is initiated by any instruction that makes use of SBUF as a destination register. The 9th bit position of the transmit shift register is loaded by the "write to SBUF" signal. This event also flags/informs the TX control unit that a transmission has been requested.

It is after the next rollover in the divide-by-16 counter when transmission actually begins. It follows that the bit times are synchronized to the divide-by-16 counter and not to the "write to SBUF" signal.

When a transmission begins, it places the Start bit at TXD. Data transmission is activated one bit time later. This activation enables the output bit of the transmit shift register to TXD. One bit time after that, the first shift pulse occurs.

In this mode, zeros are clocked in from the left as data bits are shifted out to the right. When the most significant bit of the data byte is at the output position of the shift register, the 1 that was initially loaded into the 9th position is to the immediate left of the MSB and all positions to the left of that contain zeros. This condition flags the TX control unit to shift one more time.

UART Reception in Mode 1

A one to zero transition at pin RXD will initiate reception. It is for this reason that RXD is sampled at a rate of 16 multiplied by the baud rate that has been established. When a transition is detected, 1FFh is written into the input shift register and the divide-by-16 counter is immediately reset. The divide-by-16 counter is reset in order to align its rollovers with the boundaries of the incoming bit times.

In total, there are 16 states in the counter. During the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The accepted value is the one seen in at least two of the three samples. The purpose of doing this is for noise rejection. If the value accepted during the first bit time is not zero, the receive circuits are reset and the unit goes back to searching for another one to zero transition. All false start bits are rejected by doing this. If the start bit is valid, it is shifted into the input shift register, and the reception of the rest of the frame will proceed.
For a receive operation, the data bits come in from the right as 1's shift out on the left. As soon as the start bit arrives at the leftmost position in the shift register, (9-bit register), it tells the UART's receive controller block to perform one last shift operation: to set RI and to load SBUF and RB8. The signal to load SBUF and RB8, and to set RI will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

- Either SM2 = 0 or the received stop bit = 1
- RI = 0

If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF and RI is activated. If one of these conditions is not met, the received frame is completely lost. At this time, whether the above conditions are met or not, the unit returns to searching for a one to zero transition in RXD.

UART Operation in Mode 2

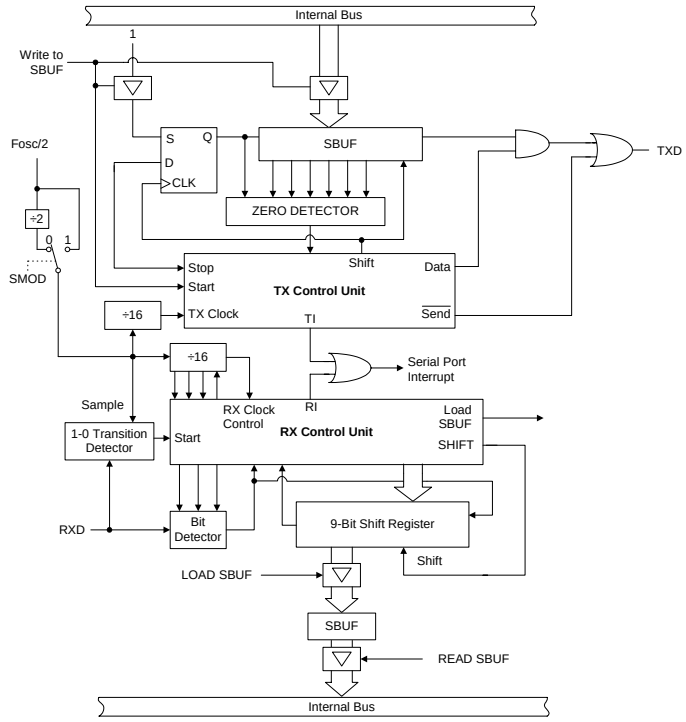
In Mode 2 a total of 11 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (low), 8 data bits (LSB first), a programmable 9th data bit and a Stop bit (high).

For transmission, the 9th data bit comes from the TB8 bit of SCON. For example, the parity bit P in the PSW could be moved into TB8.

In the case of receive, the 9th data bit is automatically written into RB8 of the SCON register.

In Mode 2, the baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

FIGURE 17: SERIAL PORT MODE 2 BLOCK DIAGRAM

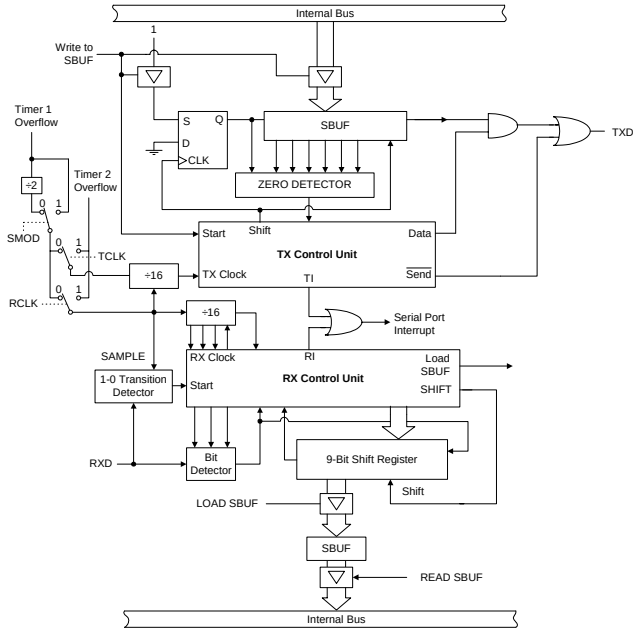


UART Operation in Mode 3

In Mode 3, 11 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (low), 8 data bits (LSB first), a programmable 9th data bit and a Stop bit (high).

Mode 3 is identical to Mode 2 in all respects but one, the baud rate. Either Timer 1 or Timer 2 generates the baud rate in Mode 3.

FIGURE 18: SERIAL PORT MODE 3 BLOCK DIAGRAM



UART in Mode 2 and 3: Additional Information

As mentioned previously, for an operation in modes 2 and 3, 11 bits are transmitted (through TXD) or received (through RXD). The signal is comprised of: a logical low Start bit, 8 data bits (LSB first), a programmable 9th data bit and a logical high Stop bit.

On transmit, (TB8 in SCON) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from either Timer 1 or Timer 2 depending on the states of TCLK and RCLK.

UART Transmission in Mode 2 and Mode 3

The transmission is initiated by any instruction that makes use of SBUF as the destination register. The 9th bit position of the transmit shift register is loaded by the "write to SBUF" signal. This event also informs the UART transmission control unit that a transmission has been requested. After the next rollover in the divide-by-16 counter, a transmission actually starts at the beginning of the machine cycle. It follows that the bit times are synchronized to the divide-by-16 counter and not to the "write to SBUF" signal, as in the previous mode.

Transmissions begin when the SEND signal is activated, which places the Start bit on the TXD pin. Data is activated one bit time later. This activation enables the output bit of the transmit shift register to the TXD pin. The first shift pulse occurs one bit time after that.

The first shift clocks a Stop bit (1) into the 9th bit position of the shift register on TXD. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition signals to the TX control unit to shift one more time and set TI, while deactivating SEND. This occurs at the 11th divide-by-16 rollover after "write to SBUF".

UART Reception in Mode 2 and Mode 3

One to zero transitions on the RXD pin initiate reception. For this reason the RXD is sampled at a rate of 16 multiplied by the established baud rate. When a transition is detected, the 1FFh is written into the input shift register and the divide-by-16 counter is immediately reset.

During the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The accepted value is the one seen in at least two of the three samples. If the value accepted during the first bit time is not zero, the receive circuits are reset and the unit goes back to searching for another one to zero transition. If the Start bit is valid, it is shifted into the input shift register, and the reception of the rest of the frame will proceed.

For a receive operation, the data bits come in from the right as 1's shift out on the left. As soon as the Start bit arrives at the leftmost position in the shift register (9-bit register), it informs the RX control block to do one more shift, to set RI and to load SBUF and RB8. The signal to set RI and to load SBUF and RB8 will be generated if, and only if, the following conditions are satisfied when the final shift pulse is generated:

- Either SM2 = 0 or the received 9th bit equal 1
- RI = 0

If both conditions are met, the 9th data bit received goes into RB8, and the first 8 data bits go into SBUF. If one of these conditions is not met, the received frame is completely lost. One bit time later, whether the above conditions are met or not, the unit goes back to searching for a one to zero transition at the RXD input.
Please note that the value of the received Stop bit is unrelated to SBUF, RB8 or RI.

UART Baud Rates

In Mode 0, the baud rate is fixed and can be represented by the following formula:

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

In Mode 2, the baud rate depends on the value of the SMOD bit in the PCON SFR. From the formula below, we can see that if SMOD = 0 (which is the value on reset), the baud rate is 1/32 the oscillator frequency.

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD} \times (\text{Oscillator Frequency})}{64}$$

The Timer 1 and/or Timer 2 overflow rate determines the baud rates in Modes 1 and 3.

Generating UART Baud Rate with Timer 1

When Timer 1 functions as a baud rate generator, the baud rate in modes 1 and 3 is determined by the Timer 1 overflow rate.

$$\text{Mode 1,3 Baud Rate} = \frac{2^{SMOD} \times \text{Timer 1 Overflow Rate}}{32}$$

Timer 1 must be configured as an 8-bit timer (TL1) in auto-reload mode with a TH1 value when an overflow occurs (Mode 2). In this application, the Timer 1 interrupt should be disabled.

The two following formulas can be used to calculate the baud rate and the reload value written into the TH1 register.

$$\text{Mode 1,3 Baud Rate} = \frac{2^{SMOD} \times Fosc}{32 \times 12(256 - TH1)}$$

The value to write into the TH1 register is defined by the following formula:

$$TH1 = 256 - \frac{2^{SMOD} \times Fosc}{32 \times 12 \times (\text{Baud Rate})}$$

Generating UART Baud Rates with Timer 2

Timer 2 is often preferred to generate the baud rate, as it can be easily configured to operate as a 16-bit timer with auto-reload. This enables far better resolution than using Timer 1 in 8-bit auto-reload mode.

The baud rate using Timer 2 is defined as:

$$\text{Mode 1,3 Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured as either a timer or a counter in any of its three running modes. In typical applications, it is configured as a timer (C/T2 is set to 0). To make Timer 2 operate as a baud rate generator, the TCLK and RCLK bits of the T2CON register must be set to 1.

The baud rate generator mode is similar to the auto-reload mode in that an overflow in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by the software. However, when Timer 2 is configured as a baud rate generator, its clock source is Osc/2.

The following formula can be used to calculate the baud rate in modes 1 and 3 using Timer 2:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

The formula below is used to define the reload value written into the RCAP2h, RCAP2L registers to achieve a given baud rate.

$$(RCAP2H, RCAP2L) = 65536 - \frac{Fosc}{32 \times [\text{Baud Rate}]}$$

In the above formula, RCAP2H and RCAP2L are the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. As such, the Timer 2 interrupt does not have to be disabled when Timer 2 is configured in baud rate generator mode.

Furthermore, when Timer 2 is configured as a UART baud rate generator and is running (TR2 is set to 1), the user should not try to perform read or write operations to the TH2/TL2, RCAP2H and RCAP2L registers.

Timer 1 Reload Value in Modes 1 & 3 for UART Baud Rate

The following table provides examples of the Timer 1, 8-bit reload value when used as a UART baud rate generator and the SMOD bit of the PCON register is set to 1:

	22.184MHz	16.000MHz	14.745MHz	12.000MHz	11.059MHz	8.000MHz	3.57MHz
115200bps	FFh	-	-	-	-	-	-
57600bps	Feh	-	-	-	FFh	-	-
38400bps	FDh	-	FEh	-	-	-	-
31250bps	-	-	-	FEh	-	-	-
19200bps	FAh	-	FCh	-	FDh	-	-
9600bps	F4h	-	F8h	-	FAh	-	-
2400bps	D0h	DDh	E0h	E6h	E8h	-	-
1200bps	A0h	BBh	C0h	CCh	D0h	DDh	-
300bps	-	-	00h	30h	40h	75h	C2h

Timer 2 Reload Value in Modes 1 & 3 for UART Baud Rate

The following are examples of [RCAP2H, RCAP2L] reload values for Timer 2 when it is used as a baud rate generator for the CRD89C512RD UART:

	22.184MHz	16.000MHz	14.745MHz	12.000MHz	11.059MHz	8.000MHz	3.57MHz
230400bps	FFFDh	-	FFFEh	-	-	-	-
115200bps	FFFAh	-	FFFCh	-	FFFDh	-	-
57600bps	FFF4h	-	FFF8h	-	FFFAh	-	-
38400bps	FFEEh	FFF3h	FFF4h	-	FFF7h	-	-
31250bps	FFEAh	FFF0h	FFF1h	FFF4h	FFF5h	FFF8h	-
19200bps	FFDCh	FFE6h	FFE8h	-	FFEEh	FFF3h	
9600bps	FFB8h	FFCCh	FFD0h	FFD9h	FFDCh	FFE6h	-
2400bps	FEE0h	FF30h	FF40h	FF64h	FF70h	FF98h	FFD1h
1200bps	FDC0h	FE5Fh	FE80h	FEC7h	FEE0h	FF30h	FFA3h
300bps	F700h	F97Dh	FA00h	FB1Eh	FB80h	FCBEh	FE8Bh

UART initialization in Mode 3 using Timer 1

```
;*** INTIALIZE THE UART @ 9600BPS, Fosc=11.0592MHz

INISER0T1I:     MOV  A,T2CON    ;RETRIEVE CURRENT VALUE OF T2CON
        ANL  A,#11001111B;RCLK & TCLK BIT = 0 -> TO USE TIMER1
        MOV  T2CON,A    ;BAUD RATE GENERATOR SOURCE FOR UART
        MOV  PCON,#80H  ;SET THE SMOD BIT TO 1
        MOV  TL1,#0FAH  ;CONFIG TIMER1 AT 8BIT WITH AUTO-RELOAD
        MOV  TH1,#0FAH  ;CALCULATE THE TIMER 1 RELOAD VALUE
                        ;TH1 = [(2^SMOD) * Fosc] / (32 * 12 * Fcomm)
                        ;TH1 FOR 9600BPS @ 11.059MHz = FAh
        MOV  SCON,#05Ah;CONFIG SCON_0 MODE_1
        MOV  TMOD,#00100000B ;CONFIG TIMER 1 IN MODE 2, 8BIT
                        ; + AUTO RELOAD
        MOV  TCON,#01000000B  ;START TIMER1

        CLR  SCON.0     ;CLEAR UART RX, TX FLAGS
        CLR  SCON.1
        MOV  SBUF,#DATA         ;SEND ONE BYTE ON THE SERIAL PORT
```

UART initialization in Mode 3, using Timer 2

```
;*** INTIALIZE THE UART @57600BPS, Fosc=11.0592MHz

INISER0T2I:     MOV  SCON,#05Ah;CONFIG SCON_0 MODE_1,
                        ;CALCULATE RELOAD VALUE WITH T2
                        ;RCAP2H,RCAP2L = 65536 - [ Fosc / (32*Fcomm)]

        MOV  RCAP2H,#0FFh       ;RELOAD VALUE 57600bps, 11.059MHz =FFFAh
        MOV  RCAP2L,#0DCh       ;

        MOV  T2CON,#034h        ;SERIAL PORT0, TIMER2 RELOAD START

        CLR  SCON.0     ;CLEAR UART RX, TX FLAGS
        CLR  SCON.1

        MOV  SBUF,#DATA         ;SEND ONE BYTE ON THE SERIAL PORT
```

Interrupts

The CRD89C512RD has 8 interrupt sources (9 if the WDT is included) and 7 interrupt vectors (including reset) used for handling.

The interrupts are enabled via the IE register shown below:

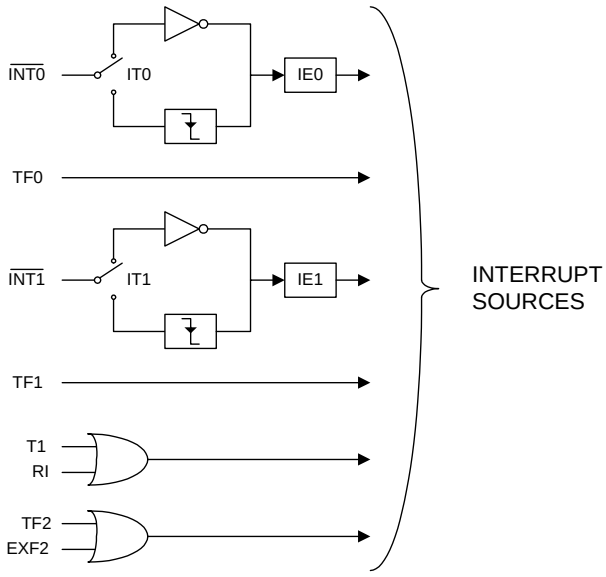
TABLE 31: IE INTERRUPT ENABLE REGISTER –SFR A8H

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit	Mnemonic	Description
7	EA	Disables All Interrupts 0: no interrupt acknowledgment 1: Each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
6	-	Reserved
5	ET2	Timer 2 Interrupt Enable Bit
4	ES	Serial Port Interrupt Enable Bit
3	ET1	Timer 1 Interrupt Enable Bit
2	EX1	External Interrupt 1 Enable Bit
1	ET0	Timer 0 Interrupt Enable Bit
0	EX0	External Interrupt 0 Enable Bit

The following figure illustrates the various interrupt sources on the CRD89C512RD.

FIGURE 19: INTERRUPT SOURCES



Interrupt Vectors

The following table specifies each interrupt source, its flag and its vector address.

TABLE 32: INTERRUPT VECTOR ADDRESS

Interrupt Source	Flag	Vector Address
RESET (+ WDT)	WDR	0000h*
INT0	IE0	0003h
Timer 0	TF0	000Bh
INT1	IE1	0013h
Timer 1	TF1	001Bh
Serial Port	RI+TI	0023h
Timer 2	TF2+EXF2	002Bh

*If location 0000h = FFh, the PC jump to the ISP program.

External Interrupts

The CRD89C512RD has two external interrupt inputs (INT0 and INT1). These interrupt lines are shared with the P3.2 and P3.3 I/Os.

Bits IT0 and IT1 of the TCON register determine whether the external interrupts are level or edge sensitive.

If ITx = 1, the interrupt will be raised when a 1-> 0 transition occurs at the interrupt pin. The duration of the transition must be at least equal to 12 oscillator cycles.

If ITx = 0, the interrupt will occur when a logic low condition is present on the interrupt pin.

The state of the external interrupt, when enabled, can be monitored using the flags, IE0 and IE1 of the TCON register and will be set when the interrupt condition occurs.

In the case where the interrupt was configured as edge sensitive, the associated flag is automatically cleared when the interrupt is serviced.

If the interrupt is configured as level sensitive, the interrupt flag must be cleared by the software.

Timer 0 and Timer 1 Interrupt

Both Timer 0 and Timer 1 can be configured to generate an interrupt when a rollover of the timer/counter occurs (except Timer 0 in Mode 3).

The TF0 and TF1 flags serve to monitor timer overflow occurring in Timer 0 and Timer 1. These interrupt flags are automatically cleared when the interrupt is serviced.

Timer 2 interrupt

A Timer 2 interrupt can occur if TF2 and/or EXF2 flags are set to 1 and if the Timer 2 interrupt is enabled.

The TF2 flag is set when a rollover of the Timer 2 Counter/Timer occurs. The EXF2 flag can be set by a 1 to 0 transition on the T2EX pin by the software.

Note that neither flag is cleared by the hardware upon execution of the interrupt service routine. The service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt. These flag bits will have to be cleared by the software.

Every bit that generates interrupts can either be cleared or set by the software, yielding the same result as when the operation is done by the hardware. In other words, pending interrupts can be cancelled and interrupts can be generated by the software.

Serial Port Interrupt

The serial port can generate an interrupt upon byte reception or once the byte transmission is completed.

These two conditions share the same interrupt vector and it is up to the user-developed interrupt service routine software to determine the cause of the interrupt by examining serial interrupt flags RI and TI.

Note that neither of these flags is cleared by the hardware upon execution of the interrupt service routine. The software must clear these flags.

Execution of an Interrupt

When the processor receives an interrupt request, an automatic jump to the desired subroutine occurs. This jump is similar to executing a branch to a subroutine instruction: the processor automatically saves the address of the next instruction on the stack. An internal flag is set to indicate that an interrupt is taking place, and then the jump instruction is executed. An interrupt subroutine must always end with the RETI instruction. This instruction allows users to retrieve the return address placed on the stack.

The RETI instruction also allows updating of the internal flag that will take into account an interrupt with the same priority.

Interrupt Enable and Interrupt Priority

When the CRD89C512RD is initialized, all interrupt sources are inhibited by the bits of the IE register being reset to 0. It is necessary to start by enabling the interrupt sources that the application requires.This is achieved by setting bits in the IE register, as discussed previously.

This register is part of the bit addressable internal SRAM. For this reason, it is possible to modify each bit individually in one instruction without having to modify the other bits of the register. All interrupts can be inhibited by setting EA to 0.

The order in which interrupts are serviced is shown in the following table:

TABLE 33: INTERRUPT PRIORITY

Interrupt Source
RESET + WDT (Highest Priority)
IE0
TF0
IE1
TF1
RI+TI
TF2+EXF2 (Lowest Priority)

Modifying the Order of Priority

The CRD89C512RD allows the user to modify the natural priority of the interrupts. The order can be modified by programming the bits in the IP (Interrupt Priority) register. When any bit in this register is set to 1, it gives the corresponding source priority over interrupts coming from sources that don't have their corresponding IP bits set to 1.

The IP register is represented in the table below.

TABLE 34: IP INTERRUPT PRIORITY REGISTER –SFR B8H

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit	Mnemonic	Description
7	-	
6	-	
5	PT2	Gives Timer 2 Interrupt Higher Priority
4	PS	Gives Serial Port Interrupt Higher Priority
3	PT1	Gives Timer 1 Interrupt Higher Priority
2	PX1	Gives INT1 Interrupt Higher Priority
1	PT0	Gives Timer 0 Interrupt Higher Priority
0	PX0	Gives INT0 Interrupt Higher Priority

Watchdog Timer

The CRD89C512RD watchdog timer (WDT) is a 16-bit free-running counter operating from an independent 250KHz internal RC oscillator. The overflow of the watchdog timer counter will reset the processor. The WDT is a useful safety measure for systems that are susceptible to noise, power glitches and other conditions that can cause the software to go into infinite dead loops or runaways; The WDT provides a recovery mechanism from abnormal software conditions.

Watchdog Timer Registers

The configuration and use of the CRD89C512RD watchdog timer is handled by three registers: WDTKEY, WDTCTRL and SYSCON.

The WDTKEY register ensures that the watchdog timer is not inadvertently reset in case of program malfunction.

TABLE 35: WATCH DOG TIMER KEY REGISTER: WDTKEY – SFR 97H

7	6	5	4	3	2	1	0
WDTKEY7:0							

Bit	Mnemonic	Description
7:0	WDTKEY	Watch Dog Key

The WDTCTRL register is, by default, configured as a read-only register. To modify its contents, two consecutive write operations to the WDTKEY register must be performed:

```
MOV    WDTKEY,#01Eh
MOV    WDTKEY,#0E1h
```

Once the configuration or WDT reset operation is complete, the WDTCTRL register can be restored to read-only by writing the following sequence into the WDTKEY register:

```
MOV    WDTKEY,#0E1h
MOV    WDTKEY,#01Eh
```

Once the WDT operation is activated, the user software must clear it periodically. If the WDT is not cleared, its overflow will trigger a reset of the CRD89C512RD.

TABLE 36: WATCH DOG TIMER CONTROL (WDTCTRL) – SFR 9FH

7	6	5	4	3	2	1	0
WDTE	Unused	WDT CLR	Unused		WDT PS2	WDT PS1	WDT PS0

Bit	Mnemonic	Description
7	WDTE	Watchdog Timer Enable Bit 0: Watchdog Timer is disabled 1: Watchdog Timer is enabled
6	Unused	-
5	WDTCLR	Watchdog Timer Counter Clear Bit
[4:3]	Unused	-
2	WDTPS2	Clock Source Divider Bit 2
1	WDTPS1	Clock Source Divider Bit 1
0	WDTPS0	Clock Source Divider Bit 0

The WDT timeout delay can be adjusted by configuring the clock divider input on the WDT's time base source clock. To select the divider value, the [WDTPS2~WDTPS0] bits of the WDT control register should be set accordingly.

The following table provides the approximate timeout periods associated with different values of the WDTPSx bits of the watchdog timer register.

TABLE 37: WDT TIMEOUT PERIOD AT

WDTPS [2:0]	WDT Period
000	2.05ms
001	4.10ms
010	8.19ms
011	16.38ms
100	32.77ms
101	65.54ms
110	131.07ms
111	262.14ms

To enable the WDT, the user must set bit 7 (WDTE) of the WDTCTRL register to 1. The 16-bit counter will start to count using the internal 250kHz oscillator as a clock source, divided according to the value of the WDTPS2~WDTPS0 bits.

To clear the WDT, set the WDTCLR bit of the WDTCTRL to 1. This action will clear the contents of the 16-bit counter and force it to restart.

If the watchdog timer overflows, it will reset the processor, the WDR bit (7) of SYSCON register will be set to 1 and the WDTE bit will be cleared to 0. The user should check the WDR bit if an unexpected reset has taken place. If the WDR bit is set, the processor reset was caused by the watchdog timer.

WDT Initialization Example

The following program example demonstrates the watchdog timer initialization sequence and the routine to periodically clear it.

```
;*** VARIABLE DEFINITION ***

CPTR      EQU       020H
PORTVAL             EQU       00H

;*** PROGRAM START HERE ****
ORG   0000h
          LJMP    START

;*** MAIN PROGRAM START ***
ORG   0100h

;*** CHECK IF RESET WAS CAUSED BY THE WATCHDOG
TIMER
START:   MOV    A,SYSCON
          ANL    A,#80H
          JNZ    WDTRESET   ;WDT BIT SET -> WE GOT A WDT
RESET

INITWDT:              MOV    WDTKEY,#01EH        ;UNLOCK
THE WDTCTRL REG ACCESS IN
          MOV    WDTKEY,#0E1H        ;WRITING MODE

          MOV   WDTCTRL,#10000010B  ;CONFIG THE
WATCHDOG TIMER
                              ;BIT 7  - WDTEN=1 WATCHDOG
TIMER ENABLE
                              ;BIT 6   - UNUSED
                              ;BIT 5   - WDTCLR=1
WATCHDOG CLEAR
                              ;BIT 4:3 - UNUSED
                              ;BIT 2:0 - WDTCLK=010 - WDT
TIMEOUT = 8mS

          MOV    WDTKEY,#0E1H        ;LOCK THE WDTCTRL
          ACCESS IN WRITING MOV    WDTKEY,#01EH
          MOV    PORTVAL,#00H        ;INIT PORT VALUE TO
00H


WDTRESET:          NOP                 ;IF THE WDT CAUSE
THE RESET INIT PORTVAL
          MOV    A,PORTVAL;TOGGLE P1 VALUE
          CPL    A
          MOV    PORTVAL,A
          MOV    P1,A

;*** SEQUENCE TO CLEAR THE WATCHDOG TIMER (SAME
AS CONFIG)
LOOP:     ;MOV    WDTKEY,#01EH        ;UNLOCK THE
WDTCTRL REG ACCESS IN
                              ;WRITING MODE
          ;MOV    WDTKEY,#0E1H

          ;MOV    WDTCTRL,#10100010B            ;CONFIG THE
          WDT TIMER                           ;BIT 7 -
WDTEN=1 WDT ENABLE
                              ;BIT 6   - UNUSED
                              ;BIT 5   - WDTCLR=1 WDT
CLEAR
                              ;BIT 4:3 - UNUSED
                              ;BIT 2:0 - WDTCLK=010 - WDT
TIMEOUT = 8mS

          ;MOV    WDTKEY,#0E1H        ;LOCK THE WDTCTRL
ACCESS IN WRITING
          ;MOV    WDTKEY,#01EH

          (…)

          LJMP    LOOP
```

Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) module consists of four outputs. Each output uses an 8-bit PWM data register (PWMD) to set the number of continuous pulses within a PWM frame cycle.

PWM Function Description:

Each 8-bit PWM output incorporates an 8-bit register that consists of a 5-bit PWM (5 MSBs) and a 3-bit (LSBs) narrow pulse generator (NP). The 5-bit PWM determines the duty cycle of the output. The 3-bit NPx generates and inserts narrow pulses among the PWM frame made of 8 cycles.

The number of pulses generated is equal to the number programmed into the 3-bit NP. The NP is used to generate an equivalent 8-bit resolution PWM-type DAC with a reasonably high repetition rate through a 5-bit PWM clock speed. The PDCK[1:0] settings of the PWMC (A3h) register are used to derive the PWM clock from Fosc.

$$\text{PWM Clock} = \frac{F_{osc}}{2^{(\text{PDCK [1:0]} +1)}}$$

The PWM output cycle frame repetition rate (frequency) is calculated using the following formula:

$$\text{PWM Clock} = \frac{F_{osc}}{32 \times 2^{(\text{PDCK [1:0]} +1)}}$$

PWM Output Enable Register

TABLE 38: PWM OUTPUT ENABLE REGISTER (PWME) – SFR 9BH

7	6	5	4
--		PWM3E	PWM2E

3	2	1	0
PWM1E	PWM0E	-	

Bit	Mnemonic	Description
7:6	-	When bit is set to one, the corresponding PWM pin is active as a PWM function. When the bit is cleared, the corresponding PWM pin is active as an I/O pin. These five bits are cleared upon reset.
5	PWM3E	
4	PWM2E	
3	PWM1E	
2	PWM0E	
1:0	-	

PWM Registers -PWM Control Register

The table below describes the PWM control register.

TABLE 39: PWM CONTROL REGISTER (PWMC) – SFR A3H

7	6	5	4	3	2	1	0
Unused						PDCK1	PDCK0

Bit	Mnemonic	Description
[7:2]	Unused	-
1	PDCK1	Input Clock Frequency Divider Bit 1
0	PDCK0	Input Clock Frequency Divider Bit 0

The following table describes the relationship between the values of PDCK1/PDCK0 and the value of the divider. Numerical values of the corresponding frequencies are also provided.

PDCK1	PDCKO	Divider	PWM clock, Fosc=20MHz	PWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

PWM Data Registers

The following tables describe the PWM data registers. The PWMDx bits hold the content of the PWM data register and determine the duty cycle of the PWM output waveforms. The NPx[2:0] bits will insert narrow pulses into the 8-PWM-cycle frame.

TABLE 40: PWM DATA REGISTER 0 (PWMD0) – SFR A4H

7	6	5	4
PWMD0.4	PWMD0.3	PWMD0.2	PWMD0.1

3	2	1	0
PWMD0.0	NP0.2	NP0.1	NP0.0

Bit	Mnemonic	Description
7	PWMD0.4	Contents of PWM Data Register 0 Bit 4
6	PWMD0.3	Contents of PWM Data Register 0 Bit 3
5	PWMD0.2	Contents of PWM Data Register 0 Bit 2
4	PWMD0.1	Contents of PWM Data Register 0 Bit 1
3	PWMD0.0	Contents of PWM Data Register 0 Bit 0
2	NP0.2	Inserts Narrow Pulses in a 8-PWM-Cycle Frame
1	NP0.1	
0	NP0.0	

TABLE 41: PWM DATA REGISTER 1 (PWMD1) – SFR A5H

7	6	5	4
PWMD1.4	PWMD1.3	PWMD1.2	PWMD1.1

3	2	1	0
PWMD1.0	NP1.2	NP1.1	NP1.0

Bit	Mnemonic	Description
7	PWMD1.4	Contents of PWM Data Register 1 Bit 4
6	PWMD1.3	Contents of PWM Data Register 1 Bit 3
5	PWMD1.2	Contents of PWM Data Register 1 Bit 2
4	PWMD1.1	Contents of PWM Data Register 1 Bit 1
3	PWMD1.0	Contents of PWM Data Register 1 Bit 0
2	NP1.2	Inserts Narrow Pulses in a 8-PWM-Cycle Frame
1	NP1.1	
0	NP1.0	

TABLE 42: PWM DATA REGISTER 2 (PWMD2) – SFR A6H

7	6	5	4
PWMD2.4	PWMD2.3	PWMD2.2	PWMD2.1

3	2	1	0
PWMD2.0	NP2.2	NP2.1	NP2.0

Bit	Mnemonic	Description
7	PWMD2.4	Contents of PWM Data Register 2 Bit 4
6	PWMD2.3	Contents of PWM Data Register 2 Bit 3
5	PWMD2.2	Contents of PWM Data Register 2 Bit 2
4	PWMD2.1	Contents of PWM Data Register 2 Bit 1
3	PWMD2.0	Contents of PWM Data Register 2 Bit 0
2	NP2.2	Inserts Narrow Pulses in a 8-PWM-Cycle Frame
1	NP2.1	
0	NP2.0	

TABLE 43: PWM DATA REGISTER 3 (PWMD3) – SFR A7H

7	6	5	4
PWMD3.4	PWMD3.3	PWMD3.2	PWMD3.1

3	2	1	0
PWMD3.0	NP3.2	NP3.1	NP3.0

Bit	Mnemonic	Description
7	PWMD3.4	Contents of PWM Data Register 3 Bit 4
6	PWMD3.3	Contents of PWM Data Register 3 Bit 3
5	PWMD3.2	Contents of PWM Data Register 3 Bit 2
4	PWMD3.1	Contents of PWM Data Register 3 Bit 1
3	PWMD3.0	Contents of PWM Data Register 3 Bit 0
2	NP3.2	Inserts Narrow Pulses in a 8-PWM-Cycle Frame
1	NP3.1	

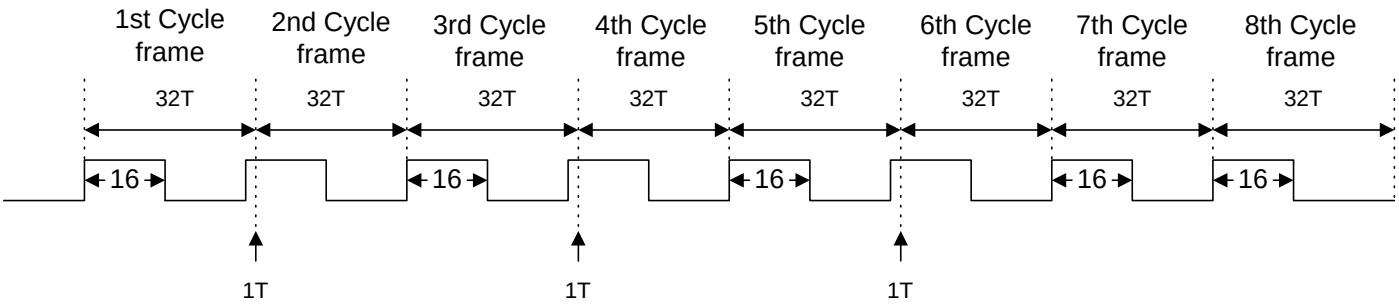
The table below shows the number of PWM cycles inserted into an 8-cycle frame when we vary the NP number.

NP[2:0]	Number of PWM cycles inserted in an 8-cycle frame
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Example of PWM Timing Diagram

```
MOV PWMD0 #83H          ; PWMD04:0]=10h (=16T high, 16T low), NP02:0] = 3
MOV PWME, #08H          ; Enable P1.3 as PWM output pin
```

FIGURE 20: PWM TIMING DIAGRAM



(Narrow pulse inserted by NP0[2:0]=3)

PWM clock= 1/T= Fosc / 2^(PDIV+1)
The SPWM output cycle frame frequency = SPWM clock/32 = [Fosc/2^(PDIV+1)]/32

If Fosc = 20MHz, PDCK[1:0] of PWMC = #03H, then PWM clock = 20MHz/2^4 = 20MHz/16 = 1.25MHz. PWM output cycle frame frequency = (20MHz/2^4)/32 = 39.1 kHz.

Crystal Consideration

The crystal connected to the CRD89C512RD oscillator input should be of a parallel type, operating in fundamental mode.

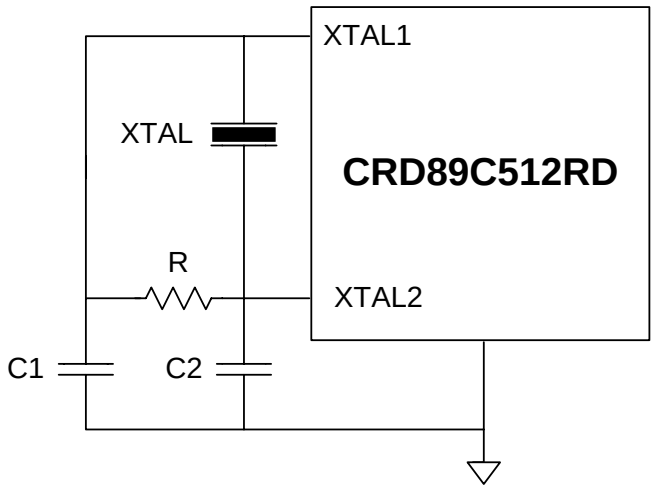
The following table provides suggested capacitor and resistor feedback values for different operating frequencies.

Valid for CRD89C512RD				
XTAL	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
XTAL	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

Note: Oscillator circuits may differ with different crystals or ceramic resonators in higher oscillator frequencies.

Crystals or ceramic resonator characteristics vary from one manufacturer to the other.

The user should review the technical literature supplied with specific crystal or ceramic resonators or contact the manufacturer to select the appropriate values for external components.



Operating Conditions

TABLE 44: OPERATING CONDITIONS

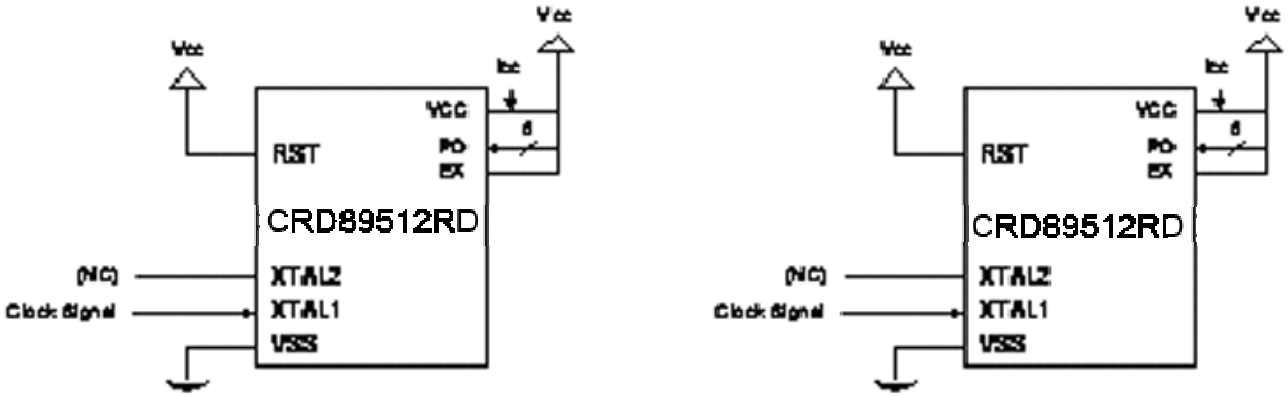
Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
TA	Operating temperature	-40	25	+85	ºC	Ambient temperature under bias
TS	Storage temperature	-55	25	155	ºC	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 40	Oscillator Frequency	3.0	-	40	MHz	For 5V application

DC Characteristics

TABLE 45: DC CHARACTERISTICS

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	Port 0,1,2,3,4,#EA	-0.5	1.0	V	VCC=5V
VIL2	Input Low Voltage	RES, XTAL1	0	08	V	VCC=5V
VIH1	Input High Voltage	Port 0,1,2,3,4,#EA	2.0	VCC+0.5	V	VCC=5V
VI H2	Input High Voltage	RES, XTAL1	70% VCC	VCC+0.5	V	VCC=5V
VOL1	Output Low Voltage	Port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	Port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	Port 0	2.4		V	IOH=-800uA
			90%VCC		V	IOH=-80uA
VOH2	Output High Voltage	Port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90% VCC		V	IOH=-10uA
IIL	Logical 0 Input Current	Port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	Port 1,2,3,4		-650	uA	Vin=2.OV
ILI	Input Leakage Current	Port 0, #EA		±10	uA	0.45V<Vin<VCC
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C-10	Pin Capacitance			10	pF	Fre=1 MHz, Ta=25°C
ICC	Power Supply Current	VDD			mA	Active mode, 40MHz
					mA	Active mode 25MHz
				20	mA	Active mode 16MHz
					mA	Idle mode, 40MHz
					mA	Idle mode 25MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

FIGURE 21: ICC ACTIVE MODE TEST CIRCUIT



AC Characteristics

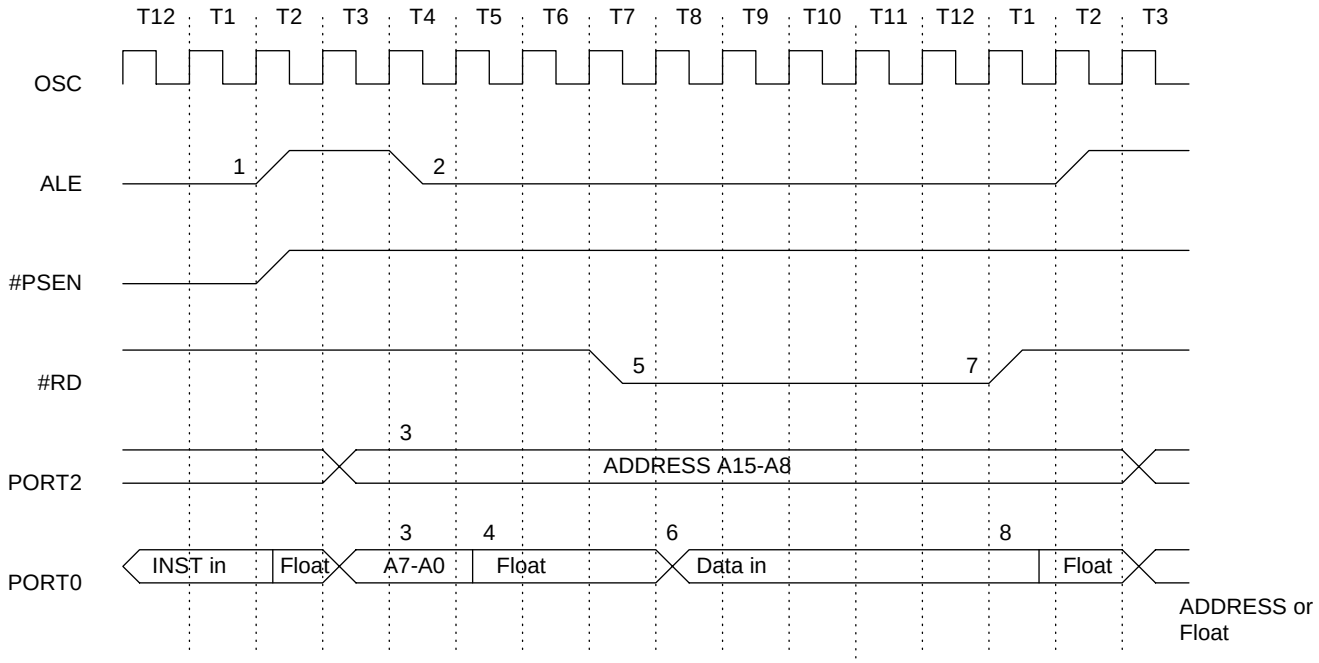
TABLE 46: AC CHARACTERISTICS

Symbol	Parameter	Valid Cycle	Fosc 16			Variable Fosc			Unit
			Min.	Type	Max.	Min.	Type	Max.	
T LHLL	ALE Pulse Width	RD/WRT	115			2xT - 10			nS
T AVLL	Address Valid to ALE Low	RD/WRT	43			T - 20			nS
T LLAX	Address Hold after ALE Low	RD/WRT	53			T - 10			nS
T LLIV	ALE Low to Valid Instruction In	RD			240			4xT - 10	nS
T LLPL	ALE Low to #PSEN low	RD	53			T - 10			nS
T PLPH	#PSEN Pulse Width	RD	173			3xT - 15			nS
T PLIV	#PSEN Low to Valid Instruction In	RD			177			3xT -10	nS
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS
T AVI V	Address to Valid Instruction In	RD			292			5xT - 20	nS
T PLAZ	#PSEN Low to Address Float	RD			10			10	nS
T RLRH	#RD Pulse Width	RD	365			6xT - 10			nS
T WLWH	#WR Pulse Width	WRT	365			6xT - 10			nS
T RLDV	#RD Low to Valid Data In	RD			302			5xT - 10	nS
T RHDX	Data Hold after #RD	RD	0			0			nS
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS
T LLDV	ALE Low to Valid Data In	RD			590			8xT - 10	nS
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS
T LLYL	ALE low to #WR High or #RD Low	RD/WRT	178		197	3xT - 10		3xT + 10	nS
T AVYL	Address Valid to #WR or #RD Low	RD/WRT	230			4xT - 20			nS
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS
T QVWX	Data Valid to #WR Transition	WRT	38			T - 25			nS
T WHQX	Data Hold after #WR	WRT	73			T + 10			nS
T RLAZ	#RD Low to Address Float	RD						5	nS
T YALH	#W R or #RD High to ALE High	RD/WRT	53		72	T -10		T+10	nS
T CHCL	Clock Fall Time								nS
T CLCX	Clock Low Time								nS
T CLCH	Clock Rise Time								nS
T CHCX	Clock High Time								nS
T, TCLCL	Clock Period		63				1/fosc		nS

Data Memory Read Cycle Timing

The following timing diagram provides Data Memory Read Cycle timing information.

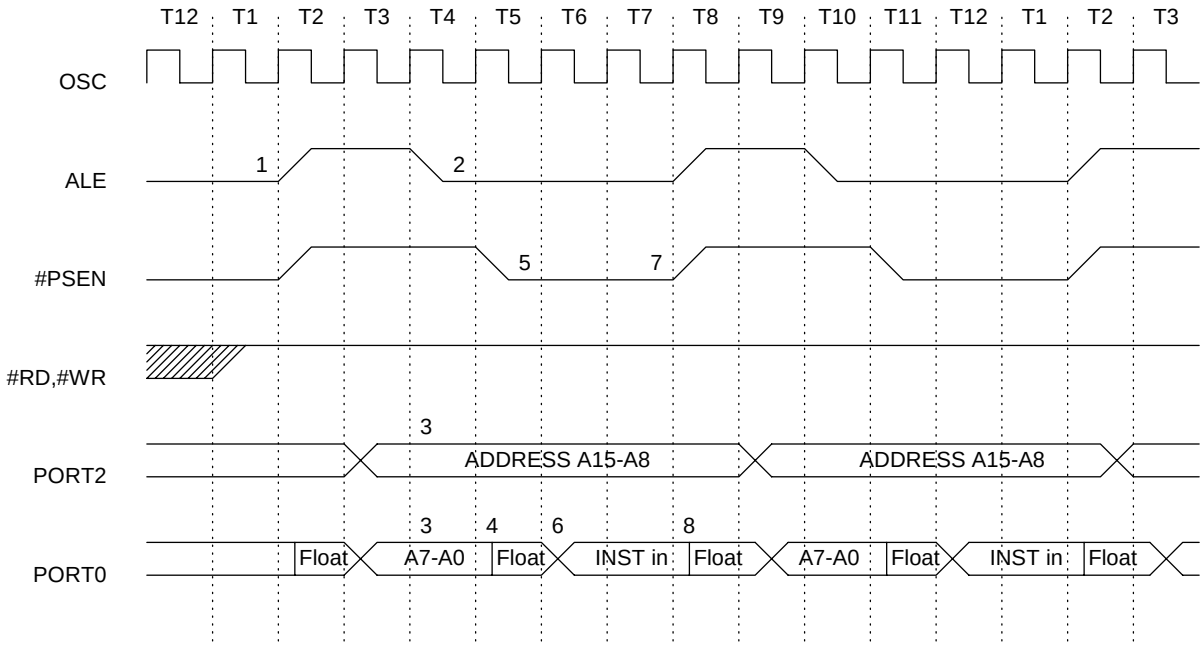
FIGURE 22: DATA MEMORY READ CYCLE TIMING



Program Memory Read Cycle Timing

The following timing diagram provides Program Memory Read Cycle timing information.

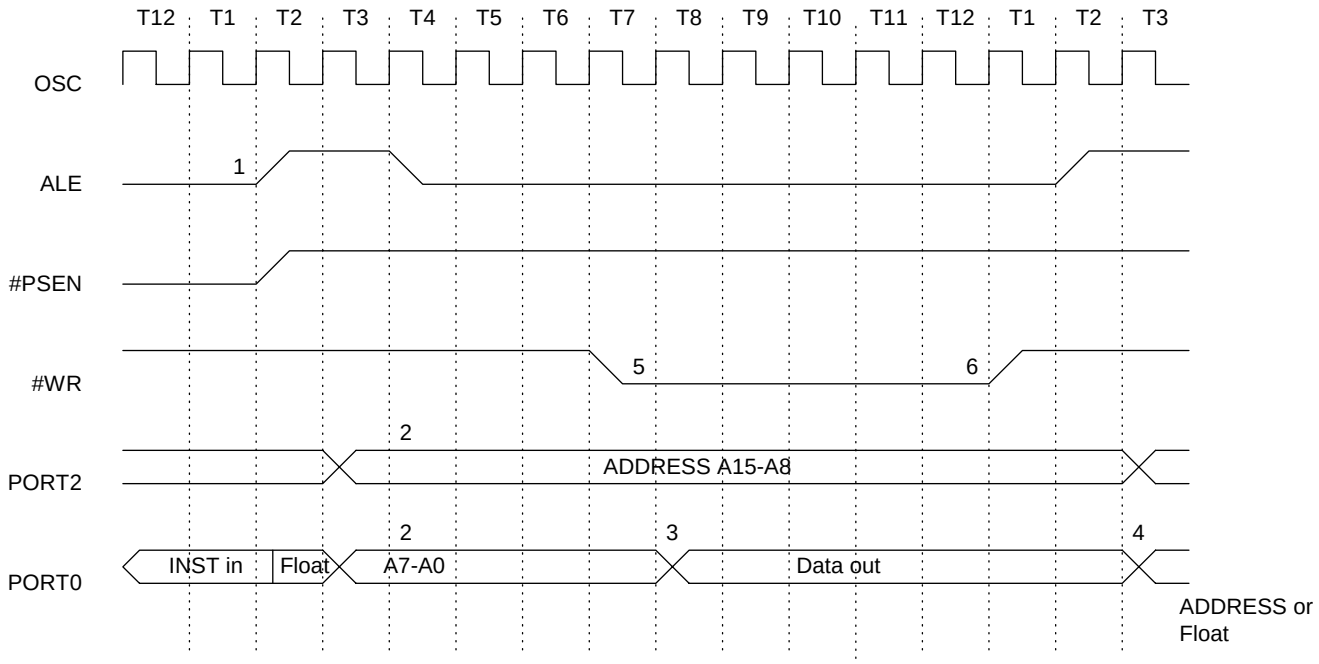
FIGURE 23: PROGRAM MEMORY READ CYCLE



Data Memory Write Cycle Timing

The following timing diagram provides Data Memory Write Cycle timing information.

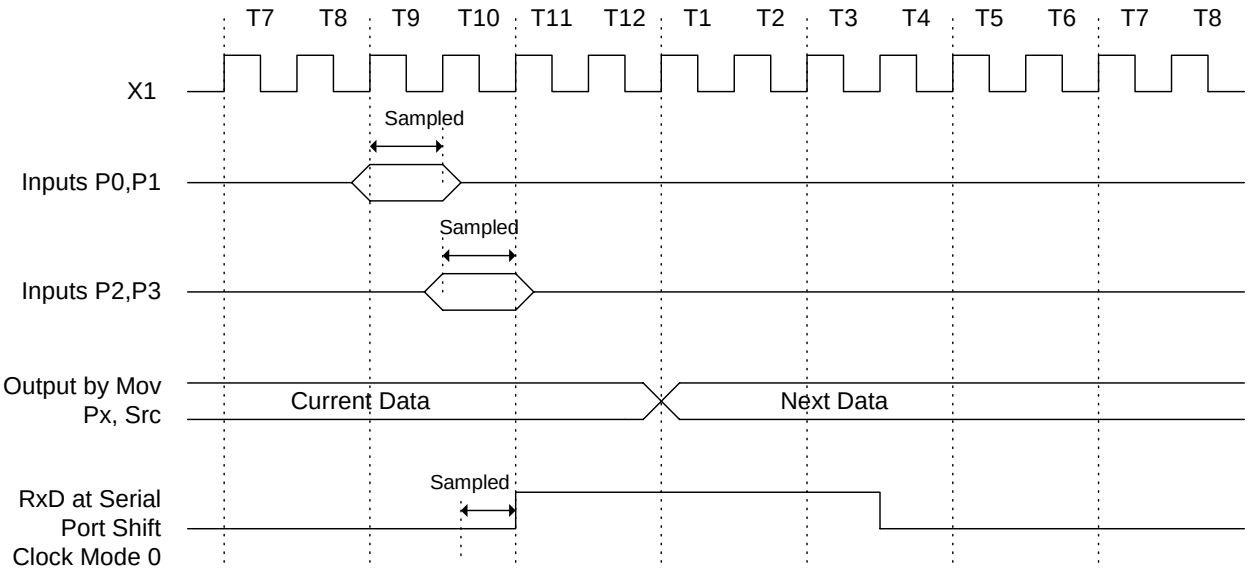
FIGURE 24: DATA MEMORY WRITE CYCLE TIMING



I/O Ports Timing

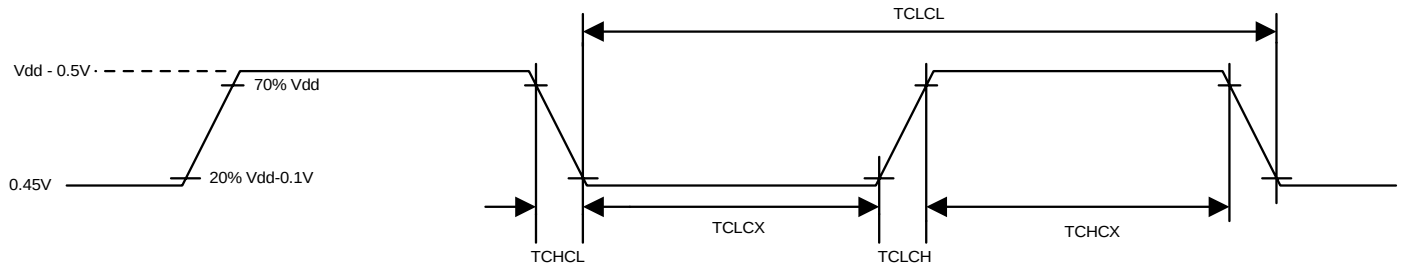
The following timing diagram provides Port Timing information.

FIGURE 25: I/O PORTS TIMING



Timing Requirement of the External Clock (VSS = 0v is assumed)

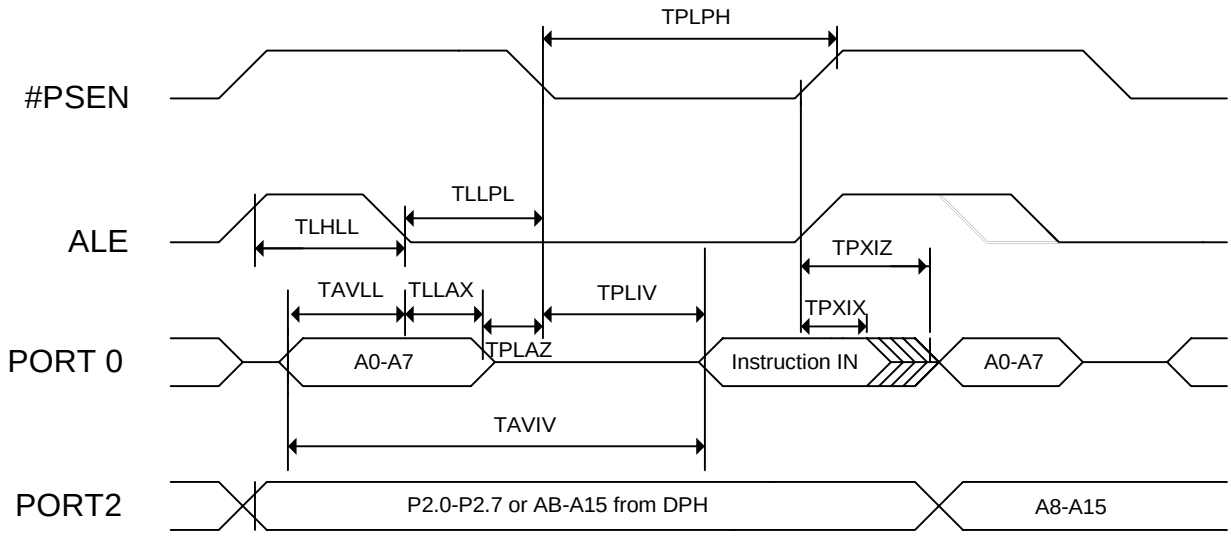
FIGURE 26: TIMING REQUIREMENT OF EXTERNAL CLOCK (VSS= 0.0V IS ASSUMED)



External Program Memory Read Cycle

The following timing diagram provides External Program Memory Read Cycle timing information.

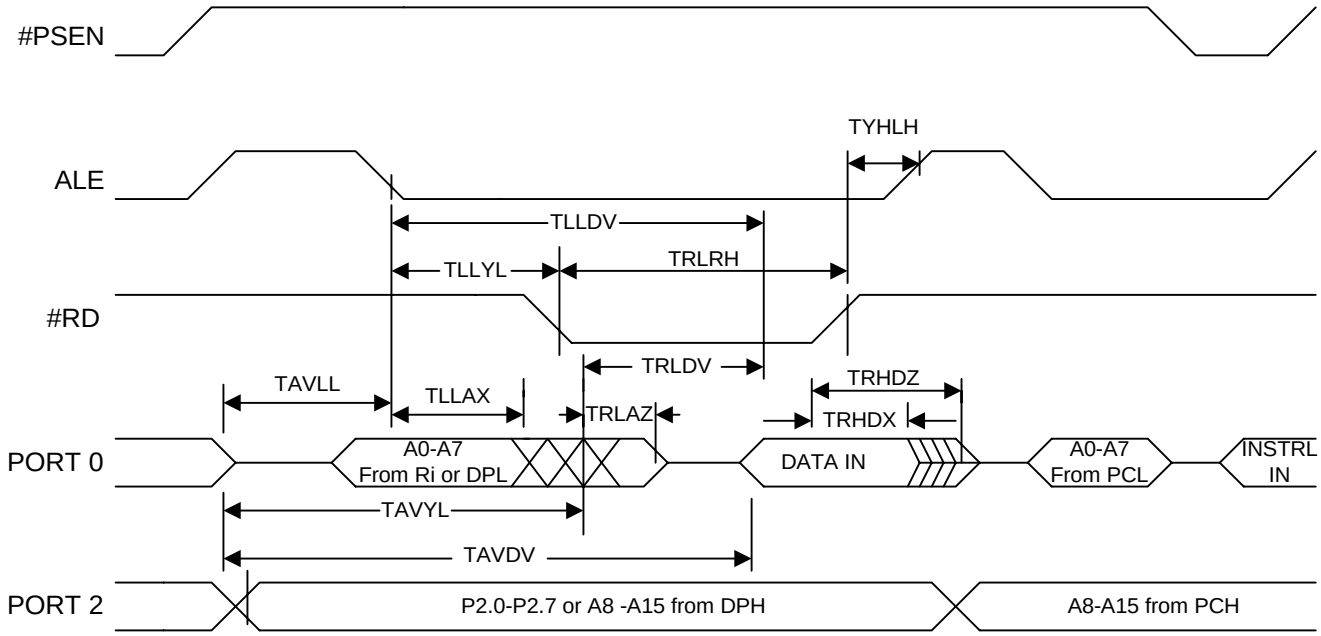
FIGURE 27: EXTERNAL PROGRAM MEMORY READ CYCLE



External Data Memory Read Cycle

The following timing diagram provides External Data Memory Read Cycle timing information.

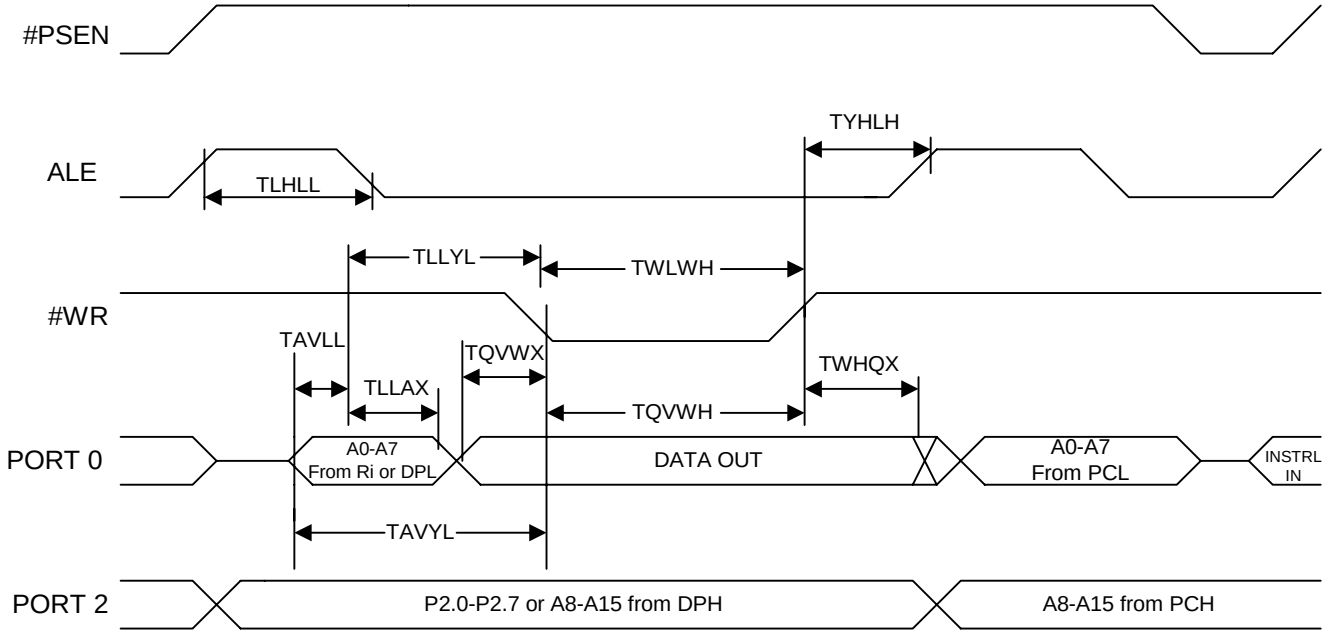
FIGURE 28: EXTERNAL DATA MEMORY READ CYCLE



External Data Memory Write Cycle

The following timing diagram provides External Data Memory Write Cycle timing information.

FIGURE 29: EXTERNAL DATA MEMORY WRITE CYCLE



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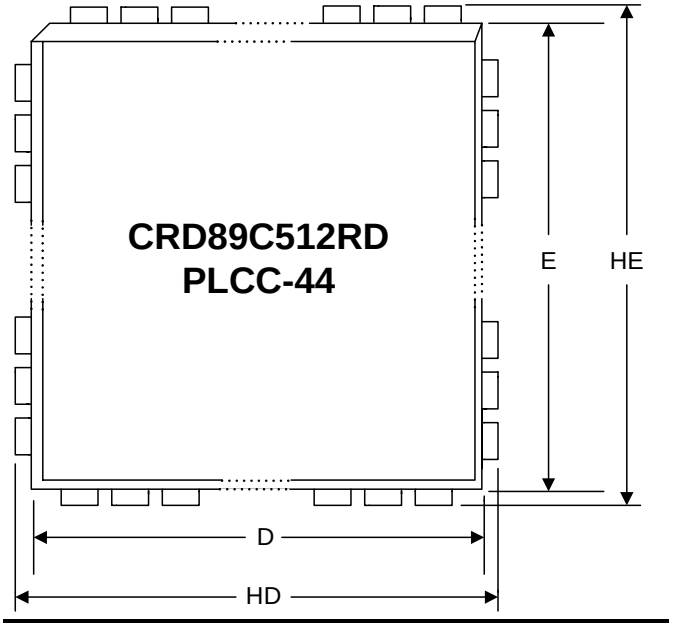
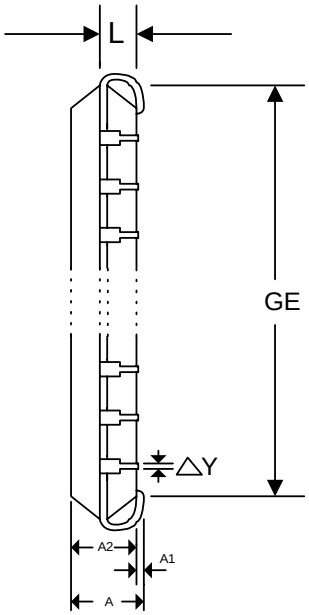
Plastic Chip Carrier (PLCC-44)





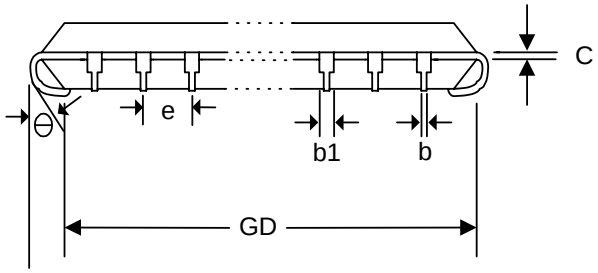
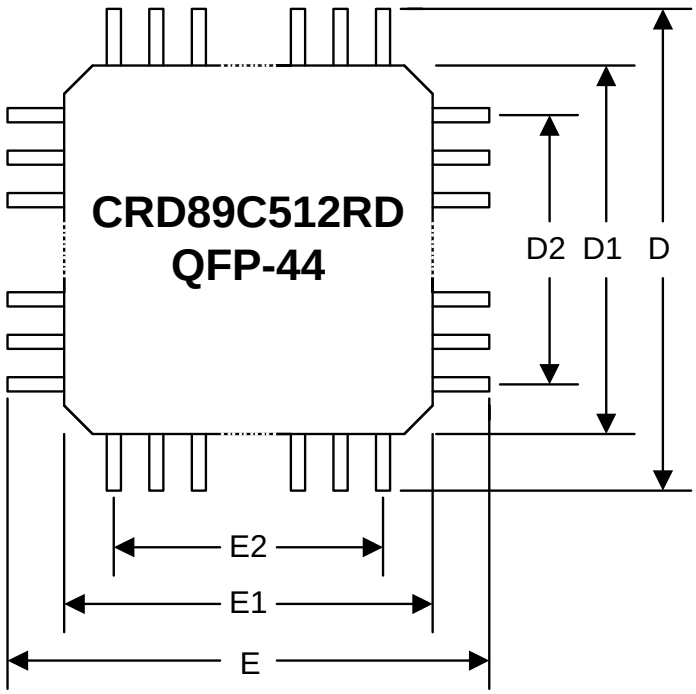


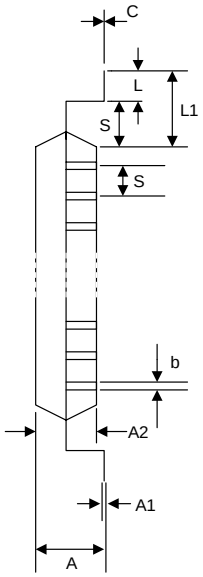
TABLE 47: DIMENSIONS OF PLCC-44 CHIP CARRIER

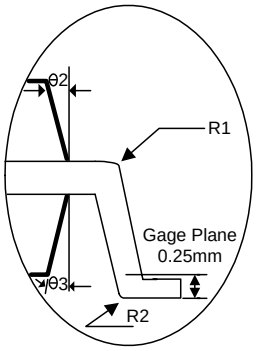
Symbol	Dimension in inch	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.185	-/4.70
Al	0.020/-	0.51/
A2	0.145/0.155	3.68/3.94
bl	0.026/0.032	0.66/0.81
b	0.016/0.022	0.41/0.56
C	0.008/0.014	0.20/0.36
D	0.648/0.658	16.46/16.71
E	0.648/0.658	16.46/16.71
e	0.050 BSC	1.27 BSC
GD	0.590/0.630	14.99/16.00
GE	0.590/0.630	14.99/16.00
HD	0.680/0.700	17.27/17.78
HE	0.680/0.700	17.27/17.78
L	0.090/0.110	2.29/2.79
θ	-/0.004	-/0.10
Δy	/	/

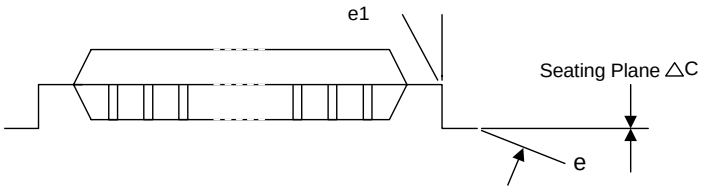
Note:
1. Dimensions D & E do not include interlead Flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inch
4. General appearance spec should be based on final visual inspection spec.

Plastic Quad Flat Package (QFP-44)









Note:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Allowance protrusion is 0.25mm per side.
3. Dimensions D1 and E1 do not include mold mismatch and are determined datum plane.
4. Dimension b does not include dambar protrusion.
5. Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the lead foot.

TABLE 48: DIMENSIONS OF QFP-44 CHIP CARRIER

Symbol	Dimension in in.	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.100	-/2.55
Al	0.006/0.014	0.15/0.35
A2	0.071 / 0.087	1.80/2.20
b	0.012/0.018	0.30/0.45
c	0.004 / 0.009	0.09/0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73/1.03
L1	0.063	1.60
R1	0.005/-	0.13/-
R2	0.005/0.012	0.13/0.30
S	0.008/-	0.20/-
0	0°/7°	as left
θ 1	0°/ -	as left
θ 2	10° REF	as left
θ 3	7° REF	as left
ΔC	0.004	0.10

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