CRD89C51RD

Data Sheet Rev 1.0

Product List

CRD89C51RD-25, 25MHz 64KB internal flash MCU
CRD89C51RD-40, 40MHz 64KB internal flash MCU

Description

The CRD89C51RD series product is an 8 - bit single chip micro controller unit (MCU) with 64KB flash & 1K byte RAM embedded. It has In-System Programming (ISP) and is a derivative of the 8052 micro controller family. It has 5-channel SPWM build-in. With its hardware features and powerful instruction set, it's a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory either for program or for data or mixed.

To program the on-chip flash memory, either a commercial parallel programmer or the serial interface via ISP.

Ordering Information

CRD89C51RD-40-QG 64KB Flash, 40 MHz, 5V, 44 QFP
CRD89C51RD-40-LG 64KB Flash, 40 MHz, 5V, 44 PLCC
CRD89C51RD-40-PG 64KB Flash, 40 MHz, 5V, 40 PDIP
CRD89C51RD-25-QG 64KB Flash, 25 MHz, 5V, 44 QFP
CRD89C51RD-25-LG 64KB Flash, 25 MHz, 5V, 44 PLCC
CRD89C51RD-25-PG 64KB Flash, 25 MHz, 5V, 40 PDIP

Features

- 64K byte on chip program Flash with in-System Programming(ISP)
- 1024 bytes on chip data RAM
- Working Voltage:4.5V through 5.5V
- General 8052 family compatible
- 12 clocks per machine cycle
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- Serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address $0000 blank initiate ISP service program
- ISP service program space configurable in N*512 byte (N=0 to 8) size
- Five channel Specific PWM(SPWM) build-in with P1.3~P1.7

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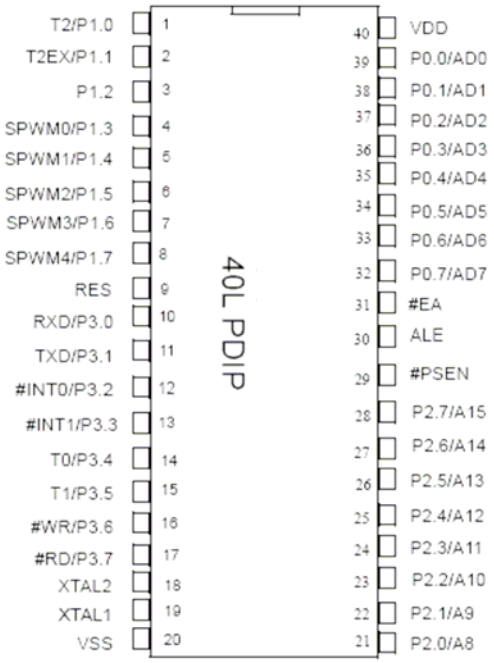
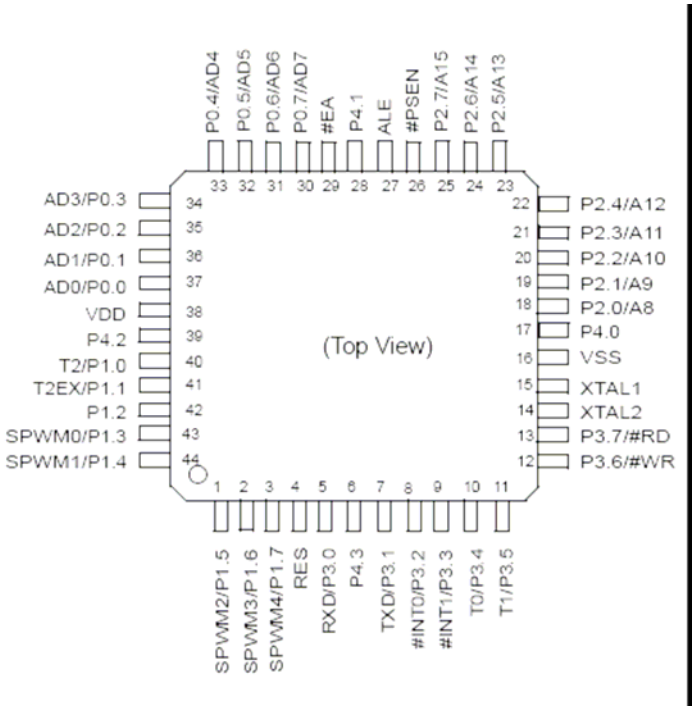
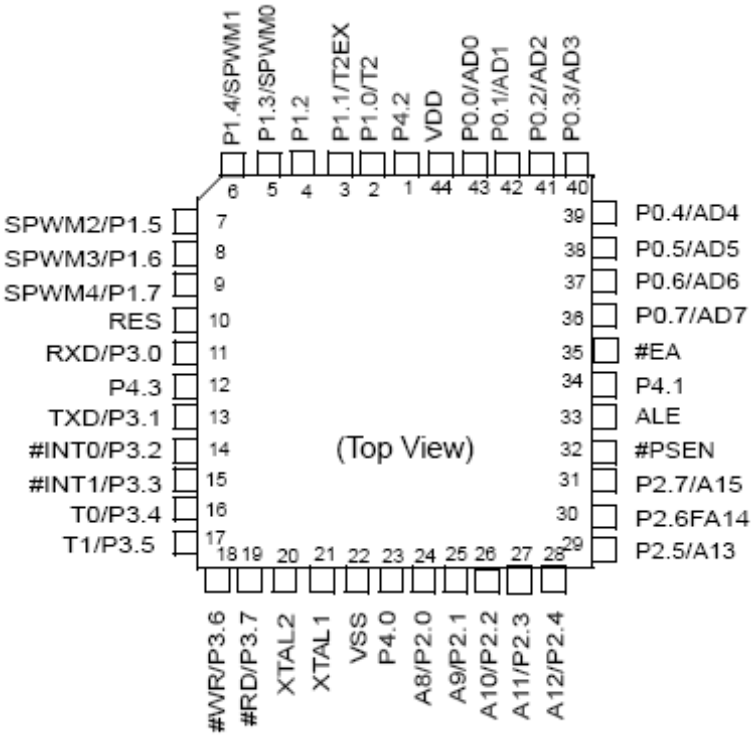
Pin Configuration







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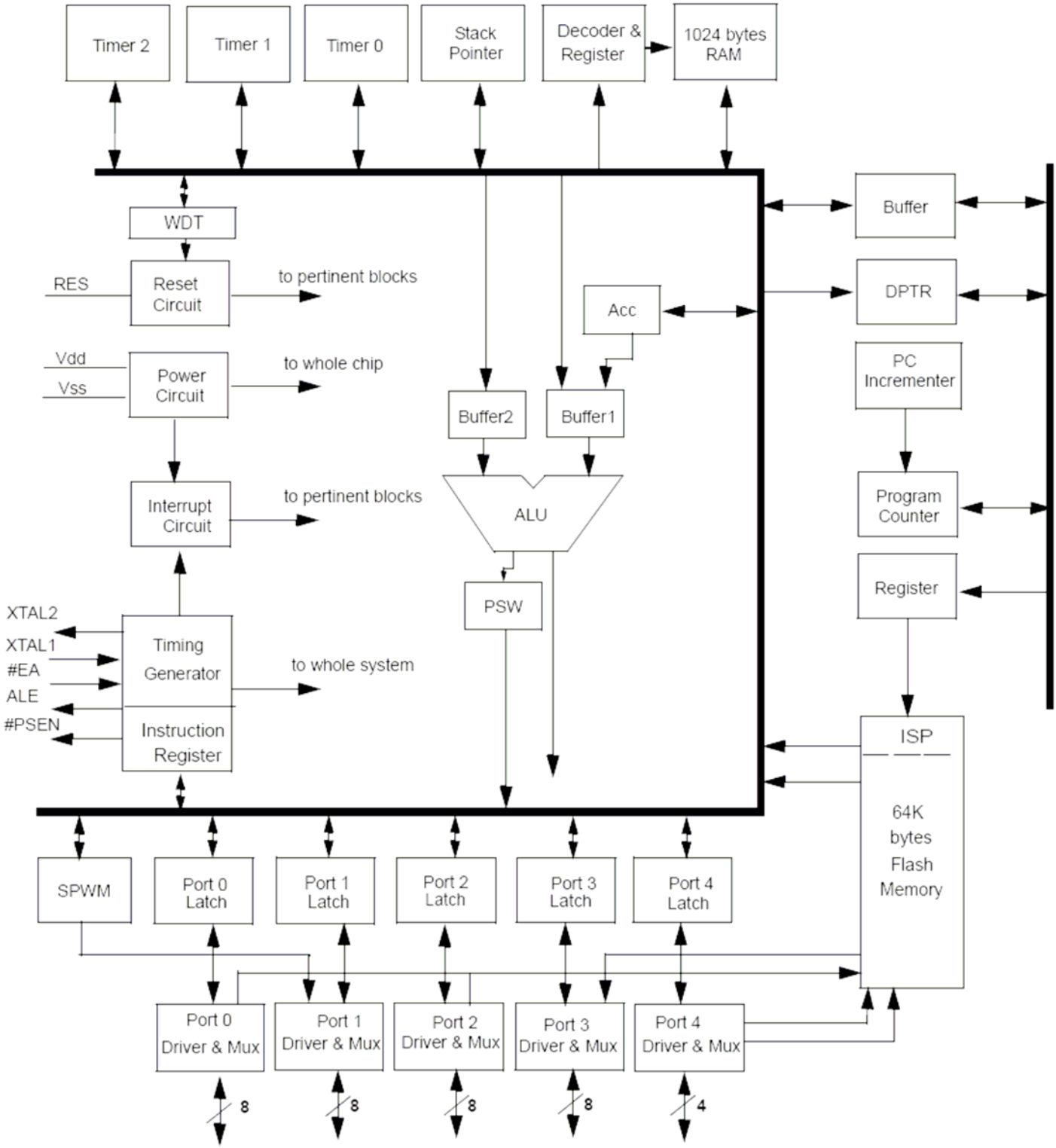
Block Diagram



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Pin Description

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0/T2		i/o	bit 0 of port 1 & timer 2 clock out
2	41	3	P1.1/T2EX		i/o	bit 1 of port 1 & timer 2 control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3/SPWM0		i/o	bit 3 of port 1 & SPWM channel 0
5	44	6	P1.4/SPWM1		i/o	bit 4 of port 1 & SPWM channel 1
6	1	7	P1.5/SPWM2		i/o	bit 5 of port 1 & SPWM channel 2
7	2	8	P1.6/SPWM3		i/o	bit 6 of port 1 & SPWM channel 3
8	3	9	P1.7/SPWM4		i/o	bit 7 of port 1 & SPWM channel 4
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR		i/o	bit 6 of port 3 & ext. memory write
17	13	19	P3.7/#RD		i/o	bit 7 of port 3 & ext. memory read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	I	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage

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	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of port 4

Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only. Address $80 to $FF is SFR area.
The following table lists the SFRs which are identical to general 8052 as well as CRD89C51RD Extension SFRs .

Special Function Register (SFR) Memory Map

$F8									$FF
$F0	B				**ISPFAH**	**ISPFAL**	**ISPFD**	**ISPC**	$F7
$E8									$EF
$E0	ACC								$E7
$D8	**P4**								$DF
$D0	PSW								$D7
$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			$CF
$C0									$C7
$B8	IP							**SCONF**	$BF
$B0	P3								$B7
$A8	IE				**SPWMD4**				$AF
$A0	P2			**SPWMC**	**SPWMD0**	**SPWMD1**	**SPWMD2**	**SPWMD3**	$A7
$98	SCON	SBUF		**P1CON**				**WDTC**	$9F
$90	P1								$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH		**RCON**		PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for CRD89C51RD

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	**RCON**	******00							RAMS1	RAMS0
9BH	**P1CON**	00000***	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWM0E			
9FH	**WDTC**	0*0**000	WDTE	Reserved**	CLEAR			PS2	PS1	PS0
A3H	**SPWMC**	******00							PDIV1	PDIV0
A4H	**SPWMD0**	00H	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
A5H	**SPWMD1**	00H	SPWMD14	SPWMD13	SPWMD12	SPWMD11	SPWMD10	BRM12	BRM11	BRM10
A6H	**SPWMD2**	00H	SPWMD24	SPWMD23	SPWMD22	SPWMD21	SPWMD20	BRM22	BRM21	BRM20

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A7H	**SPWMD3**	00H	SPWMD34	SPWMD33	SPWMD32	SPWMD31	SPWMD30	BRM32	BRM31	BRM30
ACH	**SPWMD4**	00H	SPWMD44	SPWMD43	SPWMD42	SPWMD41	SPWMD40	BRM42	BRM41	BRM40
BFH	**SCONF**	0****010	WDR					ISPE	OME	ALEI
C9H	**T2MOD**	******00	*	*	*	*	*	*	T2OE	DCEN
D8H	**P4**	****1111					P4.3	P4.2	P4.1	P4.0
F4H	**ISPFAH**	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	**ISPFAL**	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	**ISPFD**	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	**ISPC**	0*****00	START						F1	F0

** Keep to “0” when write WDTC (9FH).

Extension Function Description

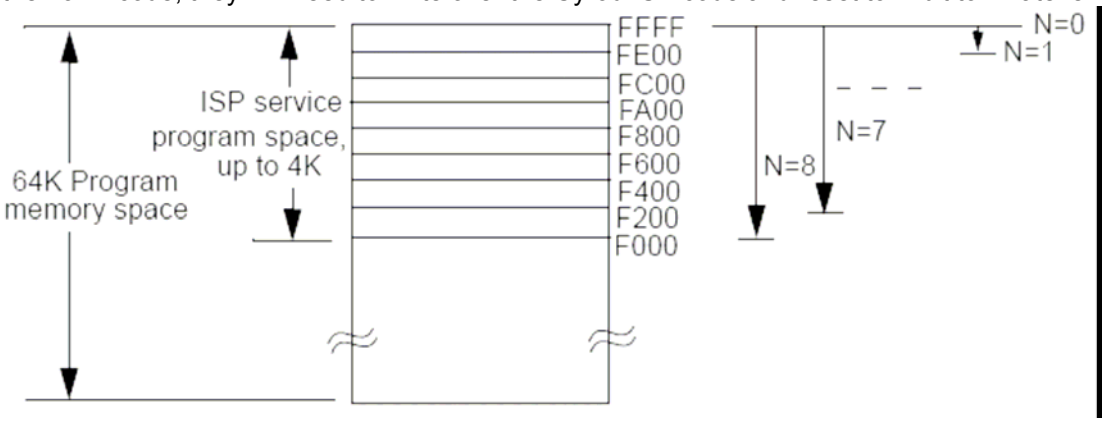
1. Memory Structure

The CRD89C51RD is the general 8052 hardware core to integrate the ISP function as a single chip micro controller. It’s memory structure follows general 8052 structure .

1.1 Program Memory

The CRD89C51RD has 64K byte on-chip flash memory which can be used as general program memory and which includes up to 4KB of specific ISP service program memory space. The address range for the 64KB is $0000 to $FFFF. The address range for the ISP service program is $F000 to $FFFF. The ISP service program size can be partitioned as N blocks of 512 byte (N=0 to 8). When N=0, it means there is no ISP service program space available and a total of 64KB of Flash memory are available for program memory. When N=1, it means that memory address $FE00 to $FFFF is reserved for the ISP service program and 63.5KB of Flash memory are available for program memory. When N=2, it means that memory address $FC00 to FFFF is reserved for the ISP service program and 63KB of Flash memory are available for program memory,...etc. Value N can be set and programmed into CRD89C51RD by writer.

The CRD89C51RD comes pre-loaded with Cyrod’s standard ISP service program. This ISP code is <1KB in size and therefore the N bit is preset to N=2 (i.e. 1KB of Flash space reserved for the Cyrod ISP code). If the user elects to use their own code, they will need to write over the Cyrod ISP code and reset to N bit to whatever value (0 to 8) is required.



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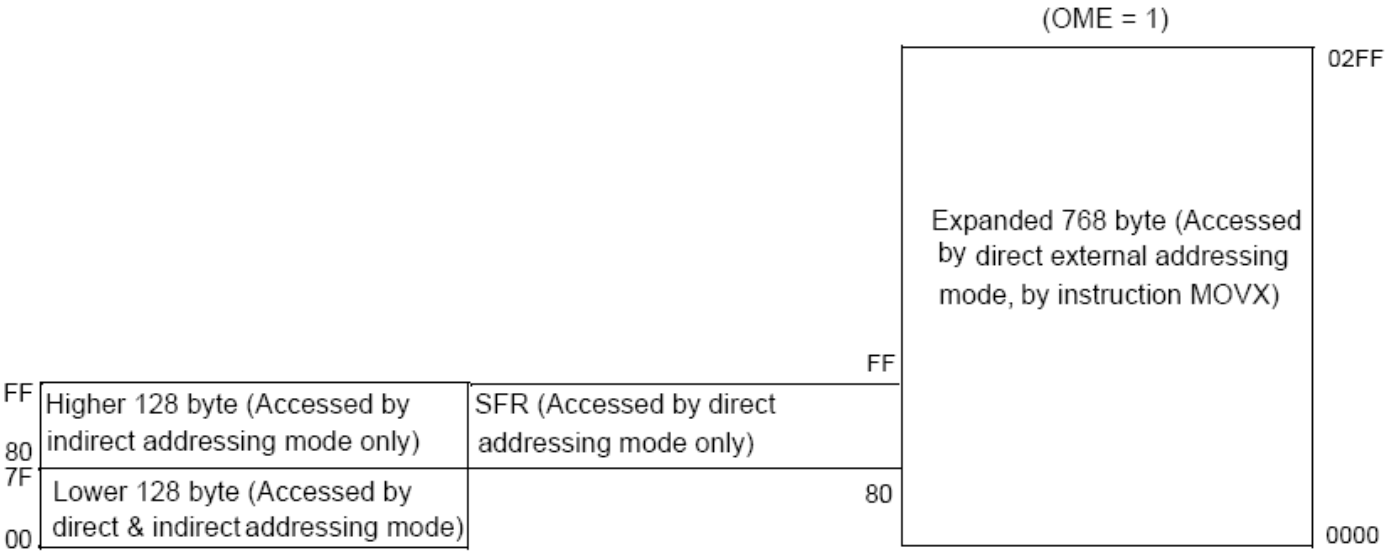
1.1.1 Program Code Security

The MOVC instruction executed from an external program memory space will not be able to fetch internal codes from on chip program memory after the chip is protected on the Writer.

1.2 Data Memory

The CRD89C51RD has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX.).



1.2.1 Data Memory - Lower 128 byte ($00 to $7F)

Data Memory $00 to $FF is the same as 8052.

The address $00 to $7F can be accessed by direct and indirect addressing modes.

Address $00 to $1F is register area.

Address $20 to $2F is memory bit area.

Address $30 to $7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte ($80 to $FF)

The address $80 to $FF can be accessed by indirect addressing mode .

Address $80 to $FF is data area.

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1.2.3 Data Memory - Expanded 768 bytes ($0000 to $02FF)

From external address $0000 to $02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX).

If the address of instruction MOVX @DPTR is larger than $02FF then CRD89C51RD will generate the external memory control signal automatically. The bit 1 (OME) of special function register $BF (SCONF) can enable or disable this expanded 768 byte RAM. The default setting of OME bit is 1 (enable).

1.3 System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	DFEN	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1.
ISPE: ISP function enable bit
OME: 768 bytes on-chip RAM enable bit .
ALEI: ALE output inhibit bit, to reduce EMI .

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.
The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768 byte RAM. The default setting of OME bit is 1 (enable).
The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

2. Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, $D8)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

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3. In-System Programming (ISP) Function

The CRD89C51RD can generate flash control signals by internal hardware circuitry. The user can utilize the flash control register, flash address register and flash data register to perform the ISP function without removing the CRD89C51RD from the system. The CRD89C51RD provides internal flash control signals which can do flash program/chip erase/page erase/protect functions.

3.1 ISP Service Program

The ISP service program is a firmware program which resides in the ISP service program space of the Flash memory. If the user elects to develop their own ISP service program, they will need to determine the size of the ISP service code and set the N bit accordingly. Once the code is complete, the users ISP code will need to be programmed into the CRD89C51RD.

The ISP service program can be initiated under CRD89C51RD active or idle mode. It cannot be initiated under power down mode.

3.2 Lock Bit (N)

The Lock Bit N has two functions: one is to define the ISP service program size and the other is to lock the ISP service program space from the flash erase/write function.

The ISP service program space address range is from $F000 to $FFFF. It is divided into blocks of N*512 byte. (N=0 to 8). When N=0 means no ISP function, all of 64K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 512 byte while the remaining 63.5K bytes of flash memory can be used as program memory, etc. The maximum ISP service program size allowed is 4K byte for N=8. Under this configuration, the usable program memory space is 60K bytes.

After N is determined, the CRD89C51RD will reserve the ISP service program space downward from the top of the program address $FFFF. The start address of the ISP service program located at $Fx00 while x is an even number, depending on the lock bit N. Please see page 6 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash has not been protected, the contents of the ISP service program still can be read. If the flash has been protected, the overall content of the flash program memory space, including the ISP service program space, can not be read.

3.3 Program the ISP Service Program

After the Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If the user needs to erase the locked ISP service program, he can do it by a writer only. User can not change ISP service program when CRD89C51RD was in system.

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3.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are three ways to do so:
(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.
(2) Execute 'JUMP' instruction can load the start address of the ISP service program to PC.

User can initiate general 8052 INT function to initiate the ISP service program. After ISP service program executed, user need to reset the CRD89C51RD, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

ISP Registers - ISPFAH, ISPFAL, ISPFD and ISPC

ISP Flash Address-High Register(ISPFAH,$F4)

	bit-7							bit-0
	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA15 ~ FA8: flash address-high for ISP function

ISP Flash Address-Low Register (ISPFAL,$F5)

	bit-7							bit-0
	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA7 ~ FA0: flash address-low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

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ISP Flash Data Register (ISPFD, $F6)

	bit-7							bit-0
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FD7 ~FD0 : flash data for ISP function

The ISPFD provide the 8-bit data for ISP function

ISP Flash Control Register (ISPC, $F7)

	bit-7							bit-0
	START	Unused	Unused	Unused	Unused	Unused	ISPF1	ISPF0
Read / Write:	R/W	-	-	-	-	-	R/W	R/W
Reset value:	0	*	*	*	*	*	0	0

F[1: 0]: ISP function select bit
START: ISP function start bit
= 1: start ISP function which indicated by bit 1, bit 0 (F1, F0)
= 0: no operation

The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPFD register to enable the START bit write attribute. That is:

```
MOV ISPFD, #55H
MOV ISPFD, #0AAH
MOV ISPFD, #55H
```

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the CRD89C51RD hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check START bit status by software method.

F[1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase
11	Chip erase

F[1:0]: ISP function select bit

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One page of flash memory is 512 byte.

To perform byte program/page erase ISP function, user need to specify flash address at first. When performing page erase function, CRD89C51RD will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $XYMN
page erase function will erase from $XY00 to $X(Y+1)FF (Y:even number), or
page erase function will erase from $X(Y-1) 00 to $XYFF (Y:odd number)

To perform the chip erase ISP function, CRD89C51RD will erase all the flash program memory except the ISP service program space, also, CRD89C51RD will un-protect the flash memory automatically. To perform chip protect ISP function, the CRD89C51RD flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV SCONF,#04H      ; enable CRD89C51RD ISP function
MOV ISPFAH,#10H     ; set flash address-high, 10H
MOV ISPFAL,#05H     ; set flash address-low, 05H
MOV ISPFD,#22H      ; set flash data to be programmed, data = 22H
MOV ISPC,#80H       ; start to program #22H to the flash address $1005H
                    ; after byte program finished, START bit of ISPC will be reset to 0 automatically
                    ; program counter then point to the next instruction
```

ISP Registers - System Control Register (SCONF,$BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

The bit 2 (ISPE) of SCONF is ISP enable bit. User can enable overall CRD89C51RD ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally.

4. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover form abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever un-predicted reset happened

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The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when CRD89C51RD been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

4.1 Watch Dog Timer Registers: WDTC and SCONF

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	bit-7							bit-0
	WDTE	reserved**	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

** Keep to “0” when write WDTC (9FH).

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS[2:0] : Overflow period select bits

PS [2:0]	Divider(OSC in)	Time Period (ms) @ 40 MHZ
000	8	13.12.048
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

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Watch Dog Timer Register - System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	1	0

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

5. Reduce EMI Function

The CRD89C51RD allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

6. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module has five 8-bit channels, each channel contains a 8-bit wide SPWM data register (SPWMD) to decide number of continuous pulses within a SPWM frame cycle.

6.1 SPWM Function Description:

Each 8-bit SPWM channel is composed of an 8-bit register which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The PDIV[1:0] settings of SPWMC ($A3) register are dividend of Fosc to be SPWM clock, Fosc/2^(PDIV[1:0]+1). The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is [Fosc/2^(PDIV[1:0]+1)]/32.

6.2 SPWM Registers - P1CON, SPWMC, SPWMR[4:0]

SPWM Registers - Port1 Configuration Register (P1CON, $9B)

	bit-7							bit-0
	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWM0E	Unused	Unused	Unused
Read / Write:	R/W	R/W	R/W	R/W	R/W	-	-	-
Reset value:	0	0	0	0	0	*	*	*

SPWM[4:0]E :When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Five bits are cleared upon reset.

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SPWM Registers -SPWM Control Register (SPWMC, $A3)

bit-7 bit-0

	Unused	Unused	Unused	Unused	Unused	Unused	PDIV1	PDIV0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

PDIV[1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

PDIV1	PDIV0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Data Register (SPWMD[4:0], $AC, $A7 ~$A4)

bit-7 bit-0

	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [2:0]2	BRM [2:0]1	BRM [2:0]0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

SPWMD[4:0][4:0]: content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[4:0][2:0]: will insert certain narrow pulses among an 8-SPWM-cycle frame .

N = BRM[4:0][2:0]	Number of SPWM cycles inserted in an 8-cycle frame
XX1	1
X1X	2
1XX	4

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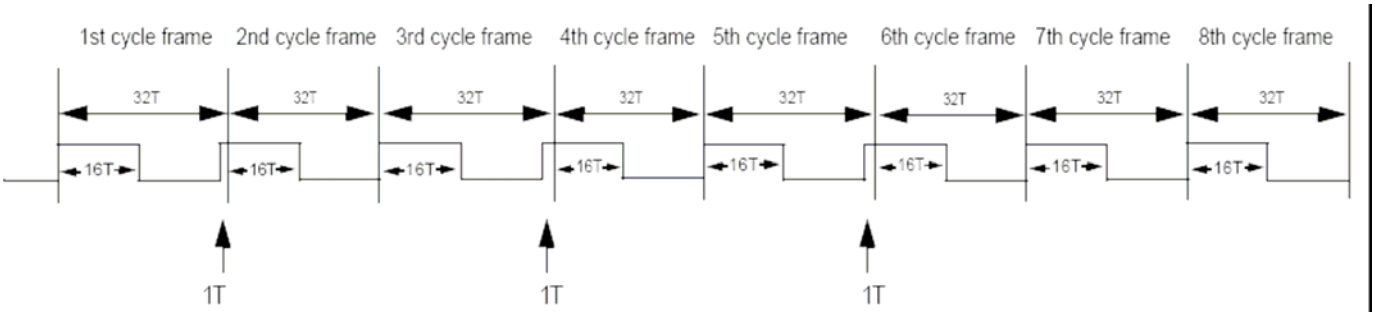
Example of SPWM timing diagram:

```
MOV SPWMD0 , #83H          ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM[2:0] = 3
MOV   P1CON , #08H         ; Enable P1.3 as SPWM output pin
```



(narrow pulse inserted by BRM0[2:0] setting, here BRM0[2:0]=3)

SPWM clock = 1 / T = Fosc / 2^(PDIV +1)
The SPWM output cycle frame frequency = SPWM clock / 32 = [Fosc/2^(SPFS[1:0]+1)]/32

If user use Fosc=20MHz, SPFS[1:0] of SPWMC=#03H, then
SPWM clock = 20MHz/2^4 = 20MHz/16 = 1.25MHz
SPWM output cycle frame frequency = (20MHz/2^4)/32=39.1KHz

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

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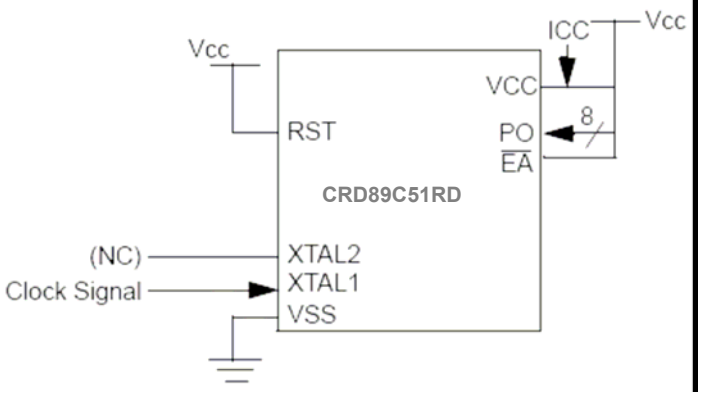
DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 ℃
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1:Under steady state (non-transient) conditions, IOL must be externally limited as follows :
Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 1,2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

ICC Active mode test circuit



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AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min	Typ	Max	Min	Typ	Max		
T_LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T_AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T_LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T_LLIV	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T_LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T_PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T_PLIV	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T_PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T_PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T_AVIV	Address to Valid Instruction In	RD			292			5xT -20	nS	
T_PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T_RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T_WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T_RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T_RHDX	Data Hold after #RD	RD	0			0			nS	
T_RHDZ	Data Float after #RD	RD			145			2xT+20	nS	
T_LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T_AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T_LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT-10		3xT+10	nS	
T_AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT-20			nS	
T_QVWH	Data Valid to #WR High	WRT	403			7xT-35			nS	
T_QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T_WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T_RLAZ	#RD low to Address Float	RD						5	nS	
T_YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T_CHCL	clock fall time								nS	
T_CLCX	clock low time								nS	
T_CLCH	clock rise time								nS	
T_CHCX	clock high time								nS	
T_TCLCL	clock period			63			1/fosc		nS	

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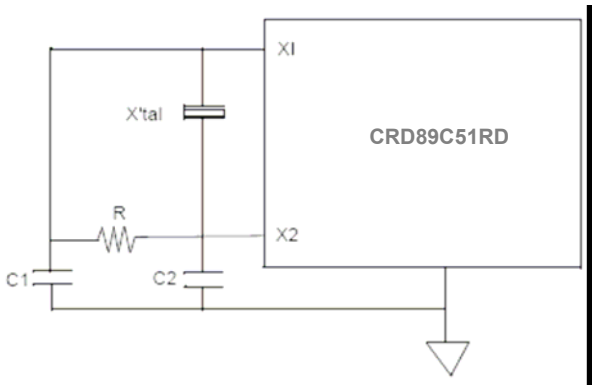
ISP Test Conditions

(40 MHZ, typical operating conditions, valid for CRD89C51RD series)

Symbol	MAX	Remark
Chip erase	3000ms	Vcc = 5V
Page erase	10ms	"
Program	30us	"
Protect	400us	"

Application Reference

Valid for CRD89C51RD				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



NOTE: Oscillator circuit may differ with different crystal or ceramic resonator in higher oscillation frequency due to each crystal or ceramic resonator having its own characteristics. User should check with the crystal or ceramic resonator manufacture for appropriate value of external components.

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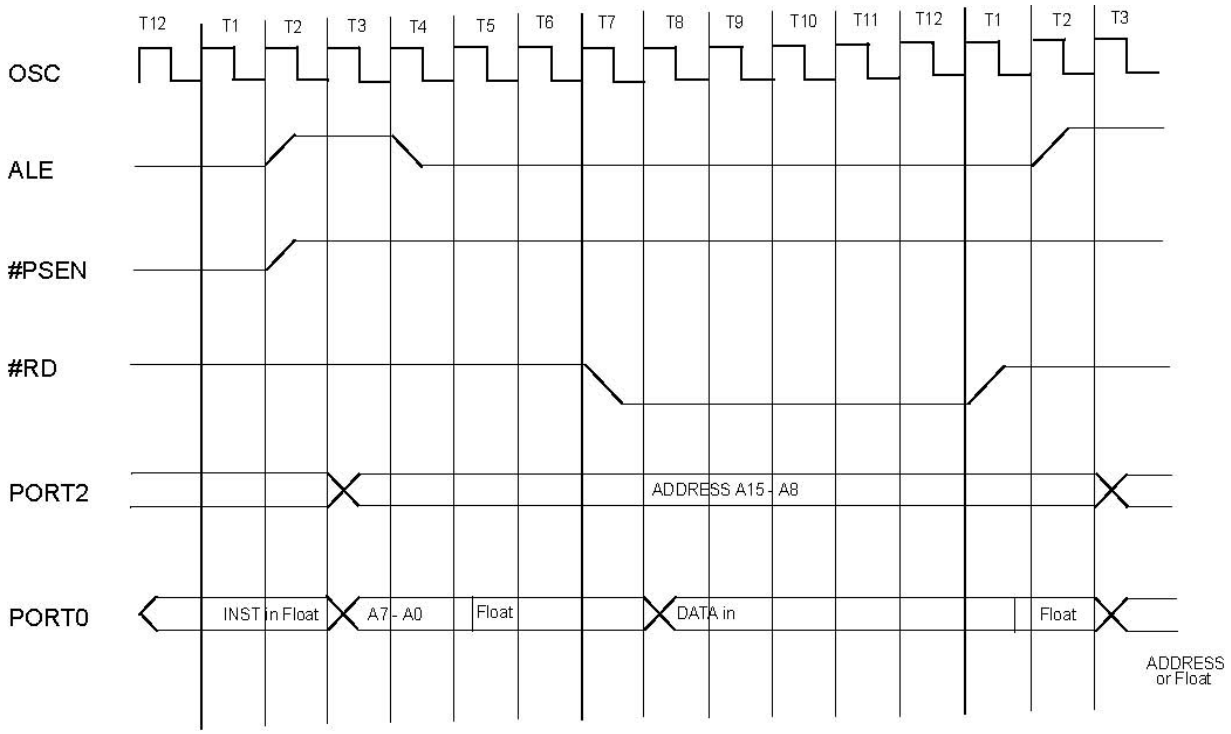
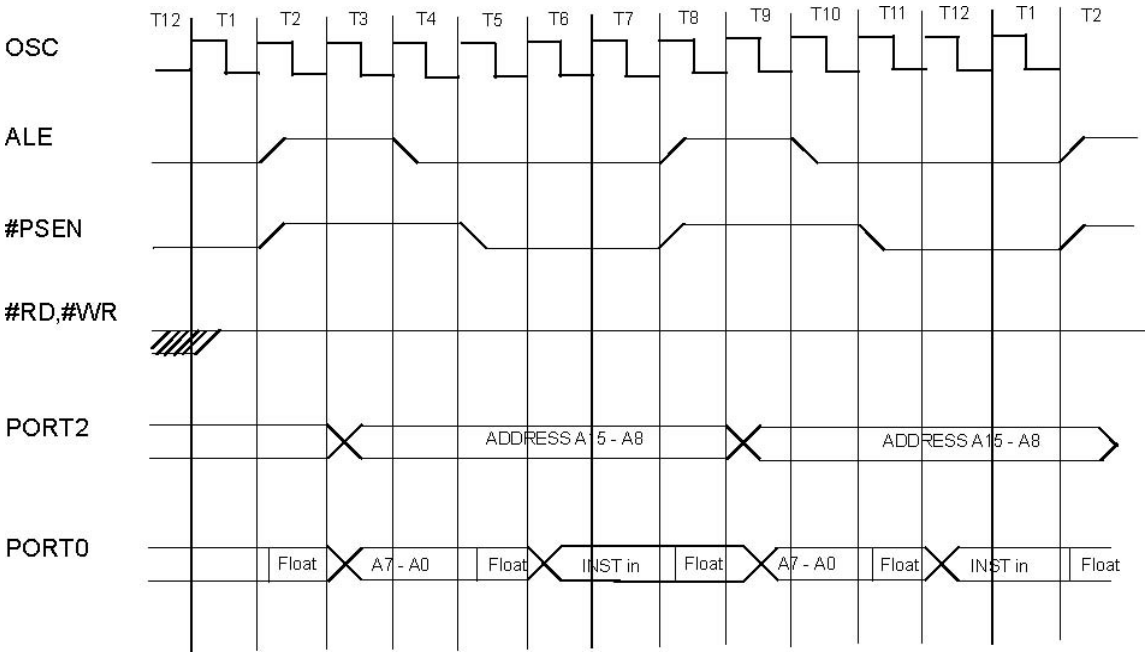
Data Memory Read Cycle Timing



Program Memory Read Cycle Timing



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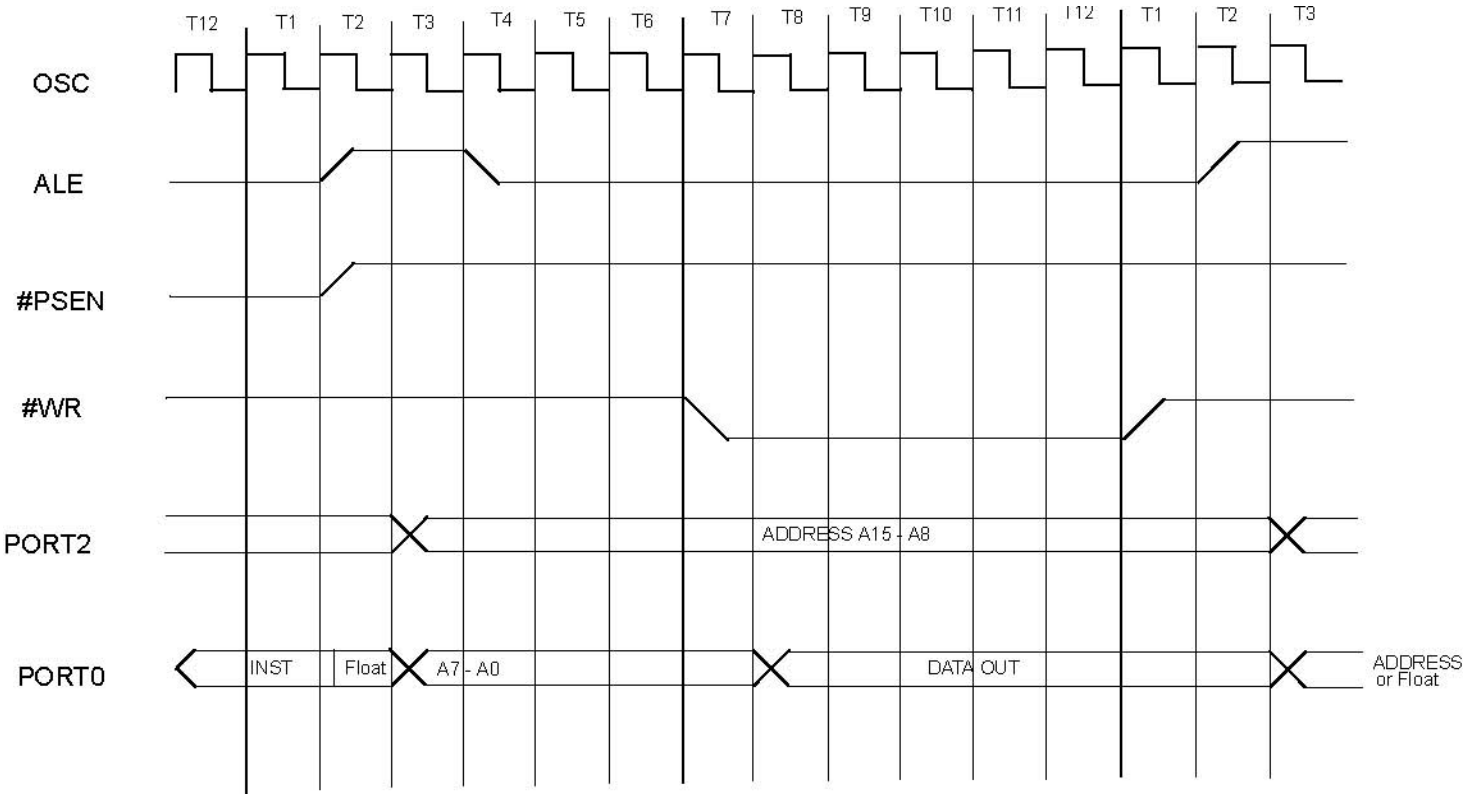
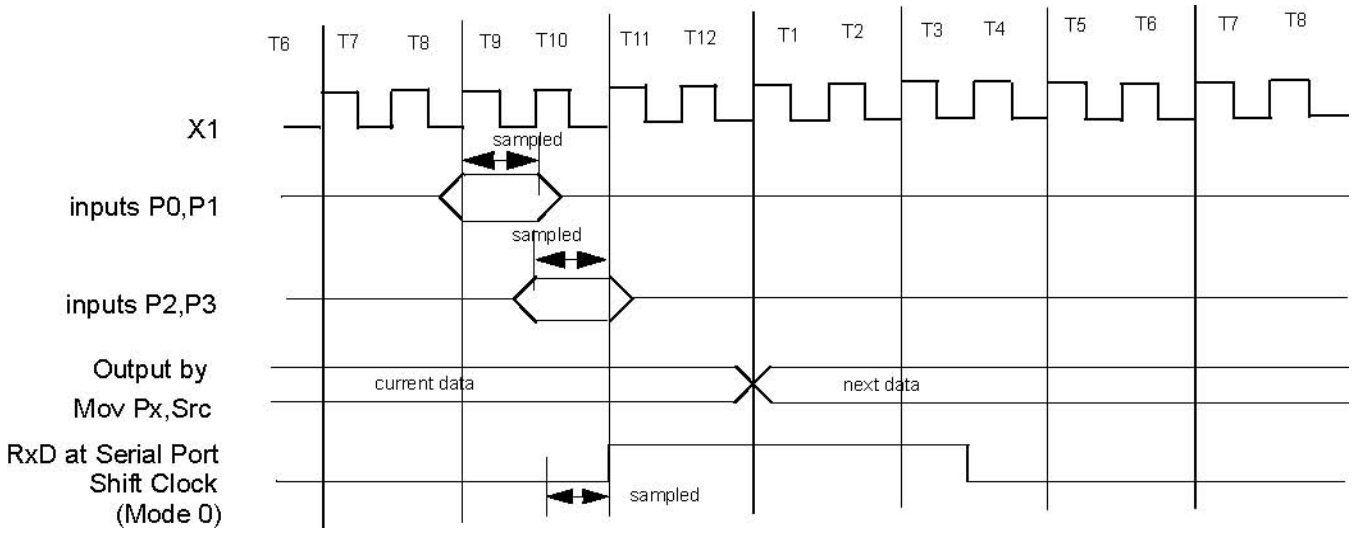
Data Memory Write Cycle Timing



I/O Ports Timing



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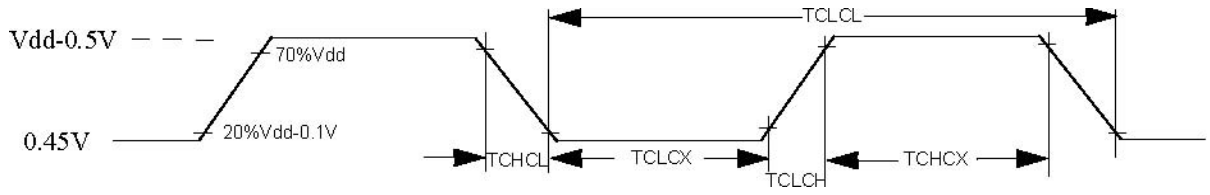
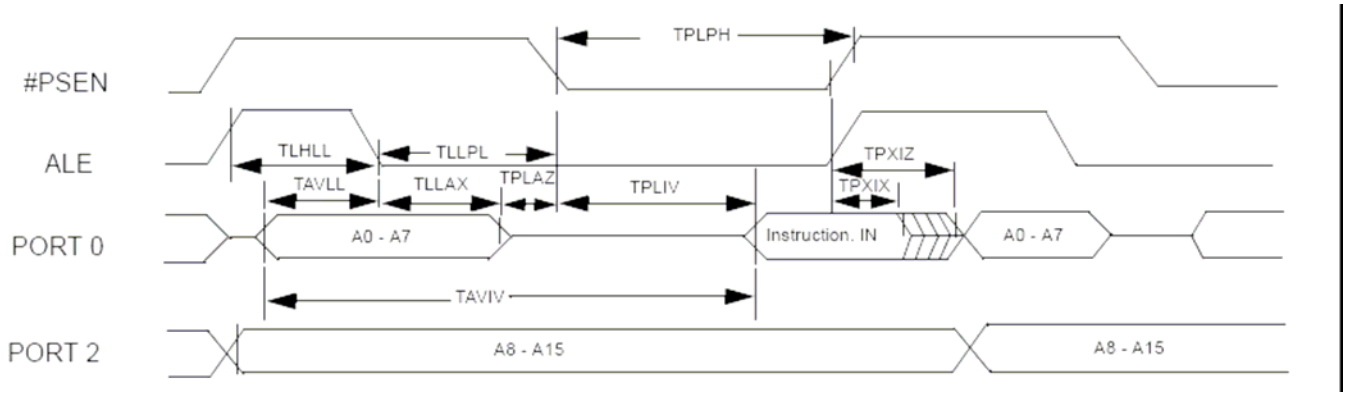
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



Tm.I External Program Memory Read Cycle



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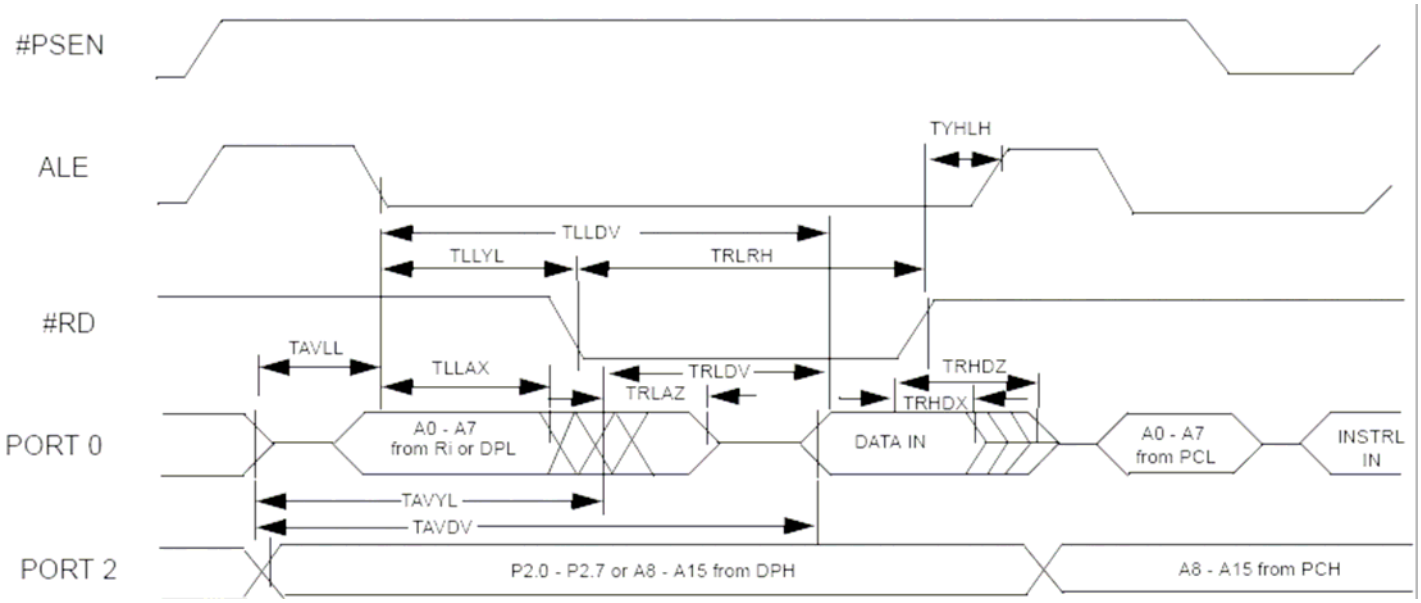
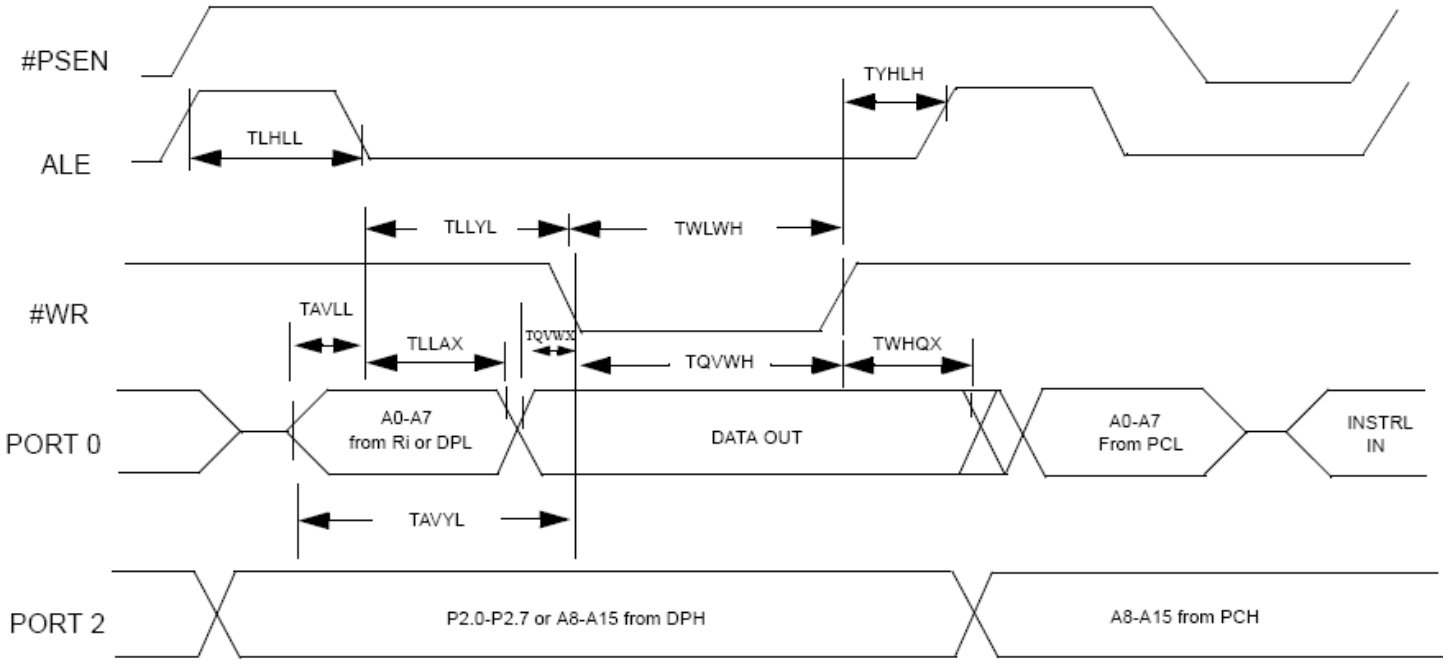
Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



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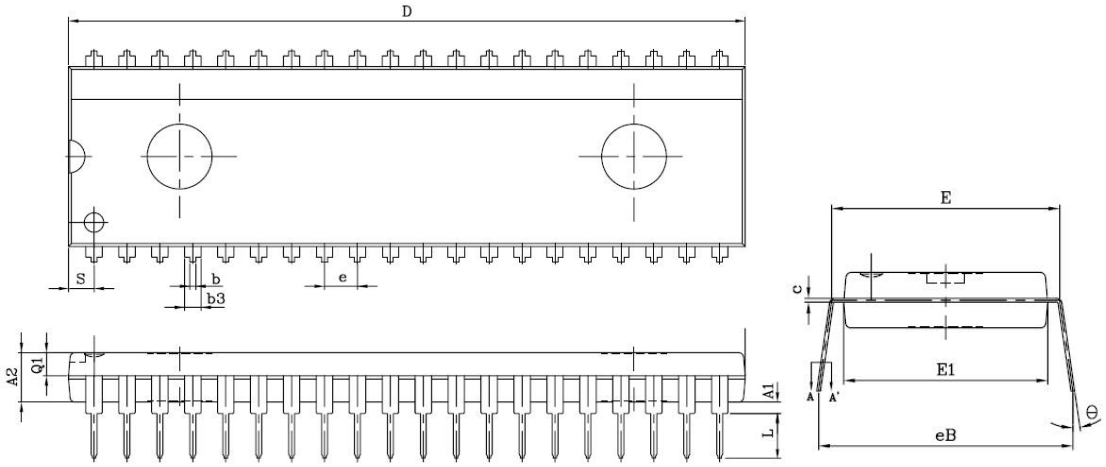
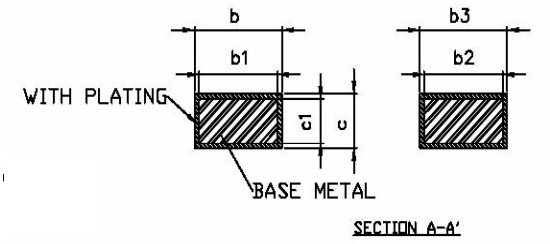
PDIP 40L (600mil) Package Information：





Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A1	0.254	—	—	10	—	—
A2	3.683	3.810	3.937	145	150	155
b	0.356	0.500	0.660	14	20	26
b1	0.356	0.457	0.508	14	18	22
b2	1.016	1.270	1.524	40	50	60
b3	1.016	1.321	1.626	40	52	64
c	0.203	0.254	0.432	8	10	17
c1	0.203	0.254	0.356	8	10	14
D	52.07	52.2	52.32	2050	2055	2060
E	14.99	15.24	15.49	590	600	610
E1	13.69	13.87	13.94	539	546	549
e	—	2.540	—	—	100	—
eB	15.75	16.26	16.76	620	640	660
L	2.921	3.302	3.683	115	130	145
S	1.727	1.981	2.235	68	78	88
Q1	1.651	1.778	1.905	65	70	75
θ	0°	—	10°	0°	—	10°

Note:
1. Refer to JEDEC STD.MS-011(AC).
2. Dimension D and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D and E1 are maximum plastic body size dimension include mold mismatch.
3. Dimension b3 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.2mm.

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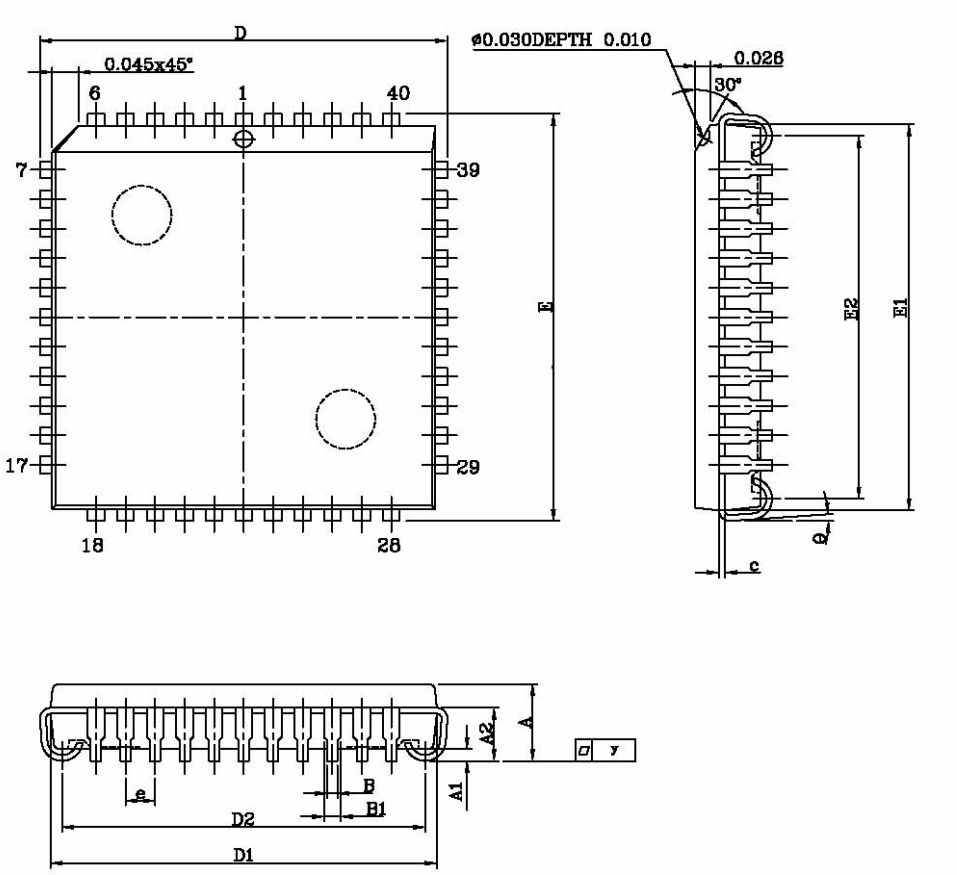
PLCC 44L Package Information：



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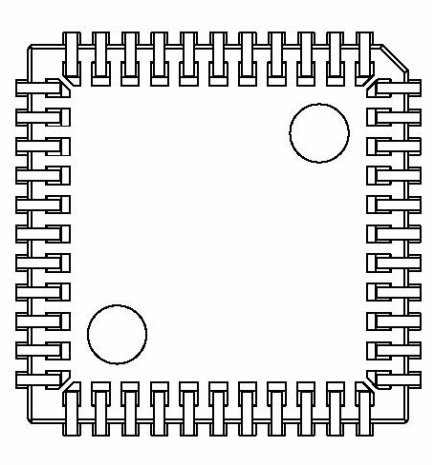

UNIT SYMBOL	INCH(REF)	MM(BASE)
A	0.180(MAX)	4.572(MAX)
A1	0.024 ±0.005	0.52 ±0.14
A2	0.105 ±0.005	2.667 ±0.127
B	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
B1	0.028 + 0.004 - 0.002	0.711 + 0.102 - 0.051
c	0.010(TYP)	0.254(TYP)
D	0.690 ±0.010	17.526 ±0.254
D1	0.653 ±0.003	16.586 ±0.076
D2	0.610 ±0.020	15.494 ±0.508
E	0.690 ±0.010	17.526 ±0.254
E1	0.653 ±0.003	16.586 ±0.076
E2	0.610 ±0.010	15.494 ±0.254
e	0.050(TYP)	1.270(TYP)
y	0.003(MAX)	0.076(MAX)
θ	0~5°	0~5°

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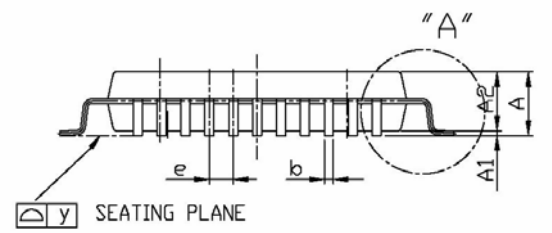
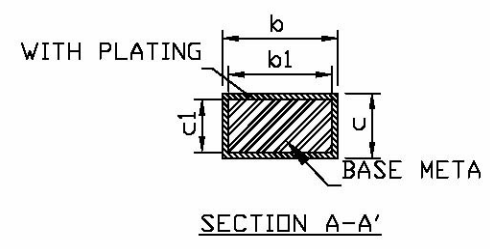
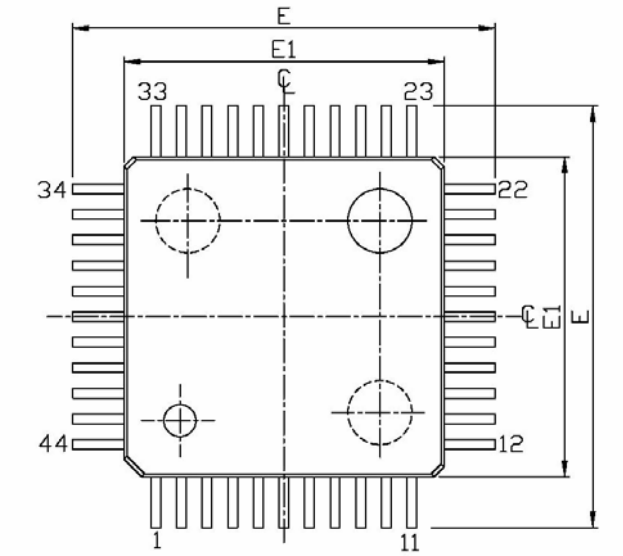
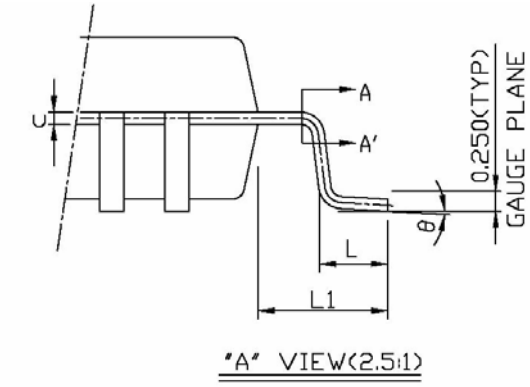
QFP 44L(10x10x2.0mm) Package Information：









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Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A	—	—	2.45	—	—	964
A1	0.05	0.15	0.25	2.1	6.0	9.6
A2	1.90	2.00	2.10	74.8	78.7	82.7
b	0.29	0.32	0.45	11.4	12.6	17.7
b1	0.29	0.30	0.41	11.4	11.8	16.1
c	0.11	0.17	0.23	4.3	6.7	9.1
c1	0.11	0.15	0.19	4.3	5.9	7.5
E	13.00	13.20	13.40	512	520	528
E1	9.90	10.00	10.10	390	394	398
【e】	—	0.800	—	—	31.5	—
L	0.73	0.88	1.03	28.7	34.6	40.6
L1	1.50	1.60	1.70	59.1	63.0	66.9
y	—	—	0.076	—	—	3
θ	0°	—	7°	0°	—	7°

Note:

1. Refer to JEDC STD.MS-022(AB).
2. Dimension E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.E1 are maximum plastic body size dimension include mold mismatch .
3. Dimension b does not include dambar protrusion .Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.1 mm.

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