

CRD89C51RA2

8 bit microcontroller with 8KB program Flash, 4KB ISP Flash and 1KB RAM

Product List

CRD89C51RA2-25, 5V 25MHz Flash MCU
CRD89L51RA2-25, 3V 25MHz Flash MCU

Description

The CRD89C51RA2 series product is an 8-bit single chip microcontroller with 8K bytes Flash, 4K bytes ISP Flash/EEPROM and 1K byte RAM. It is a derivative of the 8052 microcontroller family. Its instruction set is fully compatible to the 8052 instruction set. It can be programmed either through the ISP bootloader, or through an external programmer. The unused part of the 4k bytes ISP service program area, can be used as EEPROM. After programming, the code are can be protected to prevent illegal read, or write. It provides peripherals that can make many applications more efficient, such as dual DPTR, UART, WDT, Pulse Width Modulation (PWM), capture and compare Timers, PCA and EEI. These are functionally compatible with peripherals available in all popular 8052 derivatives. Power saving modes (Idle, Stop) and low EMI characteristics combine to the above characteristics to form a powerful microcontroller.

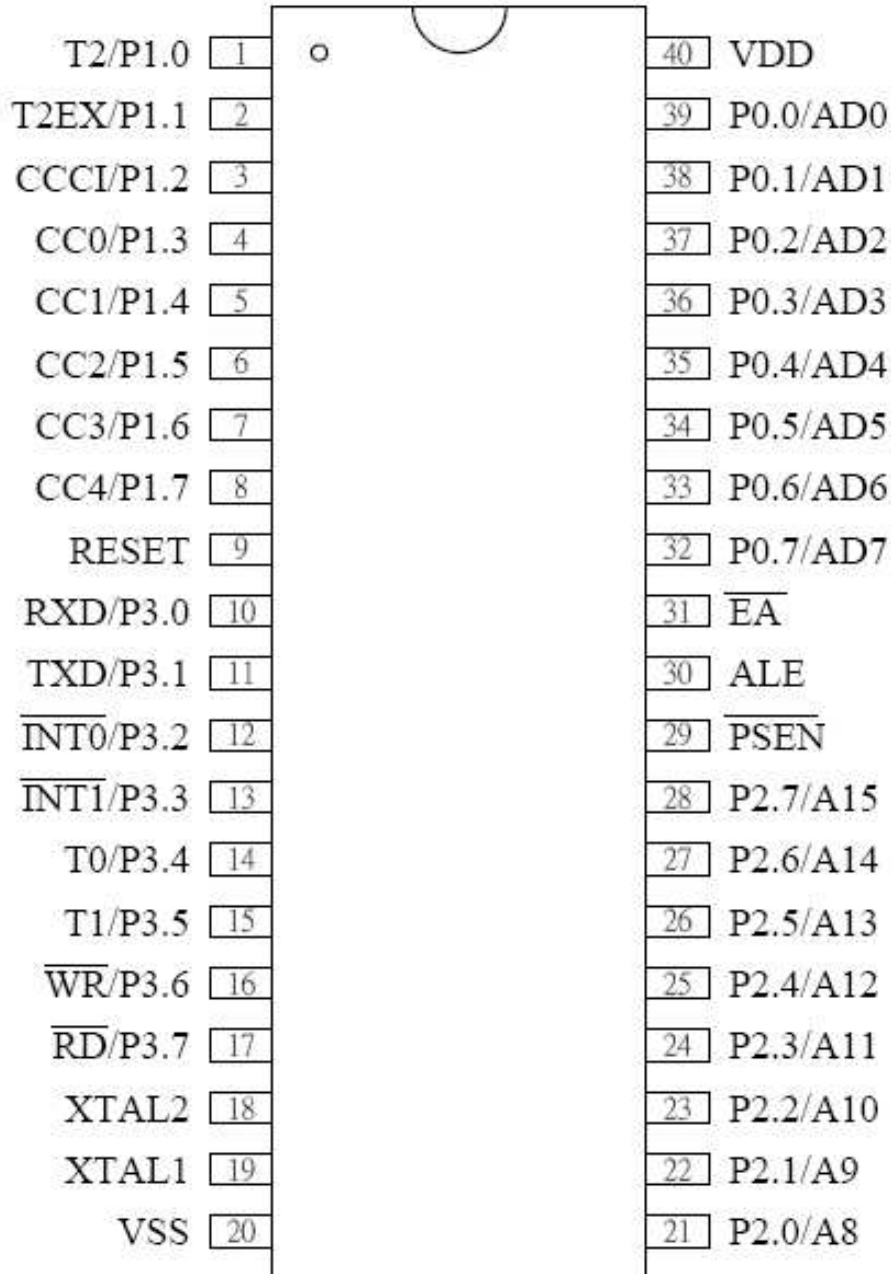
Features

- Operating Voltage: 2.7V ~ 3.6V or 4.5V ~ 5.5V
- General 8052 family compatibility
- 12 or 6 clocks per machine cycle
- Frequency runs up to 25MHz
- 8K bytes on chip program Flash
- 4K bytes In-System Programming Flash / EEPROM
- 768 Bytes on-chip expanded RAM with disable
- 256 Bytes for standard 8052 RAM.
- fully compatible instruction set.
- External RAM address up to 64KB
- Dual 16-bit Data Pointers (DPTR0 & DPTR1)
- One channel UART
- Three 16 bit Timers/Counters
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O port for PLCC or QFP package
- Programmable Watchdog Timer (WDT)
- Programmable Counter Array (PCA)
- External interrupt 0, 1 with two priority levels
- Expanded External Interrupt (EEI) interface for eight more external interrupts.
- ISP service program space configurable in N*512 byte (N=0 to 8) size for IAP application
- ALE output select for low EMI
- Power Management (IDLE & STOP mode)
- Code protection function
- Flash Memory Endurance : 100K erase & write cycles each byte at TA=25°C
- Flash Memory Data Retention :10 years

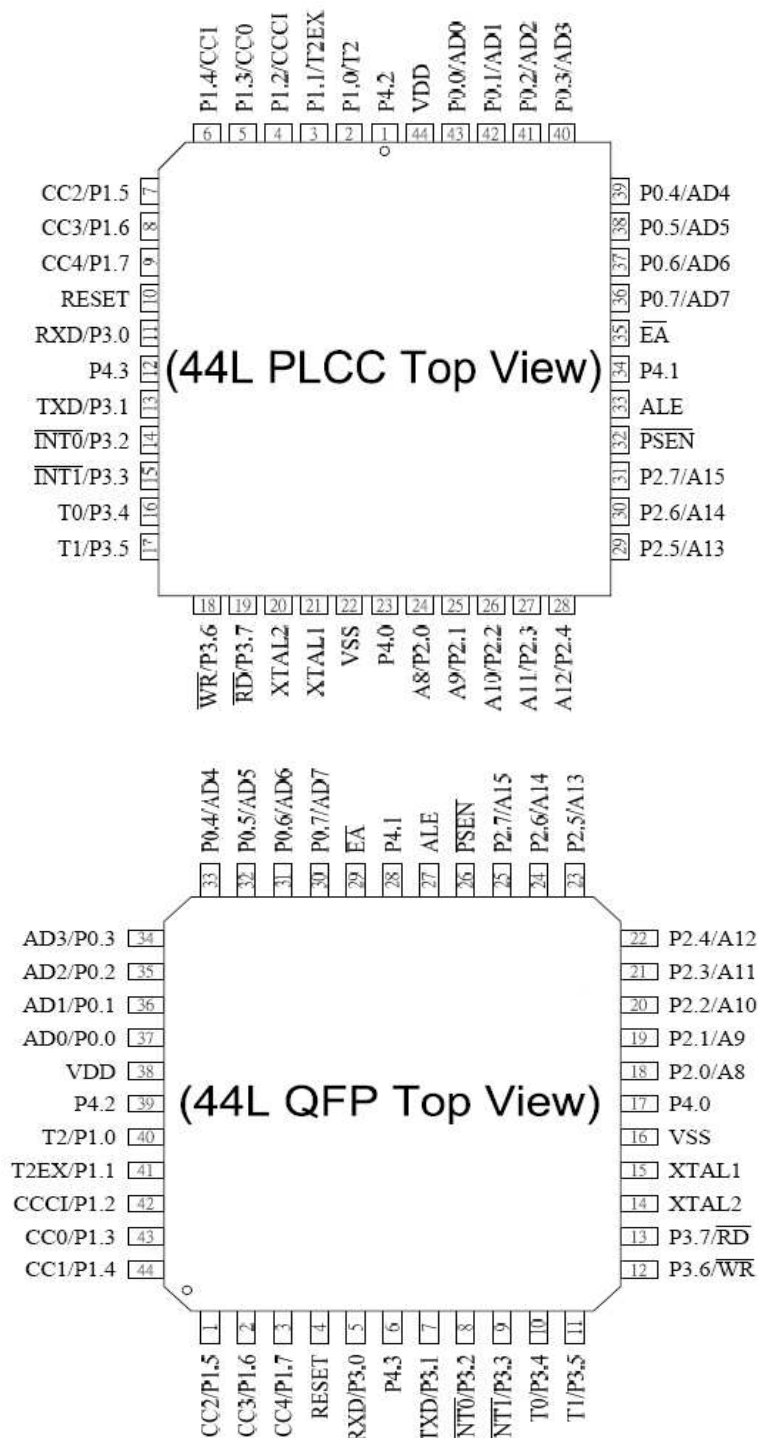
Ordering Information

CRD89C51RA2-25-PG	25MHz, PDIP, 4.5V~5.5V
CRD89C51RA2-25-LG	25MHz, PLCC, 4.5V~5.5V
CRD89C51RA2-25-QG	25MHz, PQFP, 4.5V~5.5V
CRD89L51RA2-25-PG	25MHz, PDIP, 2.7V~3.6V
CRD89L51RA2-25-LG	25MHz, PLCC, 2.7V~3.6V
CRD89L51RA2-25-QG	25MHz, PQFP, 2.7V~3.6V

Pin Assignment



Pin Assignment



Pin Description

40 pin PDIP Pin #	44 pin QFP Pin #	44 pin PLCC Pin #	Symbol	I/O	Names
1	40	2	P10/T2/EEI0/ICP_CLK	i/o	Bit 0 of port 1 & Timer 2 external input clock & EEI interrupt 0 & ICP clock input
2	41	3	P11/T2EX/EEI1/ICP_TRIG	i/o	Bit 1 of port 1 & Timer 2 capture trigger & EEI interrupt 1 & ICP Trigger (active low)
3	42	4	P12/CCCI/EEI2 / ICP_DATA	i/o	Bit 2 of port 1 & PCA External clock input & EEI interrupt 2 & ICP data/command IO
4	43	5	P13/CC0/EEI3	i/o	Bit 3 of port 1 & PCA Channel 0 & EEI interrupt 3
5	44	6	P14/CC1/EEI4	i/o	Bit 4 of port 1 & PCA Channel 1 & EEI interrupt 4
6	1	7	P15/CC2/EE5	i/o	Bit 5 of port 1 & PCA Channel 2 & EEI interrupt 5
7	2	8	P16/CC3/EEI6	i/o	Bit 6 of port 1 & PCA Channel 3 & EEI interrupt 6
8	3	9	P17/CC4/EEI7	i/o	Bit 7 of port 1 & PCA Channel 4 & EEI interrupt 7
9	4	10	RESET	i	Hardware reset input (active high)
10	5	11	P30/RXD	i/o	Bit 0 of port 3 & serial channel receive data
11	7	13	P31/TXD	i/o	Bit 1 of port 3 & serial channel transmit data
12	8	14	P32/INT0	i/o	Bit 2 of port 3 & External interrupt 0 (low, or, falling edge trigger)
13	9	15	P33/INT1	i/o	Bit 3 of port 3 & External interrupt 1 (low, or, falling edge trigger)
14	10	16	P34/T0	i/o	Bit 4 of port 3 & Timer 0 external input
15	11	17	P35/T1	i/o	Bit 5 of port 3 & Timer 1 external input
16	12	18	P36/WR	i/o	Bit 6 of port 3 & external memory write signal
17	13	19	P37/RD	i/o	Bit 7 of port 3 & external memory read signal
18	14	20	XTAL 2	o	Crystal output
19	15	21	XTAL 1	i	Crystal input
20	16	22			Ground
21	18	24	P20/A8	i/o	Bit 0 of port 2 & external memory address Bit 8
22	19	25	P21/A9	i/o	Bit 1 of port 2 & external memory address Bit 9
23	20	26	P22/A10	i/o	Bit 2 of port 2 & external memory address Bit 10
24	21	27	P23/A11	i/o	Bit 3 of port 2 & external memory address Bit 11

40 pin PDIP Pin #	44 pin QFP Pin #	44 pin PLCC Pin #	Symbol	I/O	Names
25	22	28	P24/A12	i/o	Bit 4 of port 2 & external memory address Bit 12
26	23	29	P25/A13	i/o	Bit 5 of port 2 & external memory address Bit 13
27	24	30	P26/A14	i/o	Bit 6 of port 2 & external memory address Bit 14
28	25	31	P27/A15	i/o	Bit 7 of port 2 & external memory address Bit 15
29	26	32	PSEN/ clk_out	o	Program storage enable (active low) & crystal/oscillator clock output as the clock source for the others
30	27	33	ALE	o	Address Latch Enable
31	29	35	EA	i	External Access with internal pull-up (active low)
32	30	36	P07/AD7	i/o	Bit 7 of port 0 & Bit 7 of external memory address/data
33	31	37	P06/AD6	i/o	Bit 6 of port 0 & Bit 6 of external memory address/data
34	32	38	P05/AD5	i/o	Bit 5 of port 0 & Bit 5 of external memory address/data
35	33	39	P04/AD4	i/o	Bit 4 of port 0 & Bit 4 of external memory address/data
36	34	40	P03/AD3	i/o	Bit 3 of port 0 & Bit 3 of external memory address/data
37	35	41	P02/AD2	i/o	Bit 2 of port 0 & Bit 2 of external memory address/data
38	36	42	P01/AD1	i/o	Bit 1 of port 0 & Bit 1 of external memory address/data
39	37	43	P00/AD0	i/o	Bit 0 of port 0 & Bit 0 of external memory address/data
40	38	44	Vdd		Power Supply
	17	23	P40	i/o	Bit 0 of port 4
	28	34	P41	i/o	Bit 1 of port 4
	39	1	P42	i/o	Bit 2 of port 4
	6	12	P43	i/o	Bit 3 of port 4

Special Function Registers (SFR)

Address 80h to FFh is the location of CRD89C51RA2 special function register (SFR). These locations must be accessed by direct addressing mode only.

The following tables show the SFRs, their locations and their initial values. Most of them are identically located and defined as the general 8052 series:

Table 1.1: CRD89C51RA2 SFR location

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8						KBLS	KBE	KBF	FF
F0	B				ISPF AH	ISPF AL	ISPF D	ISPC	F7
E8									EF
E0	ACC								E7
D8	P4								DF
D0	PSW								D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CF
C0									C7
B8	IP	IP1						SCONF	BF
B0	P3					RCON			B7
A8	IE	IE1							AF
A0	P2	PCAC1	PCAC2	CC0CON	CC1CON	CC2CON	CC3CON	CC4CON	A7
98	SCON	SBUF	PCACH	PCACL	CC0DH	CC0DL	CC1DH	CC1DL	9F
90	P1	CC2DH	CC2DL	CC3DH	CC3DL	CC4DH	CC4DL		97
88	TCON	TMOD	TL0	TL1	TH0	TH1	WDT C	WDT K	8F
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON	87

Table 1.2 : SFR description and initial value

Register	Location	Initial Value	Description
P0	80h	Ffh	Port 0
SP	81h	07h	Stack Pointer
DPL	82h	00h	Data Pointer Low bvte
DPH	83h	00h	Data Pointer High bvte
DPL1	84h	00h	Data Pointer 1 Low bvte
DPH1	85h	00h	Data Pointer 1 High bvte
DPS	86h	00h	Data Pointer select
PCON	87h	00h	Power control register
TCON	88h	00h	Timer control register
TMOD	89h	00h	Timer Mode
TL0	8Ah	00h	Timer 0 low bvte
TL1	8Bh	00h	Timer 1 low bvte
TH0	8Ch	00h	Timer 0 high bvte
TH1	8Dh	00h	Timer 1 high bvte

Register	Location	Initial Value	Description
DTC	8Eh	00h	Watchdog timer control register
WDTK	8Fh	00h	Watchdog timer refresh key
P1	90h	FFh	Port 1
CC2DH	91h	00h	Compare/Capture channel 2 data high byte
CC2DL	92h	00h	Compare/Capture channel 2 data low byte
CC3DH	93h	00h	Compare/Capture channel 3 data high byte
CC3DL	94h	00h	Compare/Capture channel 3 data low byte
CC4DH	95h	00h	Compare/Capture channel 4 data high byte
CC4DL	96h	00h	Compare/Capture channel 4 data low byte
SCON	98h	00h	Serial port channel (UART) control register
SBUF	99h	XXh	Serial port channel (UART) data buffer
PCACH	9Ah	00h	PCA counter high byte
PCACL	9Bh	00h	PCA counter low byte
CC0DH	9Ch	00h	Compare/Capture channel 0 data high byte
CC0DL	9Dh	00h	Compare/Capture channel 0 data low byte
CC1DH	9Eh	00h	Compare/Capture channel 1 data high byte
CC1DL	9Fh	00h	Compare/Capture channel 1 data low byte
P2	A0h	FFh	Port 2
PCAC1	A1h	00h	PCA control register 1
PCAC2	A2h	00h	PCA control register 2
CC0CON	A3h	00h	Compare/Capture channel 0 control register
CC1CON	A4h	00h	Compare/Capture channel 1 control register
CC2CON	A5h	00h	Compare/Capture channel 2 control register
CC3CON	A6h	00h	Compare/Capture channel 3 control register
CC4CON	A7h	00h	Compare/Capture channel 4 control register
IE	A8h	00h	Interrupt Enable
IE1	A9h	00h	Interrupt Enable 1 register
P3	B0h	FFh	Port 3
IP	B8h	00h	Interrupt Priority
IP1	B9h	00h	Interrupt Priority 1 register
SCONF	BFh	00h	System control flag
T2CON	C8h	C0h	Timer 2 control register
T2MOD	C9h	00h	Timer 2 mode
RCAP2L	CAh	00h	Reload/Capture data low byte
RCAP2H	CBh	00h	Reload/Capture data high byte
TL2	CCh	FFh	Timer 2 low byte
TH2	CDh	FFh	Timer 2 high byte

Register	Location	Initial Value	Description
PSW	D0h	00h	Program Status Word register
P4	D8h	xFh	Port 4
ACC	E0h	00h	Accumulator
B	F0h	00h	B register
ISPFAH	F4h	00h	ISP address high byte
ISPFAL	F5h	00h	ISP address low byte
ISPFD	F6h	00h	ISP data register
ISPC	F7h	00h	ISP control register
KBLS	FDh	00h	EEI Level Selector Register
KBE	FEh	00h	EEI input Enable Register
KBF	FFh	00h	EEI Flag register

Functional Description

1 General Features

CRD89C51RA2 is an 8-bit micro-controller. All of its functions and the detailed meanings of the SFRs will be provided in the following sections.

1.1 Embedded Flash

The program can be loaded into the embedded 8K bytes Flash memory via an external writer, an ICP (In-Circuit Programming) device, or the ISP (In-System Programming) software.

The high-quality Flash is suitable for program reloading, data recording, or EEPROM functionality.

1.2 IO Pads

The IO pads are compatible to the 8052 series. P0 is open-drain in the input or output high condition, so an external pull-up resistor is required. P1 ~ P4 are designed with internal pull-up resistors. The IO pad structure is given below:

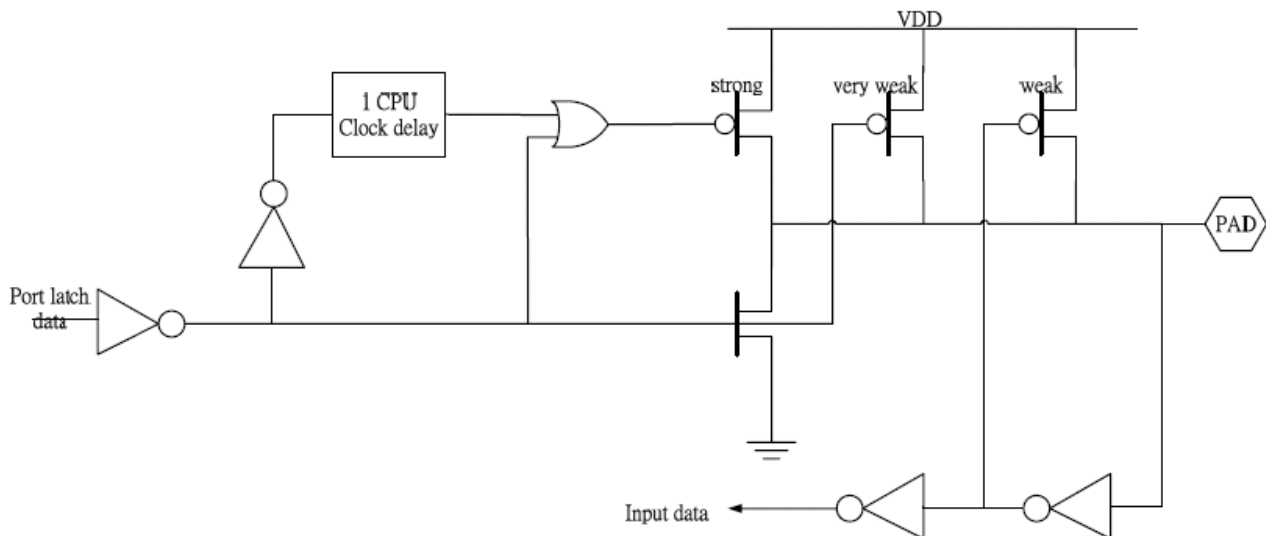


Fig. 1-1 : IO pad structure

All the pads for P0 ~ P4 are slew rate controlled to reduce EMI. Another way to reduce EMI is to disable the ALE output if unused. This is selected by its SFR.

In 3.3V applications, the IO pads are 5V tolerant except for XTAL1 and XTAL2.

1.3 12T/6T Selection

The conventional 8052 series MCUs are 12T, i.e., 12 oscillator clocks are needed for each machine cycle. If the machine cycle is changed to 6 clocks, then this 6T mode will double the running speed of 12T's with the same oscillator source. The choice of either 12T, or 6T, is configured in the information block. The figures below illustrate the difference between the 12T mode and the 6T mode.

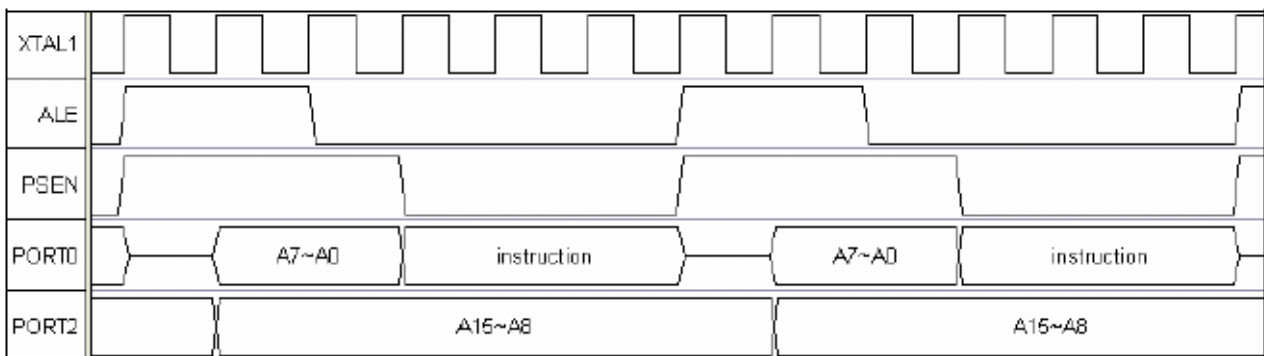


Fig 1-2(a) : The signal waveform of external program (EA=0) in 12T mode

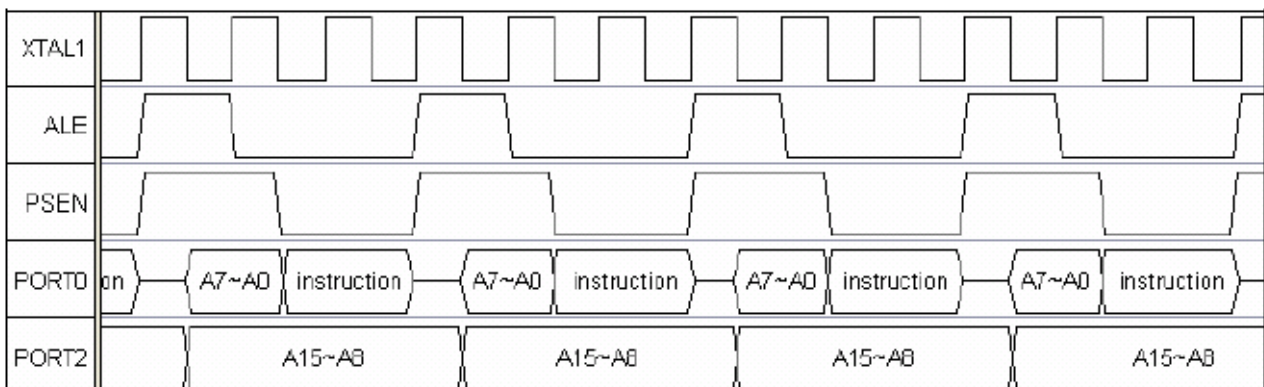


Fig 1-2(b) : The signal waveform of external program (EA=0) in 6T mode

The definition of "system clock", or "system frequency", as used in the sections to follow is:

6T: System clock frequency(F_{osc}) = crystal(F_{CRY}), or oscillator frequency

12T: System clock frequency(F_{osc}) = crystal(F_{CRY}), or oscillator frequency **divided by 2**

Take a 16MHz oscillator as an example, the system clock frequency is 16MHz in 6T. But in 12T mode, the system clock frequency is 8MHz.

2 Instruction set

The CRD89C51RA2 uses the powerful 80C51 instruction set. It consists of 49 single-byte, 42 two-byte and 15 three-byte instructions. Among them, 63 instructions are executed in 1 machine-cycle, 46 instructions in 2 machine-cycles and 2 instructions in 4 machine-cycles. A summary of the instruction set is given in Table 2-1. All of the instructions are fully compatible with standard 8052-series.

Table 2.1 Instruction Set

Mnemonic		Operation	Byte	Cycle
Arithmetic Instructions				
ADD	A, Rn	$A = A + Rn$	1	1
ADD	A, direct	$A = A + \text{direct}$	2	1
ADD	A, @Ri	$A = A + \langle @Ri \rangle$	1	1
ADD	A, #data	$A = A + \#data$	2	1
ADDC	A, Rn	$\bar{A} = A + Rn + C$	1	1
ADDC	A, direct	$\bar{A} = A + \text{direct} + C$	1	1
ADDC	A, @Ri	$\bar{A} = A + \langle @Ri \rangle + C$	1	1
ADDC	A, #data	$\bar{A} = A + \#data + C$	1	1
SUBB	A, Rn	$A = A - Rn - C$	1	1
SUBB	A, direct	$\bar{A} = A - \text{direct} - C$	2	1
SUBB	A, @Ri	$A = A - \langle @Ri \rangle - C$	1	1
SUBB	A, #data	$A = A - \#data - C$	2	1
INC	A	$\bar{A} = A + 1$	1	1
INC	Rn	$Rn = Rn + 1$	1	1
INC	direct	$\text{direct} = \text{direct} + 1$	2	1
INC	@Ri	$\langle @Ri \rangle = \langle @Ri \rangle + 1$	1	1
DEC	A	$\bar{A} = A - 1$	1	1
DEC	Rn	$Rn = Rn - 1$	1	1
DEC	direct	$\text{direct} = \text{direct} - 1$	2	1
DEC	@Ri	$\langle @Ri \rangle = \langle @Ri \rangle - 1$	1	1
INC	DPTR	$DPTR = DPTR + 1$	1	2
MUL	AB	$B:A = A * B$	1	4
DIV	AB	$A = \text{INT} (A/B)$ $B = \text{MOD} (A/B)$	1	4
DA	A	Decimal adjust ACC	1	1

Table 2.1 Instruction Set (continued)

Mnemonic		Operation	Byte	Cycle
Logical Instructions				
ANL	A, Rn	A.AND.Rn	1	1
ANL	A, direct	A.AND.direct	2	1
ANL	A, @Ri	A.AND.<@Ri>	1	1
ANL	A, #data	A.AND.#data	2	1
ANL	direct, A	direct.AND.A	2	1
ANL	direct, #data	direct.AND.#data	3	2
ORL	A, Rn	A.OR.Rn	2	1
ORL	A, direct	A.OR.direct	2	1
ORL	A, @Ri	A.OR.<@Ri>	1	1
ORL	A, #data	A.OR.#data	2	1
ORL	direct, A	direct.OR.A	2	1
ORL	direct, #data	direct.OR.#data	3	2
XRL	A, Rn	A.XOR.Rn	1	1
XRL	A, direct	A.XOR.direct	2	1
XRL	A, @Ri	A.XOR.<@Ri>	1	1
XRL	A, #data	A.XOR.#data	2	1
XRL	direct, A	direct.XOR.A	2	1
XRL	direct, #data	direct.XOR.#data	3	2
CLR	A	A = 0	1	1
CPL	A	A = /A	1	1
RL	A	Rotate ACC Left 1 bit	1	1
RLC	A	Rotate Left through Carry	1	1
RR	A	Rotate ACC Right 1 bit	1	1
RRC	A	Rotate Right through Carry	1	1
SWAP	A	Swap Nibbles in A	1	1
Data Transfers Instructions				
MOV	A, Rn	A = Rn	1	1
MOV	A, direct	A = direct	2	1
MOV	A, @Ri	A = <@Ri>	1	1
MOV	A, #data	A = #data	2	1
MOV	Rn, A	Rn = A	1	1
MOV	Rn, direct	Rn = direct	2	2

Table 2.1 Instruction Set (continued)

Mnemonic	Operation	Byte	Cycle	Mnemonic
MOV	Rn, #data	Rn = #data	2	1
MOV	direct, A	direct = A	2	1
MOV	direct, Rn	direct = Rn	2	2
MOV	direct, direct	direct = direct	3	2
MOV	direct, @Ri	direct = <@Ri>	2	2
MOV	direct, #data	direct = #data	2	1
MOV	@Ri, A	<@Ri> = A	1	1
MOV	@Ri, direct	<@Ri> = direct	2	2
MOV	@Ri, #data	<@Ri> = #data	2	1
MOV	DPTR, #data16	DPTR = #data16	3	2
MOVC	A, @A+DPTR	A = code memory[A+DPTR]	1	2
MOVC	A, @A+PC	A = code memory[A+PC]	1	2
MOVX	A, @Ri	A = external memory[Ri] (8-bits address)	1	2
MOVX	A, @DPTR	A = external memory[DPTR] (16-bits address)	1	2
MOVX	@Ri, A	external memory[Ri] = A (8-bits address)	1	2
MOVX	@DPTR, A	external memory[DPTR] = A (16-bits address)	1	2
PUSH		INC SP: MOV "@SP", <direct>	2	2
POP		MOV <direct>, "@SP": DEC SP	2	2
XCH	A, Rn	ACC and <Rn> exchange data	1	1
XCH	A, direct	ACC and <direct> exchange data	2	1
XCH	A, @Ri	ACC and <@Ri> exchange data	1	1
XCHD	A, @Ri	ACC and <@Ri> exchange low nibbles	1	1
Boolean Instructions				
CLR	C	C = 0	1	1
CLR	bit	bit = 0	2	1

Table 2.1 Instruction Set (continued)

Mnemonic	Operation	Byte	Cycle	Mnemonic
SETB	C	C = 1	1	1
SETB	bit	bit = 1	2	1
CPL	C	C = /C	1	1
CPL	bit	bit = /bit	2	1
ANL	C,bit	C = C.AND.bit	2	2
ANL	C,/bit	C = C.AND./bit	2	2
ORL	C,bit	C = C.OR.bit	2	2
ORL	C,/bit	C = C.OR./bit	2	2
MOV	C,bit	C = bit	2	1
MOV	bit,C	bit = C	2	2
JC	rel	Jump if C=1	2	2
JNC	rel	Jump if C=0	2	2
JB	bit,rel	Jump if bit=1	3	2
JNB	bit,rel	Jump if bit=0	3	2
JBC	bit,rel	Jump if bit=1 and clear the bit	3	2
Jump Instructions				
ACALL	addr11	Call Subroutine only at 2k bytes Address	2	2
LCALL	addr16	Call Subroutine in max 64K bytes Address	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Jump only at 2k bytes Address	2	2
LJMP	addr16	Jump to max 64K bytes Address	3	2
SJMP	rel	Jump on at 256 bytes	2	2
JMP	@A+DPTR	Jump to A+DPTR	1	2
JZ	rel	Jump on at 256 bytes if A = 0	2	2
JNZ	rel	Jump on at 256 bytes if A <> 0	2	2
CJNE	A, direct,rel	Jump on at 256 bytes if A <> <direct>	3	2

Table 2.1 Instruction Set (continued)

Mnemonic	Operation	Byte	Cycle	Mnemonic
CJNE	A, #data, rel	Jump on at 256 bytes if A <> <#data>	3	2
CJNE	Rn, #data, rel	Jump on at 256 bytes if Rn <> <#data>	3	2
CJNE	@Ri, #data, rel	Jump on at 256 bytes if <@Ri> <> <#data>	3	2
DJNZ	Rn, rel	Decrement and jump if Rn not zero	2	2
DJNZ	direct, rel	Decrement and jump if direct not zero	3	2
NOP		No Operation	1	1

3 Memory Structure

The CRD89C51RA2 manipulates operands in three memory spaces. They are (1) 256 bytes standard RAM, (2) 768 bytes auxiliary RAM and (3) 8K bytes embedded Flash as program memory.

3.1 Program Memory

As described in Section 1, the CRD89C51RA2 has 8K bytes on-chip Flash memory which is used as general program memory, the address range for the 8K bytes is 0000h to 1FFFh. Its features are:

- READ: byte-wise
- WRITE: byte-wise in 30µs (previously erased by a chip erase).
- ERASE: Full Erase (8+4K bytes) in 200 ms. Erased bytes contain FFh.
- Endurance : 100K erase and write cycles each byte at TA=25°C.
- Retention : 10 years

If ISP or IAP is required, there are up to 4K bytes of specific ISP service program area, available. The address range is 3000h to 3FFFh. The ISP service program size can be partitioned as N blocks of 512 bytes each (N=0 to 8). When N=0, there will be no ISP service program space available, the total 8K + 4K bytes memory are used as program memory. When N=1, the Flash from 3E00h to 3FFFh is reserved for ISP service program. When N=2, the Flash from 3C00h to 3FFFh is reserved for ISP service program, etc. Value N is set by the external programmer in the information block during programming of the ISP code. Fig 3.1 illustrates the ISP Flash reservation with different values of N.

Any unused Flash from the 4K bytes ISP service Program area can be used as EEPROM memory space for general, or program use.

When programmed with an external writer, code in the CRD89C51RA2 can be protected against unauthorised reading. If protection is activated, users can't read the program from the writer. Also, when the protect bit is set, the hardware will disable any MOVX instructions attempting to read the internal program from within a program running in external program mode (EA = 0). The only way to reset the protection bit is to erase the entire Flash.

3.2 Data Memory

The CRD89C51RA2 has 256 + 768 bytes on-chip RAM, the 256 bytes are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method, via MOVX instructions.

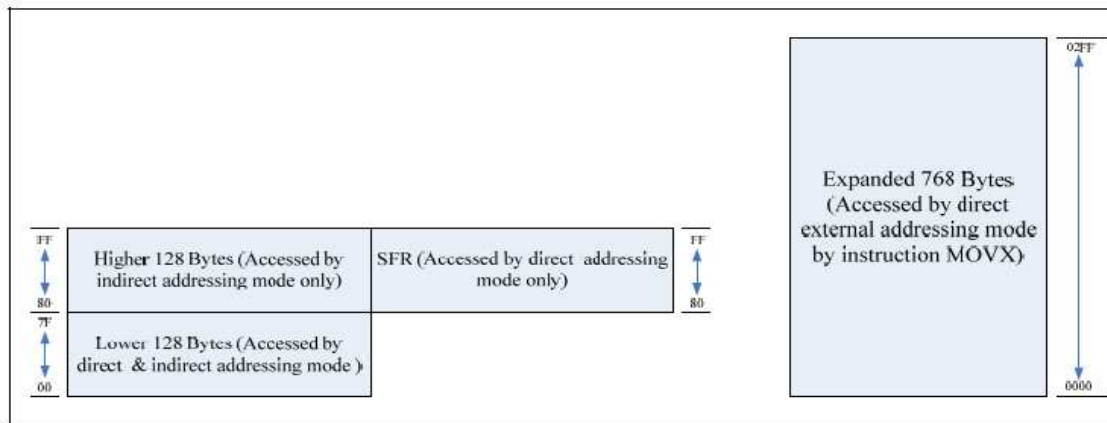


Fig. 3-2 : RAM architecture

3.2.1 Data Memory - Lower 128 byte (\$00h to \$7Fh)

Data Memory 00h to FFh is the same as defined in 8052. Addresses 00h to 7Fh can be accessed via both direct and indirect addressing modes. Addresses 00h to 1Fh are allocated to register pages. Addresses 20h to 2Fh are allocated to memory bit variables, and 30h to 7Fh are available for general memory/stack use.

3.2.2 Data Memory - Higher 128 byte (\$80h to \$FFh)

Addresses 80h to FFh can only be accessed via indirect addressing mode. It is data area.

3.2.3 Data Memory - Expanded 768 bytes (\$0000h to \$02FFh)

The on-chip expanded RAM area, a total of 768 bytes, can be found at addresses 0000h to 02FFh is. This area can be accessed via external direct addressing mode with MOVX instructions.

If the address of instruction MOVX @DPTR is larger than 02FFh, then the CRD89C51RA2 will generate the external memory control signal automatically. Bit 1 (OME) of SFR BFh (SCONF) can be used to enable or disable the expanded 768 bytes of RAM. The default setting of OME bit is 0 (disabled).

4 CPU Engine.

The CRD89C51RA2 CPU engine allows fetching instructions from the program memory, and accessing data from RAM or SFR. A description of the CPU engine SFRs follows.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET	
8051 Core												
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h	
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h	
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	F1	P	00h	
SP	Stack Pointer	81h	SP[7:0]									07h
DPL	Data pointer low 0	82h	DPL[7:0]									00h
DPH	Data pointer high 0	83h	DPH[7:0]									00h
DPL1	Data pointer low 1	84h	DPL1[7:0]									00h
DPH1	Data pointer high 1	85h	DPH1[7:0]									00h
DPS	Data pointer select	86h	-	-	-	-	-	-	-	DPS.0		
SCONF	System control flag	BFh	-	-	-	-	-	ISPE	OME	ALEI	00h	

4.1 Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to hold the operand.

Mnemonic: ACC								Address: E0h	
7	6	5	4	3	2	1	0	Reset	
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h	

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2 B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to hold temporary data.

Mnemonic: B								Address: F0h	
7	6	5	4	3	2	1	0	Reset	
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h	

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3 Program Status Word

Mnemonic: PSW							Address: D0h	
7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS[1:0]		OV	F1	P	00h

CY: Carry flag.

AC: Auxiliary Carry flag for BCD operations.

F0: General purpose Flag 0 available for user.

RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.

F1: General purpose Flag 1 available for user.

P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, that is, even parity.

4.4 Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 08h.

Mnemonic: SP							Address: 81h	
7	6	5	4	3	2	1	0	Reset
SP[7:0]								07h

SP[7:0]: The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5 Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2 byte register (MOV DPTR, #data16) or as two registers (for example MOV DPL,#data8). It is generally used to access external code or data space (eg. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Mnemonic: DPL							Address: 82h	
7	6	5	4	3	2	1	0	Reset
DPL[7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH							Address: 83h	
7	6	5	4	3	2	1	0	Reset
DPH[7:0]								00h

DPH[7:0]: Data pointer High 0

4.6 Data Pointer 1

The use of the second data pointer may accelerate the manipulation of data blocks. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the CRD89C51RA2, the standard data pointer is called DPTR0, while the second data pointer is called DPTR1. The data pointer select bit selects the active pointer. The data pointer select bit is located in bit 0 of the DPS register (DPS.0). The user switches between pointers by toggling this bit. All DPTR-related instructions use the currently selected DPTR.

Mnemonic: DPL1							Address: 84h	
7	6	5	4	3	2	1	0	Reset
DPL1[7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1							Address: 85h	
7	6	5	4	3	2	1	0	Reset
DPH1[7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: DPS							Address: 86h	
7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	-	DPS.0	00h

4.7 System control flags

Mnemonic: SCONF

Address: BFh

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	ISPE	OME	ALEI	00h

ISPE: ISP function enable bit.
ISPE = 1 enables the ISP function.
ISPE = 0 disables the ISP function.

OME: 768 bytes on-chip RAM enable bit.
OME = 1 enables the 768 bytes on-chip RAM.
OME = 0 disables the 768 bytes on-chip RAM.

ALEI: ALE output disable.
ALEI = 1 disables the ALE output.
ALEI = 0 enables the ALE output.

5 Port 0 – Port 4

Port 0 ~ Port 4 are the general purpose I/O ports of the controller. Port 4[3:0] is available at the 44-pin PLCC and QFP packages only. Most of the port pins have multiplexed functions assigned to them. For example, Port 3[0] is also used as RXD in the UART application. Port0 pins are open-drained in the input and output high conditions, so external pull-up resistors are required. Internal pull up resistors are provided to all other ports.

For general purpose applications, all pins can be individually assigned to either high or low as their SFRs are bit addressable.

Mnemonic: P0							Address: 80h	
7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

P0.7~ 0: Port0[7] ~ Port0[0]

Mnemonic: P1							Address: 90h	
7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh

P1.7~ 0: Port1[7] ~ Port1[0]

Mnemonic: P2							Address: A0h	
7	6	5	4	3	2	1	0	Reset
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh

P2.7~ 0: Port2[7] ~ Port2[0]

Mnemonic: P3							Address: B0h	
7	6	5	4	3	2	1	0	Reset
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh

P3.7~ 0: Port3[7] ~ Port3[0]

Mnemonic: P4					Address: D8h			
7	6	5	4	3	2	1	0	Reset
x	x	x	x	P4.3	P4.2	P4.1	P4.0	xFh

P4.3~ 0: Port4[3] ~ Port4[0]

6 Timer 0 and Timer 1

These timer and counter functions are presented in the same module. The “timer” or “counter” function is selected by the control bits C/T in SFR TMOD. Timer 0 and Timer 1 have four operation modes, which are selected by bit-pairs (M1, M0) in SFR TMOD. Mode 0, 1, and 2 are the same for both timer and counters. Mode 3 is different. The four operating modes are described below:

6.1 Mode 0

In this mode, the timer register is configured as a 13-bit register. Take Timer 1 for example. As the counter rolls over from all 1s to all 0s, it sets the Timer 1 interrupt flag TF1. The counter input is enabled when TR1 = 1 and either GATE = 0, or INT1 = 1. Setting GATE = 1 allows the timer to be controlled by the external input INT1. This facilitates pulse width measurements. Bit TR1 is located in TCON and GATE is located in TMOD.

The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the register contents.

Mode 0 operation is the same for both Timer 0 and Timer 1. Substituting TR0, TF0 and INT0 for the corresponding Timer 1 signals in the above description, leads us to the explanation of the operation of Mode 0 for Timer 0. Note that there are two separate GATE bits available in TMOD. One is for Timer 1 (TMOD.7) and the other is for Timer 0 (TMOD.3).

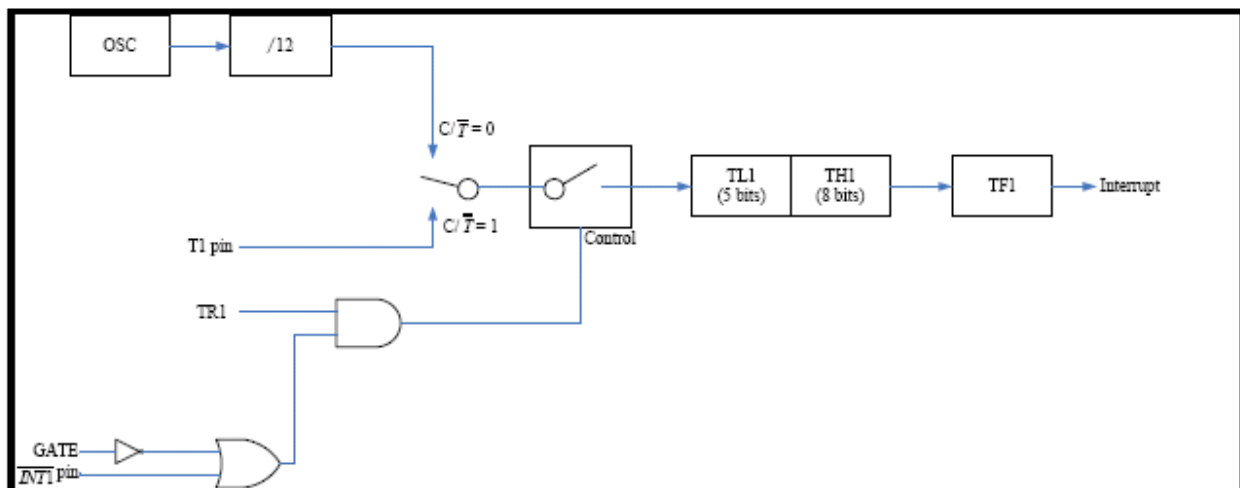


Fig. 6-1 : Mode 0 operation for Timer 1

6.2 Mode 1

Mode 1 is the same as Mode 0, except that the timer register runs with all 16 bits.

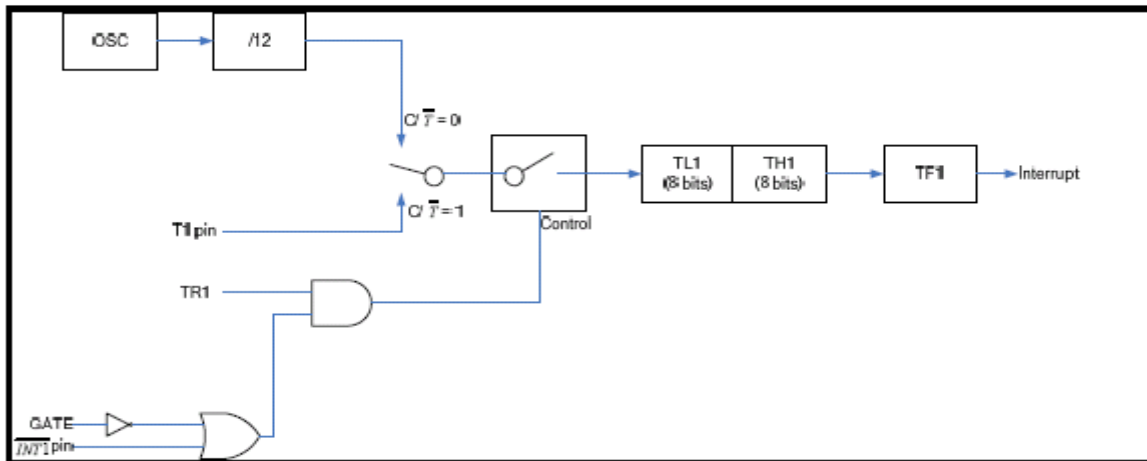


Fig. 6-2 : Mode 1 operation for Timer 1

6.3 Mode 2

For Timer 1, Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reload. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload operation leaves TH1 unchanged. Timer 0 Mode 2 operation is the same.

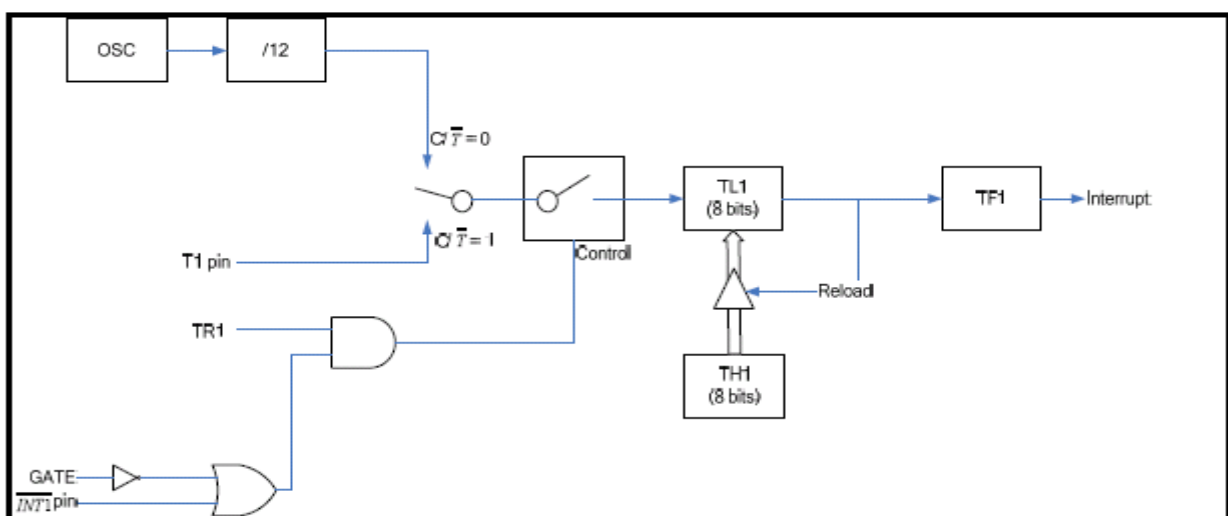


Fig. 6-3 : Mode 2 operation for Timer 1

6.4 Mode 3

Timer 1 in Mode 3 acts as a simple counter. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 considers TL0 and TH0 as two separate counters. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function to count machine cycles and takes over the use of TR1 and TF1 from Timer 1. In this mode, TH0 controls the trigger of "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. Alternatively, it can be used by the serial port as a baud rate generator, or by any application not requiring an interrupt.

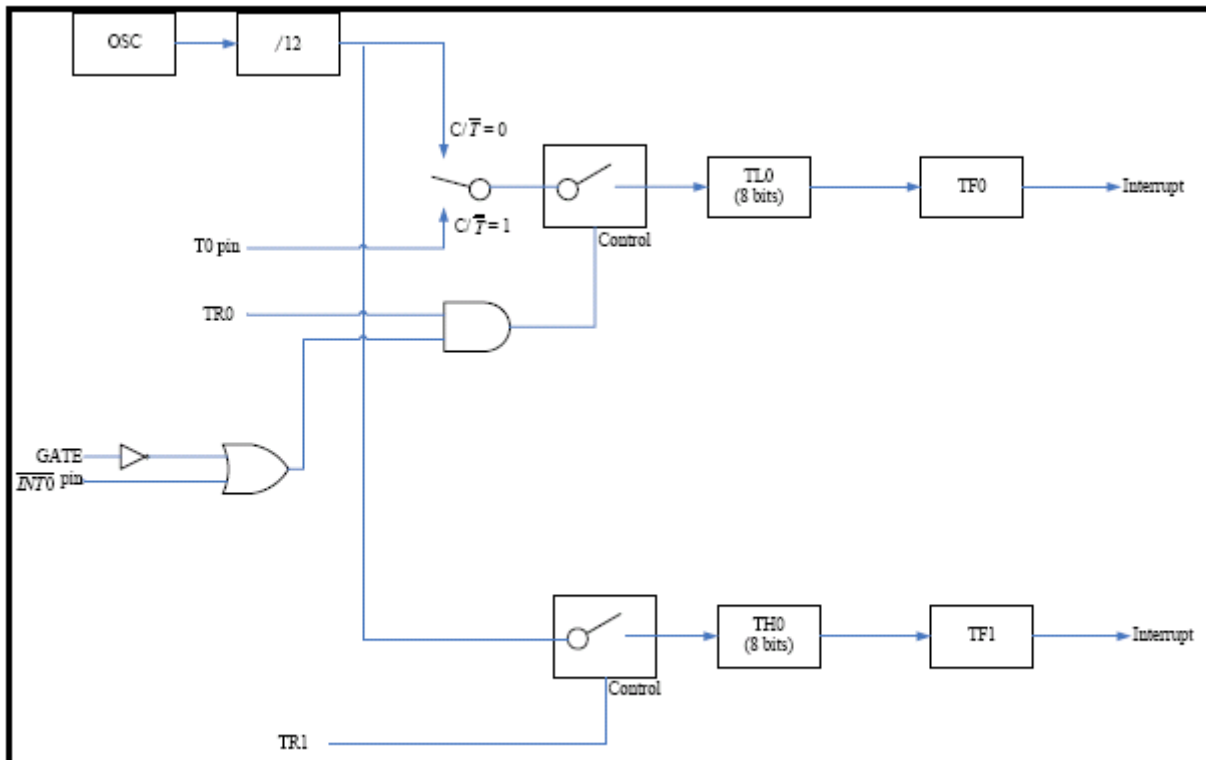


Fig. 6-4 : Mode 3 operation for Timer 0

6.5 Timer/counter SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00h
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00h
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00h
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00h
TMOD	Timer Mode Control	89h	GATE	C/\bar{T}	M1	M0	GATE	C/\bar{T}	M1	M0	00h
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

6.5.1 Timer/Counter Mode Control register (TMOD)

Mnemonic: TMOD							Address: 89h		
7	6	5	4	3	2	1	0	Reset	
GATE	C/\bar{T}	M1	M0	GATE	C/\bar{T}	M1	M0	00h	
Timer 1				Timer 0					

GATE: If set, the external gate control is enabled (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented at each falling edge on T0 or T1 input pins.

C/T: Selects Timer or Counter operation. When set to 1, a Counter operation is performed. When cleared to 0, the corresponding register will function as a Timer.

M[1:0]: Selects mode for Timer/Counter 0 or Timer/Counter 1.

M1	M0	Mode	Function
0	0	Mode0	13-bit Counter/Timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit Counter/Timer.
1	0	Mode2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit Timers / Counters.

6.5.2 Timer/Counter Control register (TCON)

Mnemonic: TCON							Address: 88h	
7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.

IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

7 Timer 2

Timer 2 is a 16-bit timer/counter which can operate either as a timer or an event counter. This is selectable by bit C/T2 in the SFR T2CON. It has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON as shown below.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the timer function, the TL2 register is incremented every machine cycle, thus one can think of it as counting machine cycles. Since a machine cycle consists of a 12-clock period in 12T, the count rate is 1/12 of the oscillator clock frequency. In 6T, it is 1/6.

In the counter function, the register is incremented in response to every 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 clock periods in 12T) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency in 12T mode or 1/12 in 6T mode. To ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Table 7-1 : Timer 2 Operating Modes

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate Generator
X	X	0	Off

7.1 Capture mode

In the capture mode, there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt.

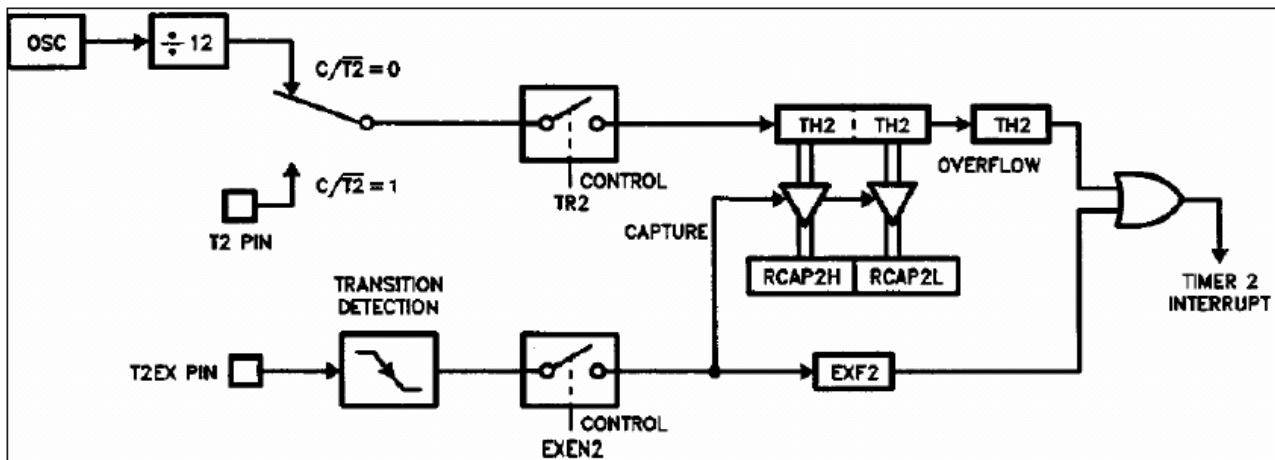


Figure 7-1 : Timer 2 in capture mode

7.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by bit DCEN (Down Counter Enable) located in T2MOD. Upon reset, the DCEN bit is set to 0 so that Timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 7-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to FFFFh and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. If enabled, both the TF2 and EXF2 bits can generate an interrupt.

Setting the DCEN bit enables Timer 2 to count up, or down, as shown in Figure 7-3. In this mode, pin T2EX controls the direction of count. A logic 1 at T2EX forces Timer 2 to count up. The timer will overflow at FFFFh and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 are equal to the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes FFFFh to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows. If needed, this bit can be considered to act as the 17th bit of the counter. In this operating mode, EXF2 does not flag an interrupt.

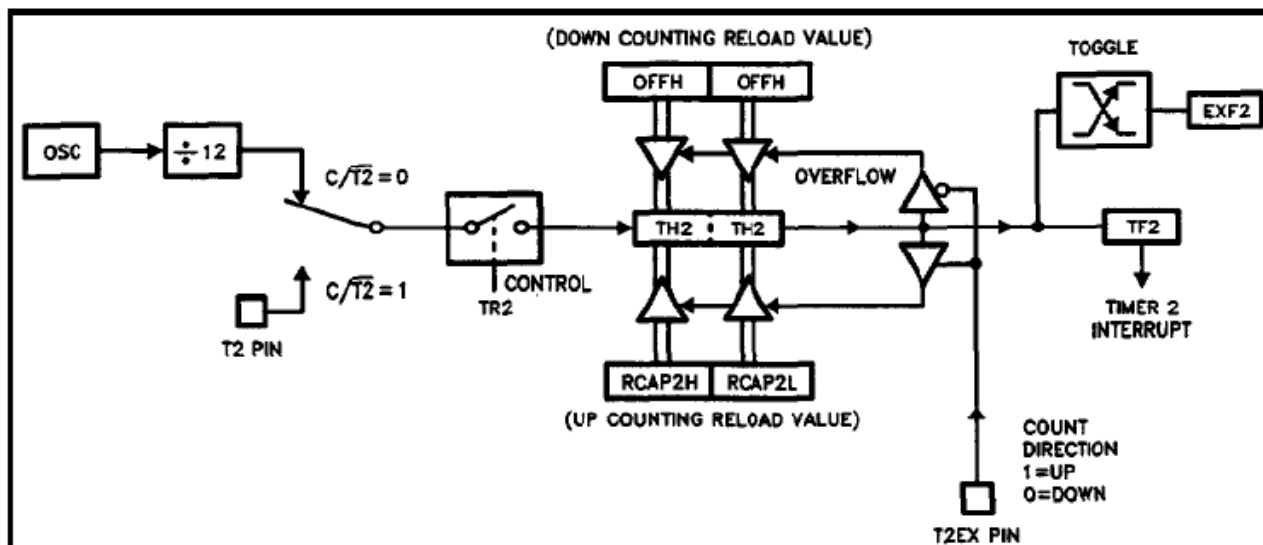


Figure 7-3 : Timer 2 in auto reload mode (DCEN=1)

7.3 Programmable clock out

Apart from being a regular I/O pin, P1.0 may also be assigned to two alternate functions. It can be set to be the input of the external clock of Timer/Counter 2, or the output of a clock with 50% duty cycle. In 12T mode and with a 16MHz oscillator frequency, the output may vary from 61Hz to 4MHz.

To configure Timer/Counter 2 as a clock generator, bit C/T2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as follows:

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 * (65536 - \text{RCAP2H, RCAP2L})}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies can not be determined independently from one another since they both use RCAP2H and RCAP2L.

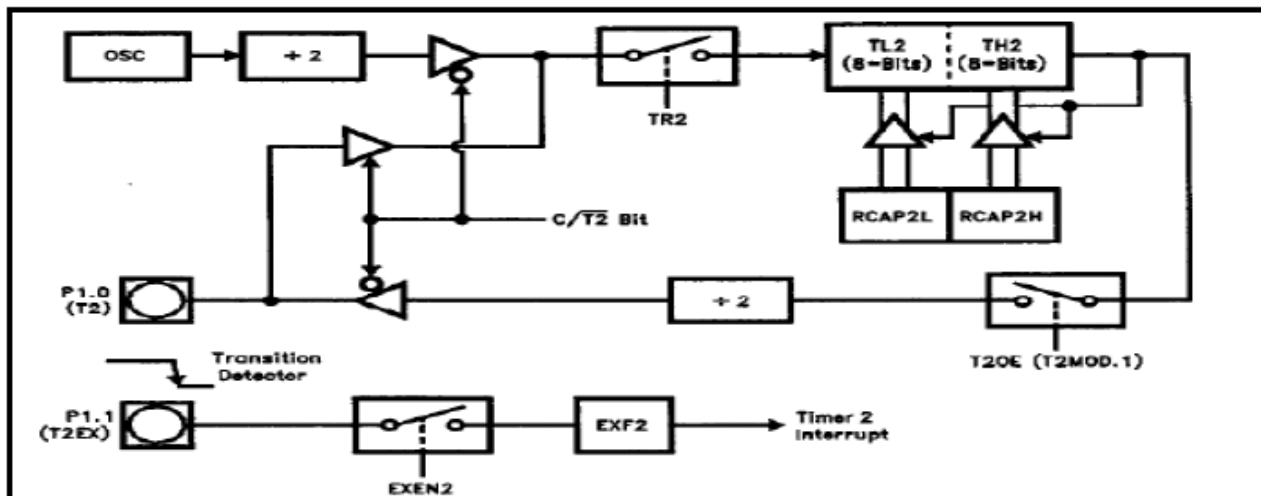


Figure 7-4 : Timer 2 in clock-out mode

7.4 Timer 2 SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RES ET
Timer 0 and 1											
TL2	Timer 2 , low byte	CCh	TL2[7:0]								00h
TH2	Timer 2 , high byte	CDh	TH2[7:0]								00h
RCAP2L	Reload and capture data low byte	CAh	RCAP2L[7:0]								00h
RCAP2H	Reload and capture data high byte	CBh	RCAP2H[7:0]								00h
T2MOD	Timer 2 mode	C9h	-	-	-	-	-	-	T2OE	DCEN	x0h
T2CON	Timer 2 control register	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$	00h

Mnemonic: T2CON

Address: C8h

7	6	5	4	3	2	1	0	Reset
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$	00h

TF2: Timer 2 overflow flag is set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.

EXF2: Timer 2 external flag is set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt service routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).

RCLK: Receive clock enable. When set, causes the serial port to use Timer 2

overflow pluses as its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used as the receive clock.

TCLK: Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses as its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used as the transmit clock.

EXEN2: Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.

TR2: Start/Stop control for Timer 2. TR2 = 1 starts the timer.

C/T2: Timer or counter select for Timer 2. C/T2 = 0 for timer function. C/T2 = 1 for external event counter (falling edge triggered).

CP/RL2: Capture/Reload select. CP/RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/RL2 = 0 causes automatic reloads to occur when Timer 2 overflows, or negative transitions occur at T2EX, when EXEN2 = 1. When either RCLK, or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Mnemonic: T2MOD						Address: C9h		
7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	T2OE	DCEN	x0h

T2OE: Timer 2 Output Enable bit.

DCEN: When set, this bit allows Timer 2 to be configured as an up/down counter.

8 Watchdog timer

The watchdog timer is an 8-bit counter that is incremented once every WDTCLK clock cycle. After a device reset is initiated by a stimulus from either the external reset pin, or the the watchdog timer, the watchdog timer is disabled and all its associated registers are cleared to zero. When the reset sequence is complete, the CRD89C51RA2 reads bit WDTE. If set, the watchdog timer function will be enabled. Bits WDTM[2:0] determine the timer overflow period.

Table 8-1 Watchdog Timer Overflow Period :

WDTM[2:0]	000	001	010	011	100	101	110	111
OverFlow Period	1.58ms	3.15ms	6.30ms	12.60ms	25.12ms	50.41ms	100.82ms	201.65ms

Both WDTE and WDTM are set by the user, through the external writer, during the initial loading of the application software.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Watchdog Timer											
WDTC	Watchdog timer control register	8Eh	WDTE	-	CLEAR	-	-	WDTM2	WDTM1	WDTM0	00H
WDTK	Watchdog timer refresh key	8Fh	WDTK[7:0]								00H

The watchdog timer will reset the system if the CLEAR bit of WDTC register is not set before the timer overflows. Once the watchdog is started it cannot be stopped. If WDTE allows it, WDT is enabled by setting 1 to WDTE, bit 7 of WDTC. The WDTE bit will be cleared to 0 automatically when the CRD89C51RA2 has been reset, either through hardware, or WDT.

Resetting the WDT is done by setting 1 to CLEAR, bit 5 of WDTC, before the counter overflows. This will clear the content of the counter and let it re-start. In order to set the CLEAR bit, the user must first load register WDTK with the value 1Eh, followed immediately with the value E1h.

Mnemonic: WDTC

Address: 8Eh

7	6	5	4	3	2	1	0	Reset
WDTE	-	CLEAR	-	-	WDTM2	WDTM1	WDTM0	00H

WDTM[2:0]: Watchdog timer over flow period setting.

WDTE: Watchdog timer Enable.

WDTE=0: Disable the WDT function (if WDTE was set from the external writer)

WDTE=1: Enable the WDT function (if WDTE was set from the external writer)

This bit will be cleared to 0 automatically when MCU been reset, either hardware reset, or WDT reset.

CLEAR: Setting this bit will clear and restart the Watchdog timer counter.

Mnemonic: WDTK

Address: 8Fh

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.

A programmer must set it to 1Eh first, then E1h next. After these, CLEAR may be set and the watchdog reset.

9 ISP (In-System Programming)

A user may update the application software found in the CRD89C51RA2 if an ISP service code is preloaded in the ISP code area as shown in Table 9-1. One page of Flash memory is 512bytes.

Table 9-1 : ISP code area

Lock-bit number	ISP code area
1	512 bytes (from \$3E00h to \$3FFF)
2	1K bytes (from \$3C00h to \$3FFF)
3	1.5K bytes (from \$3A00h to \$3FFF)
4	2K bytes (from \$3800h to \$3FFF)
5	2.5K bytes (from \$3600h to \$3FFF)
6	3K bytes (from \$3400h to \$3FFF)
7	3.5K bytes (from \$3200h to \$3FFF)
8	4K bytes (from \$3000h to \$3FFF)

There are three ways to invoke the code located at the ISP code area. These are:

- (1) Address 0000h is loaded with FFh. After reset, the controller identifies the blank byte and jumps at the beginning of the ISP code.
- (2) The application program executes an "LJMP" instruction to the beginning of the ISP code.
- (3) The hardware invokes the ISP code if, after power on reset, either P2.6 and P2.7 are both low, or Port4.3 is low.

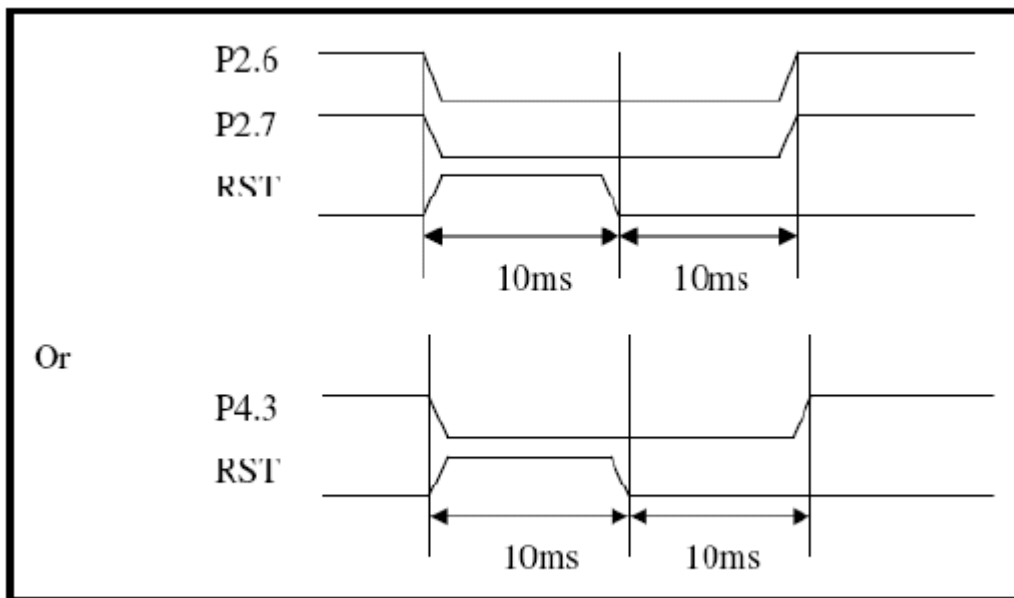


Fig 9-1 : ISP entering by hardware setting

9.1 ISP SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
ISP											
ISPC	ISP control register	F7h	START	-	-	-	-	-	ISPF1	ISPF0	00h
ISPF AH	ISP Flash address high byte	F4h	ISPFA[15:8]								00h
ISPF AL	ISP Flash address low byte	F5h	ISPFA[7:0]								00h
ISPF D	ISP Flash data	F6h	ISPF D[7:0]								00h

Mnemonic: ISPF AH			Address: F4h					
7	6	5	4	3	2	1	0	Reset
ISPFA[15:8]								00h

Mnemonic: ISPF AL			Address: F5h					
7	6	5	4	3	2	1	0	Reset
ISPFA[7:0]								00h

ISPFA[15:0]: The ISPF AH and ISPF AL provide the 16-bit Flash memory address for the ISP function. The Flash memory address should not include any part of the ISP service program space address. If the Flash memory address indicated by ISPF AH and ISPF AL registers overlaps with the ISP service program space, the Flash write and page erase functions will be ignored.

Mnemonic: ISPF D			Address: F6h					
7	6	5	4	3	2	1	0	Reset
ISPF D[7:0]								00h

Mnemonic: ISPC			Address: F7h					
7	6	5	4	3	2	1	0	Reset
START	-	-	-	-	-	ISPF[1:0]		00h

ISPF[1:0]	ISP function
00	Byte program
01	Chip Protect
10	Page erase(512 Bytes)
11	Chip erase

ISPFD[7:0]: The ISPF D contains the 8-bits data to be written.

ISPF[1:0]: ISP function select (see table above).

START: ISP START bit.

START = 1 : Start ISP function as indicated by ISPF[1:0].

START = 0 : no operation.

In order to activate the ISP mechanism, the application software must first load the ISPF D register with values 55h, AAh and 55h in that sequence:

```
MOV ISPF D,#055h
MOV ISPF D,#0AAh
MOV ISPF D,#055h
```

Any attempt to set the START bit will be disregarded, unless preceded by the above sequence. Following the setting of START to 1, the CRD89C51RA2 hardware circuit latches the address and data bus and freezes the program counter until the ISP function is finished and the START bit reset to 0 by the hardware. The application does not need to monitor the status of the START bit.

To perform the byte program, or page erase, ISP function, the user needs to first specify the Flash address concerned. When performing the page erase function, the CRD89C51RA2 will erase the entire page indicated by the Flash address in the ISPF AH register located within the page.

To perform the chip erase ISP function, the CRD89C51RA2 will erase all the Flash program memory and data Flash memory except the ISP program space. Also, the CRD89C51RA2 will unprotect the Flash memory automatically if it has been protected by clearing the information block bit LOCK to 0. Note that if LOCK is 0, all the Flash memory contents will be read as zeros.

The following example shows how to use the ISP facility in order to write data 22h to address 1005h.

```
MOV ISPF D, #055h
MOV ISPF D, #0AAh
MOV ISPF D, #055h ; ISP function may now be enabled
MOV SCONE, #04h ; enable ISP function
MOV ISPF AH, #10h ; Set Flash address high byte
MOV ISPF AL, #05h ; Set Flash address low byte
MOV ISPF D, #22h ; Set Flash data to be programmed
MOV ISPF C, #80h ; Start programming 22h to the Flash address 1005h
; After programming is complete, START is reset
; and PC then points to the next instruction.
```

10 Serial interface (UART)

The UART serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port's receive and transmit registers are both accessed through SFR SBUF. SBUF is made up of two separate registers, a transmit buffer and a receive buffer. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in the following 4 modes:

Mode 0: Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received with LSB first. The baud rate is fixed at 1/6 the system frequency as defined in Section 1.

Mode 1: 10 bits are transmitted through TXD and received through RXD with a start bit (=0), then the 8 data bits with LSB first, finally a stop bit (=1). On the receiving side, the stop bit is stored in RB8 in SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted through TXD and received through RXD with a start bit (=0), then the 8 data bits with LSB first, then a programmable 9th data bit, finally a stop bit (=1). On the transmitting side, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, or, for example, the parity bit (P in the PSW) could be moved into TB8. On the receiving side, the 9th data bit is stored in RB8 in SCON. The baud rate is programmable to either 1/32, or 1/16, of the system frequency.

Mode 3: 11 bits are transmitted through TXD and received through RXD with a start bit (=0), then the 8 data bits with LSB first, then a programmable 9th data bit, finally a stop bit (=1). Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that loads SBUF. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in other modes by the incoming start bit if REN = 1.

10.1 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit is stored in RB8. Then comes a stop bit. The port can be setup so that if RB8 = 1, when the stop bit is received, the serial port interrupt will be serviced. This feature is enabled by setting bit SM2 in SCON. This feature is used in multiprocessor systems as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data

byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be transmitted. The slave that weren't being addressed leave their SM2s set and go on their business, ignoring the transmitted data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

10.2 Baud rates

The baud rate in Mode 0 is fixed:

$$\text{Mode 0} \quad \text{Baud Rate} = \frac{\text{System Frequency}}{6}$$

The baud rate in mode 2 depends on the value of bit SMOD in SFR PCON. If SMOD = 0 (which is the value on reset), the baud rate is 1/32 the system frequency. If SMOD = 1, the baud rate is 1/16 the system frequency.

$$\text{Mode 2} \quad \text{Baud Rate} = \frac{2^{\text{SMOD}}}{32} * (\text{System Frequency})$$

10.3 Using Timer 1 to Generate Baud Rates.

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Modes 1 \& 3} \quad \text{Baud Rate} = \frac{2^{\text{SMOD}}}{32} * (\text{Timer 1 overflow rate})$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case, the baud rate is given by the formula

$$\text{Modes 1 \& 3} \quad \text{Baud Rate} = \frac{2^{\text{SMOD}}}{32} * \frac{\text{System Frequency}}{6 * [256 - \text{TH1}]}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

10.4 Using Timer 2 to Generate Baud Rates.

In the CRD89C51RA2, Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Note that the baud rates for transmit and receive can be different.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1,3: Baud Rate} = \frac{\text{Timer 2 overflow rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In most applications, it is configured as timer (C/T2 = 0). "Timer" operation is slightly different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer, it would increment every machine cycle (once every 12 oscillator cycles in 12T, and 6 cycles in 6T). In baud rate generation however, it follows the system frequency. The baud rate is given by the formula:

$$\text{Modes 1,3: Baud Rate} = \frac{\text{System Frequency}}{16 * [65536 - (RCAP2H, RCAP2L)]}$$

Where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L considered as a 16-bit unsigned integer.

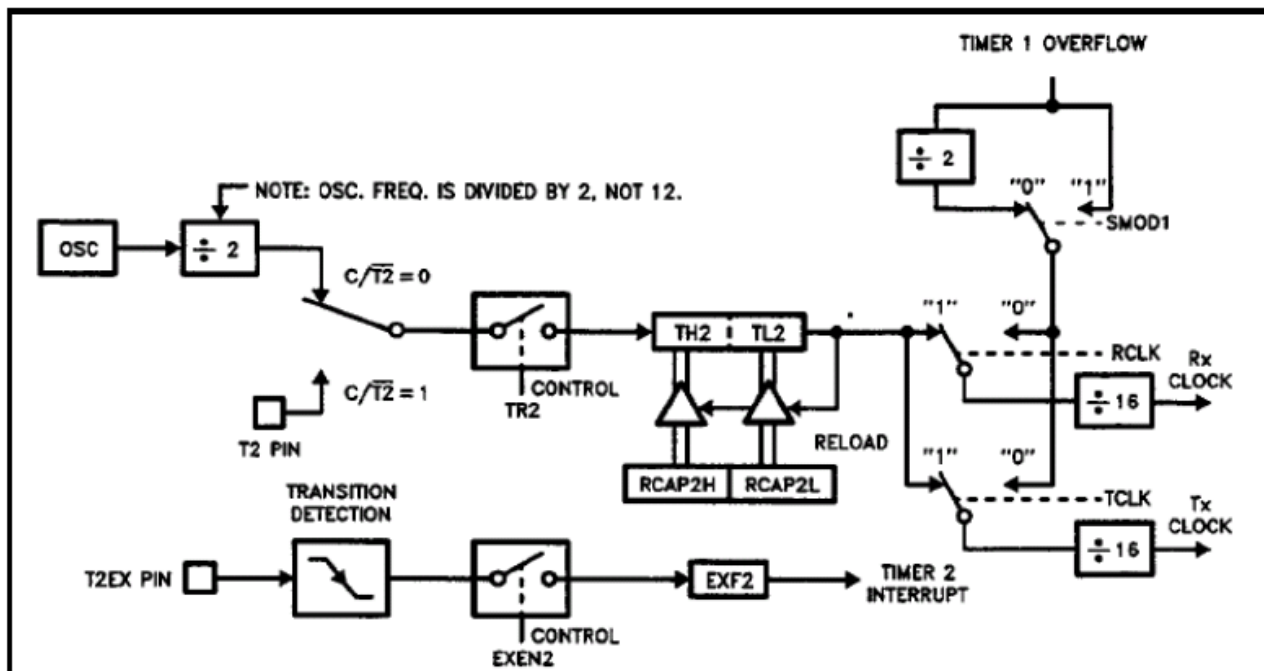


Figure 10-1 Timer 2 in Baud Rate Generator Mode

Figure 10-1 illustrates Timer 2 being used as a baud rate generator. This illustration is valid only if $RCLK + TCLK = 1$ in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. A Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also note that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if needed.

When Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. The results of a read or write may be inaccurate. The RCAP registers may be read, but shouldn't be written to, because a write might overlap with a reload operation and cause write and/or reload errors. In this case, the timer should be turned off (clear TR2) before accessing the Timer 2 or the RCAP registers.

10.5 Serial Port SFR description.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Serial port											
PCON	Power Control	87h	SMOD	-	-	-	GF1	GF0	PD	IDLE	00h
SCON	Serial port 0 control register	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h
SBUF	Serial port 0 data buffer	99h	SBUF[7:0]								XXh

Mnemonic: PCON								Address: 87h	
7	6	5	4	3	2	1	0	Reset	
SMOD	-	-	-	GF1	GF0	PD	IDLE	00h	

Mnemonic: SCON								Address: 98h	
7	6	5	4	3	2	1	0	Reset	
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h	

SMOD: When set, the UART baud-rate is doubled.

SM0, SM1 SM0, SM1 specify the serial port mode as follows:

(Fosc is the system frequency) :				
SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	Fosc /6
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	Fosc /16 or Fosc/32
1	1	3	9-bit UART	variable

SM2: Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.

REN: Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8: In Modes 2 and 3, it is the 9th data bit that will be transmitted. Set or cleared by software as needed.

RB8: In Modes 2 and 3, it is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI: The transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes. It must be cleared by software.

RI: The receive interrupt flag.

11. Programmable Counter Array (PCA)

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. The PCA consists of a dedicated counter which serves as the time base for an array of five compare/capture modules. Its clock input can be programmed to count any one of the following signals:

- Fosc
- Fosc/4
- Fosc/12
- External clock input (CCCI pin at P1.2)

where Fosc is the system Frequency as defined in Section 1. Each compare/capture module can be programmed in any one of the following modes:

- Positive edge capture mode
- Negative edge capture mode
- Both positive and negative edge capture mode
- Timer mode
- High Speed Output mode
- 8-bit PWM mode
- 16-bit PWM mode

When the compare/capture modules are programmed in the capture mode, timer mode, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules share one interrupt vector.

11.1 PCA clock select.

The clock input can be selected from the following four modes:

11.1.1 CCCLK = 00, selected system clock.

The PCA counter increments once per system clock. For example, with a 16MHz crystal, the counter increments every 62.5ns in 6T mode, or 125ns in 12T mode.

11.1.2 CCCLK = 01, selected system clock/4

The PCA counter increments once every 4 system clocks. For example, with a 16MHz crystal, the counter increments every 250ns in 6T mode, or 500ns in 12T mode.

11.1.3 CCCLK = 10, selected system clock/12.

The PCA counter increments once every 12 system clocks. For example, with a 16MHz crystal, the counter increments every 750ns in 6T mode, or 1.5µs in 12T mode.

11.1.4 CCCLK = 11, selected external clock input.

The PCA counter increments when a 1-to-0 transition is detected on the CCCI pin.

NOTE: Irrespective of 12T or 6T, the frequency applied at the CCCI pin must not exceed $F(\text{crystal})/8$. So, for a 16MHz crystal, $F(\text{CCCI})$ must not exceed 2 MHz.

Table 11-1 PCA clock sample period example

Machine cycle	Fcry (MHz)	CCCLK[1:0]	PCA counter increment	Div	Sample period(μs)
6T	16	00	1 system clocks	1	0.0625
6T	16	01	2 system clocks	4	0.25
6T	16	10	12 system clocks	12	0.75
12T	16	00	1 system clocks	2	0.125
12T	16	01	2 system clocks	8	0.5
12T	16	10	12 system clocks	24	1.5
6T/12T	16	11	External clock input (CCCI pin)	/	External clock input (CCCI pin)

Fig. 11-1: PCA clock selection

Note: apart from the PCA counter being incremented from the External clock input, Sample period(μs) = 1 / (Fcrystal / Div)

11.2 PCA Compare/Capture mode

11.2.1 Positive edge capture mode:

The external input pins CC0 through CC4 are sampled for a 0-to 1 transition. When a positive edge transition is detected, the hardware loads the 16-bit value of the PCA counter (CCCH, CCCL) into the module's capture registers (CCnDH, CCnDL). The resulting value in the capture registers reflects the PCA timer value at the time a transition was detected on the CCn pin.

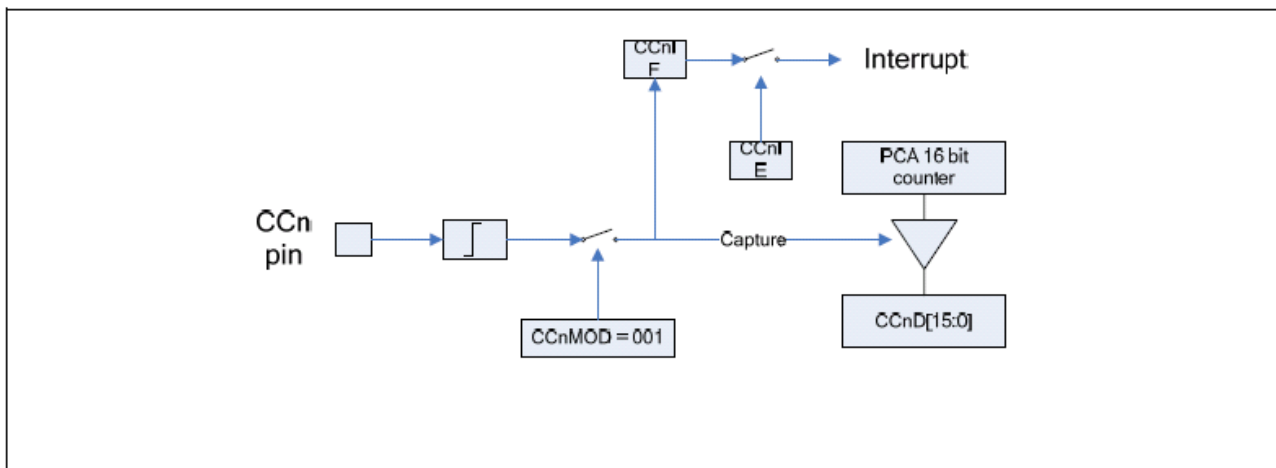


Fig 11-2: PCA capture mode with positive edge

11.2.2 Negative edge capture mode:

The external input pins CC0 through CC4 are sampled for a 1-to 0 transition. When a negative edge transition is detected, the hardware loads the 16-bit value of the PCA counter (CCCH, CCCL) into the module's capture registers (CCnDH, CCnDL). The resulting value in the capture registers reflects the PCA timer value at the time a transition was detected on the CCn pin.

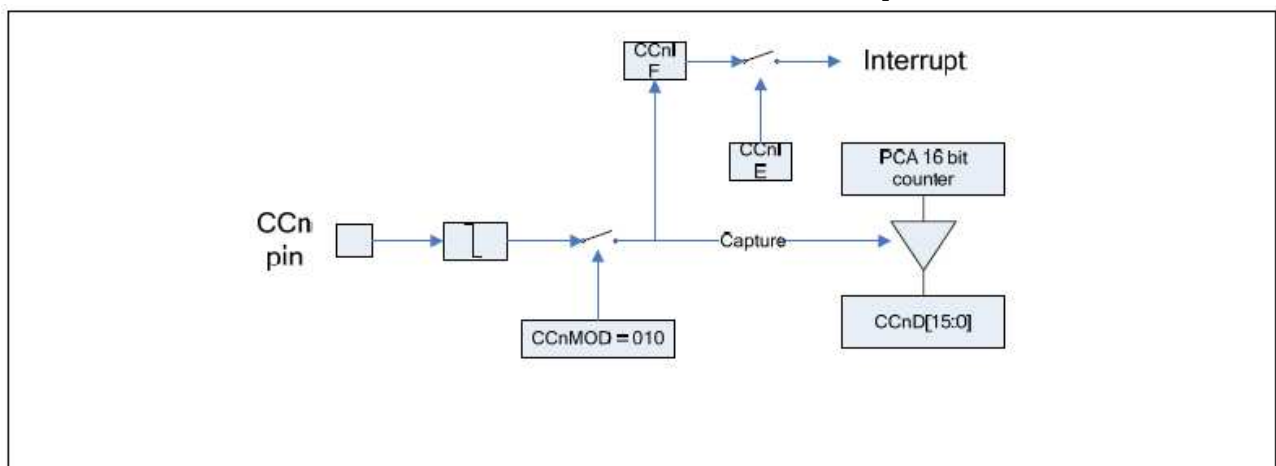


Fig 11-3: PCA capture mode with negative edge

11.2.3 Both positive and negative edge capture mode:

The external input pins CC0 through CC4 are sampled for a 0-to-1 or 1-to-0 transition. When a positive edge or negative edge transition is detected, the hardware loads the 16-bit value of the PCA counter (CCCH, CCCL) into the module's capture registers (CCnDH, CCnDL). The resulting value in the capture registers reflects the PCA timer value at the time a transition was detected on the CCn pin.

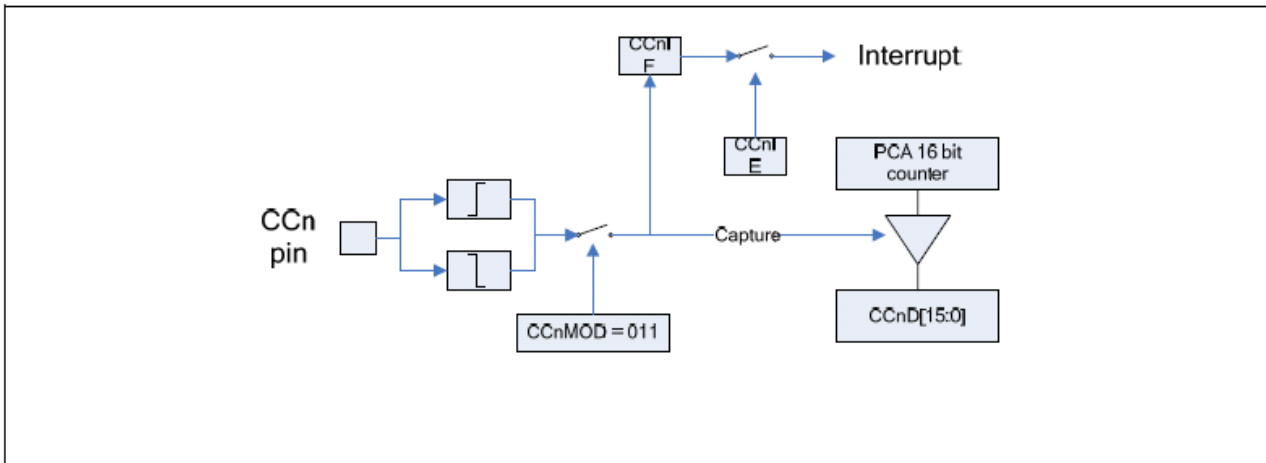


Fig 11-4: PCA capture mode with both negative and positive edge

11.2.4 Timer mode:

In the Timer mode. When the PCA counter rolls over, the CCnIF bit will be set which can then generate an interrupt if CCnIE is enabled.

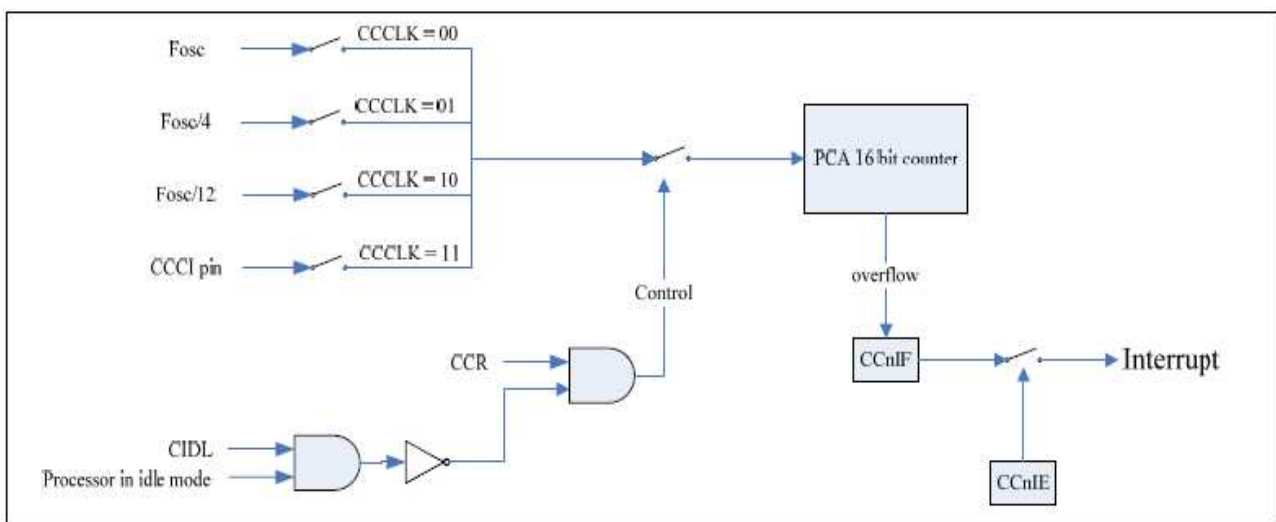


Fig 11-5: PCA Timer mode

11.2.5 High speed output:

The high speed output mode toggles a CCn pin when a match occurs between the PCA counter and a pre-loaded value (CCnD[15:0]) in a module's compare registers. When the PCA counter matches the CCnD register, the TOGn toggles and is output on the CCn pin. Here is an example: If the TOGn register is set to one by software, the hardware will clear the TOGn register and output low on the CCn pin when the PCA counter matches the CCnD register. If software doesn't set the bit before the next match, the hardware will set the TOGn register and output high automatically.

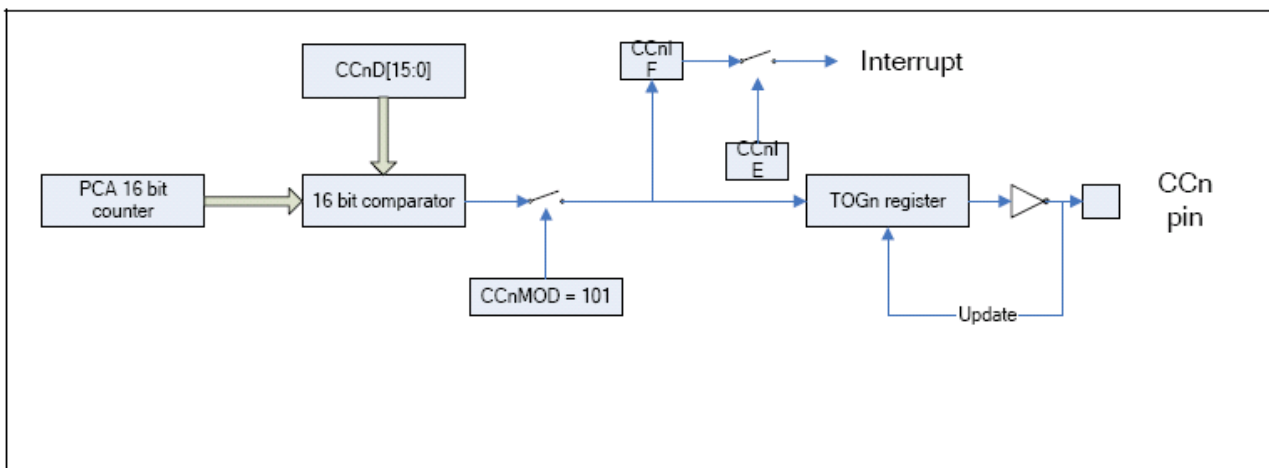


Fig 11-6: PCA high speed output

11.2.6 8-bit PWM:

Any, or all, of the five PCA modules can be programmed to be a Pulse Width Modulator (PWM). The PWM output can be used to convert digital data to an analog signal through a simple external circuit. The frequency of the PWM depends on the clock source for the PCA counter. The pulse width depends on the CCnDL[7:0] register. CCnDH[15:8] is not used. When all the bits in CCnDL[7:0] are zero, the CCn pin will always remain low. The PWM frequency is selected by SFR CCCLK as :

- When CCCLK = 00, PWM output frequency = $F_{osc}/256$.
- When CCCLK = 01, PWM output frequency = $(F_{osc}/4)/256$.
- When CCCLK = 10, PWM output frequency = $(F_{osc}/12)/256$.
- When CCCLK = 11, PWM output frequency = (CCCI pin frequency)/256.

If users want to use the PWM mode, the software must set the CCR register and always keep it high. If software clears the CCR register, the PWM will be disabled and keep the CCn pin low.

11.2.7 16-bit PWM:

It is almost the same as 8-bit PWM. Any or all of the five PCA modules can be programmed to be a 16-bit PWM. The frequency of the PWM depends on the clock source for the PCA counter. The pulse width depends on the CCnD[15:0] register. When all the bits in CCnD[15:0] are zero, the CCn pin will always remain low. The PWM frequency is selected by SFR CCCLK as :

When CCCLK = 00, PWM output frequency = $F_{osc}/65536$.

When CCCLK = 01, PWM output frequency = $(F_{osc}/4)/65536$.

When CCCLK = 10, PWM output frequency = $(F_{osc}/12)/65536$.

When CCCLK = 11, PWM output frequency = $(CCCI \text{ pin frequency })/65536$.

Still, if users want to use this PWM mode, the software must set the CCR register and always keep it high. If software clears the CCR register, the PWM will be disabled and keep the CCn pin to low.

11.3 PCA SFR description

Mnemonic	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
PCAC1	PCA Control register 1	A1h	CCR	CIDL	--	CC4IE	CC3IE	CC2IE	CC1IE	CC0IE	00h
PCAC2	PCA Control register 2	A2h	CCCLK[1:0]			CC4IF	CC3IF	CC2IF	CC1IF	CC0IF	00h
PCAH	PCA Counter high byte	9Ah	PCA[15:8]								00h
PCAL	PCA Counter low byte	9Bh	PCA[7:0]								00h
CC0CON	CC0 Control register	A3h	-	-	-	TOG0	-	CC0MOD[2:0]		00h	
CC0DH	CC0 data high byte	9Ch	CC0D[15:8]								00h
CC0DL	CC0 data low byte	9Dh	CC0D[7:0]								00h
CC1CON	CC1 Control register	A4h	-	-	-	TOG1	-	CC1MOD[2:0]		00h	
CC1DH	CC1 data high byte	9Eh	CC1D[15:8]								00h
CC1DL	CC1 data low byte	9Fh	CC1D[7:0]								00h
CC2CON	CC2 Control register	A5h	-	-	-	TOG2	-	CC2MOD[2:0]		00h	
CC2DH	CC2 data high byte	91h	CC2D[15:8]								00h
CC2DL	CC2 data low byte	92h	CC2D[7:0]								00h
CC3CON	CC3 Control register	A6h	-	-	-	TOG3	-	CC3MOD[2:0]		00h	
CC3DH	CC3 data high byte	93h	CC3D[15:8]								00h
CC3DL	CC3 data low byte	94h	CC3D[7:0]								00h
CC4CON	CC4 Control register	A7h	-	-	-	TOG4	-	CC4MOD[2:0]		00h	
CC4DH	CC4 data high byte	95h	CC4D[15:8]								00h
CC4DL	CC4 data low byte	96h	CC4D[7:0]								00h

11.3.1 PCA Control register 1

Mnemonic: PCAC1							Address: A1h	
7	6	5	4	3	2	1	0	Reset
CCR	CIDL	-	CC4IE	CC3IE	CC2IE	CC1IE	CC0IE	00h
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	

CCR: PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.

CIDL: Counter Idle control: CIDL = 0 sets the PCA counter to continue functioning during idle mode. CIDL = 1 sets it to be gated off during idle mode.

CCnIE: CC0~CC4 interrupt enable. CCnIE = 1 to enable interrupt, 0 to disable it.

11.3.2 PCA Control register 2

Mnemonic: PCAC2							Address: A2h	
7	6	5	4	3	2	1	0	Reset
CCCLK[1:0]		-	CC4IF	CC3IF	CC2IF	CC1IF	CC0IF	00h
R/W		-	R/W	R/W	R/W	R/W	R/W	

CCCLK[1:0]: Compare/Capture clock source select

CC0CLK[1:0]	Clock source
00	Fosc
01	Fosc/4
10	Fosc/12
11	External clock input (CCCI pin)

CcnIF: CC0 ~ CC4 interrupt flag. Must be cleared by software.

11.3.3 PCA Counter register

Mnemonic: PCAH							Address: 9Ah	
7	6	5	4	3	2	1	0	Reset
PCA[15:8]								00h
R/W								

Mnemonic: PCAL							Address: 9Bh	
7	6	5	4	3	2	1	0	Reset
PCA[7:0]								00h
R/W								

11.3.4 Compare/Capture channel 0 control register

Mnemonic: CC0CON Address: A3h

7	6	5	4	3	2	1	0	Reset
-	-	-	TOG0	-	CC0MOD[2:0]			00h
-	-	-	R/W	-	R/W			

CC0MOD[2:0]: Compare/Capture channel 0 modes select.

CC0MOD[2:0]	Function
000	Disable PCA channel 0
001	Positive edge capture mode
010	Negative edge capture mode
011	Both positive and negative edge capture mode
100	Timer mode
101	High Speed Output mode
110	8-bit PWM
111	16-bit PWM

TOG0: CC0 toggle register.

11.3.5 CC0 Data register

Mnemonic: CC0DH Address: 9Ch

7	6	5	4	3	2	1	0	Reset
CC0D[15:8]								00h
R/W								

Mnemonic: CC0DL Address: 9Dh

7	6	5	4	3	2	1	0	Reset
CC0D[7:0]								00h
R/W								

11.3.6 Compare/Capture channel 1 control register

Mnemonic: CC1CON Address: A4h

7	6	5	4	3	2	1	0	Reset
-	-	-	TOG1	-	CC1MOD[2:0]			00h
-	-	-	R/W	-	R/W			

CC1MOD[2:0]: Compare/Capture channel 1 modes select.

CC1MOD[2:0]	Function
000	Disable PCA channel 1
001	Positive edge capture mode
010	Negative edge capture mode
011	Both positive and negative edge capture mode
100	Timer mode
101	High Speed Output mode
110	8-bit PWM
111	16-bit PWM

TOG1: CC1 toggle register.

11.3.7 CC1 Data register

Mnemonic: CC1DH							Address: 9Eh	
7	6	5	4	3	2	1	0	Reset
CC1D[15:8]							00h	
R/W								

Mnemonic: CC1DL							Address: 9Fh	
7	6	5	4	3	2	1	0	Reset
CC1D[7:0]							00h	
R/W								

11.3.8 Compare/Capture channel 2 control register

Mnemonic: CC2CON							Address: A5h	
7	6	5	4	3	2	1	0	Reset
-	-	-	TOG2	-	CC2MOD[2:0]		00h	
-	-	-	R/W	-	R/W			

CC2MOD[2:0]: Compare/Capture channel 2 modes select.

CC2MOD[2:0]	Function
000	Disable PCA channel 2
001	Positive edge capture mode
010	Negative edge capture mode
011	Both positive and negative edge capture mode
100	Timer mode
101	High Speed Output mode
110	8-bit PWM
111	16-bit PWM

TOG2: CC2 toggle register.

11.3.9 CC2 Data register

Mnemonic: CC2DH							Address: 91h	
7	6	5	4	3	2	1	0	Reset
CC2D[15:8]								00h
R/W								

Mnemonic: CC2DL							Address: 92h	
7	6	5	4	3	2	1	0	Reset
CC2D[7:0]								00h
R/W								

11.3.10 Compare/Capture channel 3 control register

Mnemonic: CC3CON							Address: A6h	
7	6	5	4	3	2	1	0	Reset
-	-	-	TOG3	-	CC3MOD[2:0]		00h	
-	-	-	R/W	-	R/W			

CC3MOD[2:0]: Compare/Capture channel 3 modes select.

CC3MOD[2:0]	Function
000	Disable PCA channel 3
001	Positive edge capture mode
010	Negative edge capture mode
011	Both positive and negative edge capture mode
100	Timer mode
101	High Speed Output mode
110	8-bit PWM
111	16-bit PWM

TOG3: CC3 toggle register.

11.3.11 CC3 Data register

Mnemonic: CC3DH							Address: 93h	
7	6	5	4	3	2	1	0	Reset
CC3D[15:8]								00h
R/W								

Mnemonic: CC3DL							Address: 94h	
7	6	5	4	3	2	1	0	Reset
CC3D[7:0]								00h
R/W								

11.3.12 Compare/Capture channel 4 control register

Mnemonic: CC4CON							Address: A7h	
7	6	5	4	3	2	1	0	Reset
-	-	-	TOG4	-	CC4MOD[2:0]			00h
-	-	-	R/W	-	R/W			

CC4MOD[2:0]: Compare/Capture channel 4 modes select.

CC4MOD[2:0]	Function
000	Disable PCA channel 4
001	Positive edge capture mode
010	Negative edge capture mode
011	Both positive and negative edge capture mode
100	Timer mode
101	High Speed Output mode
110	8-bit PWM
111	16-bit PWM

TOG4: CC4 toggle register.

11.3.13 CC4 Data register

Mnemonic: CC4DH							Address: 95h	
7	6	5	4	3	2	1	0	Reset
CC4D[15:8]								00h
R/W								

Mnemonic: CC4DL							Address: 96h	
7	6	5	4	3	2	1	0	Reset
CC4D[7:0]								00h
R/W								

12 Expanded External Interrupt (EEI) interface

CRD89C51RA2 implements an EEI interface allowing the connection of an 8xn matrix keyboard. It is based on 8 inputs with programmable interrupt capability for either high or low levels. These inputs are available as an alternate function of P1 and allow to exit from idle and power-down modes described in Section 14.

The EEI interfaces with the CPU core through 3 SFR: KBLs, the EEI Level Selection register, KBE, the EEI Enable register, and KBF, the EEI Flag register.

The EEI inputs are considered as 8 independent interrupt sources sharing the same interrupt vector. Figure 12-1 shows that each EEI input has the capability to detect a programmable level according to KBLs.x bit value. Level detection is then reported in interrupt flags KBF.X that can be masked by software using KBE.x bits. An interrupt enable bit (KBD in IE1) allows global enable or disable of the keyboard interrupt as in Fig. 12-2.

This structure allows keyboard arrangements from 1xn to 8xn matrix, and allows usage of P1 inputs for other purpose. P1 inputs allow exiting from the idle and power-down modes.

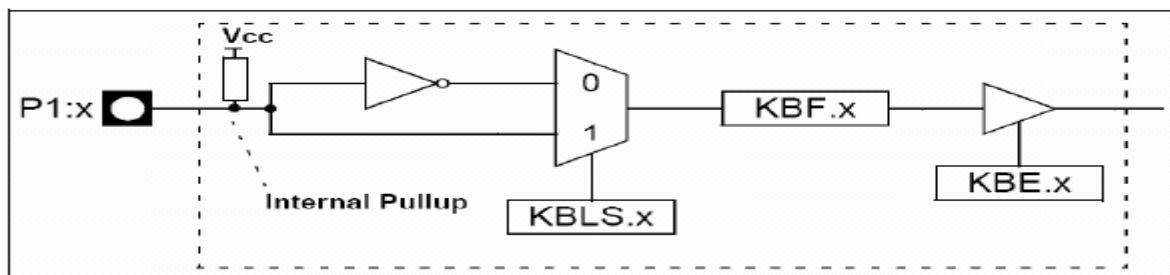


Figure 12.1 EEI interface Block Diagram

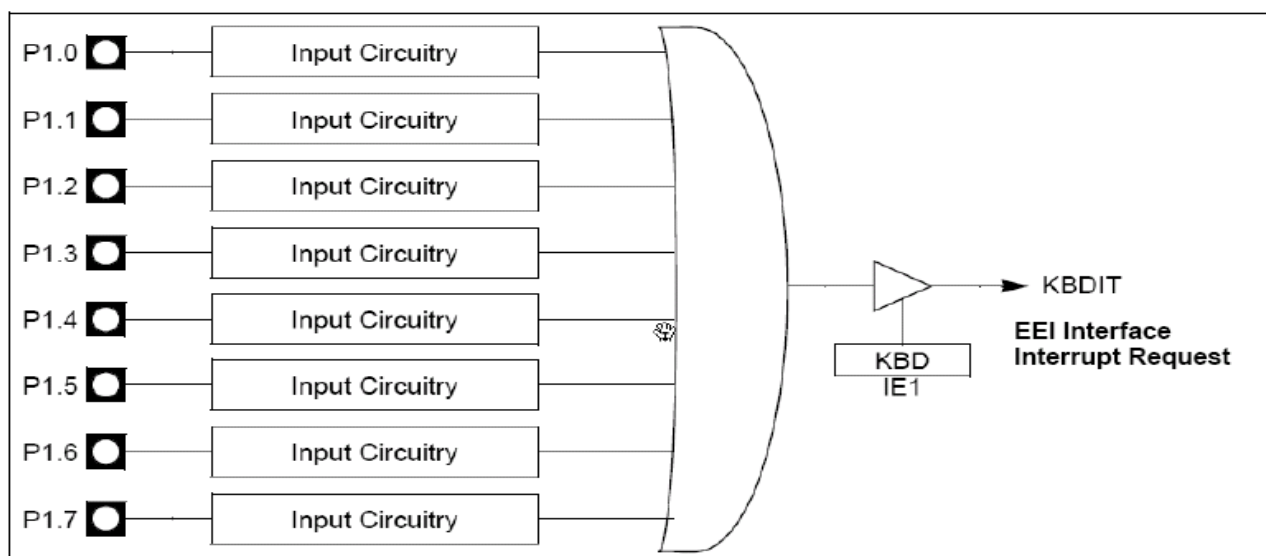


Figure 12.2 EEI input Circuitry

12.1 EEI SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Keyboard interface											
KBLS	EEI level Selector register	FDh	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0	00h
KBE	EEI Input Enable register	FEh	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	00h
KBF	EEI Flag register	FFh	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0	00h

12.1.1 EEI level selector register

Mnemonic: KBLS

Address: FDh

7	6	5	4	3	2	1	0	Reset
KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0	00h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

KBLS7: EEI line 7 level selection bit

Cleared to enable a low level detection on Port line 7.

Set to enable a high level detection on Port line 7.

KBLS6: EEI line 6 level selection bit

Cleared to enable a low level detection on Port line 6.

Set to enable a high level detection on Port line 6.

KBLS5: EEI line 5 level selection bit

Cleared to enable a low level detection on Port line 5.

Set to enable a high level detection on Port line 5.

KBLS4: EEI line 4 level selection bit

Cleared to enable a low level detection on Port line 4.

Set to enable a high level detection on Port line 4.

KBLS3: EEI line 3 level selection bit

Cleared to enable a low level detection on Port line 3.

Set to enable a high level detection on Port line 3.

KBLS2: EEI line 2 level selection bit

Cleared to enable a low level detection on Port line 2.

Set to enable a high level detection on Port line 2.

KBLS1: EEI line 1 level selection bit

Cleared to enable a low level detection on Port line 1.

Set to enable a high level detection on Port line 1.

KBLS0: EEI line 0 level selection bit

Cleared to enable a low level detection on Port line 0.

Set to enable a high level detection on Port line 0.

12.1.2 EEI input enable register

Mnemonic: KBE								Address: FEh
7	6	5	4	3	2	1	0	Reset
KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	00h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- KBE7:** EEI line 7 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.7 bit in KBE register to generate an interrupt request.
- KBE6:** EEI line 6 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.6 bit in KBE register to generate an interrupt request.
- KBE5:** EEI line 5 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.5 bit in KBE register to generate an interrupt request.
- KBE4:** EEI line 4 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.4 bit in KBE register to generate an interrupt request.
- KBE3:** EEI line 3 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.3 bit in KBE register to generate an interrupt request.
- KBE2:** EEI line 2 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.2 bit in KBE register to generate an interrupt request.
- KBE1:** EEI line 1 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.1 bit in KBE register to generate an interrupt request.
- KBE0:** EEI line 0 Enable bit.
Cleared to enable standard I/O pin.
Set to enable KBE.0 bit in KBE register to generate an interrupt request.

12.1.3 EEI flag register

Mnemonic: KBF							Address: FFh	
7	6	5	4	3	2	1	0	Reset
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0	00h
R	R	R	R	R	R	R	R	

KBF7: EEI line 7 flag.

Set by hardware when the port line 7 detects a programmed level. It generates a EEI interrupt request if the KBE.7 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF6: EEI line 6 flag.

Set by hardware when the port line 6 detects a programmed level. It generates a EEI interrupt request if the KBE.6 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF5: EEI line 5 flag.

Set by hardware when the port line 5 detects a programmed level. It generates a EEI interrupt request if the KBE.5 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF4: EEI line 4 flag.

Set by hardware when the port line 4 detects a programmed level. It generates a EEI interrupt request if the KBE.4 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF3: EEI line 3 flag.

Set by hardware when the port line 3 detects a programmed level. It generates a EEI interrupt request if the KBE.3 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF2: EEI line 2 flag.

Set by hardware when the port line 2 detects a programmed level. It generates a EEI interrupt request if the KBE.2 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

KBF1: EEI line 1 flag.

Set by hardware when the port line 1 detects a programmed level. It generates a EEI interrupt request if the KBE.1 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.


KBF0: EEI line 0 flag.

Set by hardware when the port line 0 detects a programmed level. It generates a EEI interrupt request if the KBE.0 bit in the KBE register is set. The register is read only access; the flag is automatically cleared by reading the register.

13 Interrupts

The CRD89C51RA2 has a total of 8 interrupt vectors, they include two external interrupts, three timer interrupts, one serial port interrupt, the EEI interrupts, and a PCA interrupt.

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the IE, or the IE1 register. This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Interrupt Source	Interrupt Vector	Polling sequence
External interrupt 0	0003h	 Polling sequence
Timer 0	000Bh	
External interrupt 1	0013h	
Timer 1	001Bh	
Serial Port	0023h	
Timer 2	002Bh	
EEI	0033h	
PCA interrupt	003Bh	

13.1 SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
EEI interface											
IE	Interrupt Enable register	A8h	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00h
IE1	Interrupt Enable 1 register	A9h	-	-	-	-	-	-	EPCA	KBD	00h
IP	Interrupt Priority register	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	00h
IP1	Interrupt Priority 1 register	B9h	-	-	-	-	-	-	PPCA	PKBD	00h

Mnemonic: IE

Address: A8h

7	6	5	4	3	2	1	0	Reset
EA	-	ET2	ES	ET1	EX1	ET0	EX0	00h

EA: Disable all interrupt. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

ET2: Timer 2 interrupt enable bit.

ES: Serial port interrupt enable bit.

ET1: Timer 1 interrupt enable bit.

EX1: External interrupt 1 enable bit.

ET0: Timer 0 interrupt enable bit.

EX0: External interrupt 0 enable bit.

Mnemonic: IE1

Address: A9h

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	EPCA	KBD	00h

EPCA: PCA interrupt enable bit.

KBD: EEI interrupt enable bit. Cleared to disable EEI interrupt. Set to enable EEI interrupt.

Mnemonic: IP

Address: B8h

7	6	5	4	3	2	1	0	Reset
-	-	PT2	PS	PT1	PX1	PT0	PX0	00h

PT2: Timer 2 interrupt priority bit. PT2 = 1 is high priority.

PS: Serial port 0 interrupt priority bit. PS = 1 is high priority.

PT1: Timer 1 interrupt priority bit. PT1 = 1 is high priority.

PX1: External interrupt 1 priority bit. PX1 = 1 is high priority.

PT0: Timer 0 interrupt priority bit. PT0 = 1 is high priority.

PX0: External interrupt 0 priority bit. PX0 = 1 is high priority.

Mnemonic: IP1

Address: B9h

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	PPCA	PKBD	00h

PPCA: PCA interrupt priority bit. PPCA = 1 is high priority.

PKBD: EEI interrupt priority bit. PKBD = 1 is high priority.

14 Power Management

14.1 Idle Mode

Setting the IDLE bit of PCON register invokes the IDLE mode. During IDLE mode, program execution is halted, leaving timers, serial ports and other clock sources running. The CPU will exit idle mode when either an interrupt, or a reset, occurs. Power consumption drops because the CPU is not active.

14.2 Power down mode

When the PD bit in the PCON register is set, the CPU enters the power-down mode as idle mode does. But the peripherals are also stopped. To exit from power down mode is done by a hardware reset or external interrupts.

14.3 SFR description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Power Management											
PCON	Power Control	87h	SMOD	-	-	-	GF1	GF0	PD	IDLE	00h

Mnemonic: PCON

Address: 87h

7	6	5	4	3	2	1	0	Reset
SMOD	-			GF1	GF0	PD	IDLE	00h

GF1: General-purpose flag bit.

GF0: General-purpose flag bit.

PD: When set to "1", the MCU will into Power-down mode.

IDLE: When set to "1", the MCU will into IDLE mode.

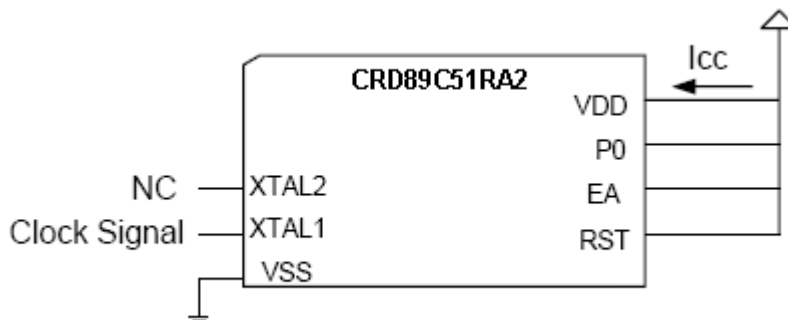
Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 25	Oscillator Frequency	2	25	25	MHz	

DC Characteristics

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 °C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Icc Active Mode Test circuit:



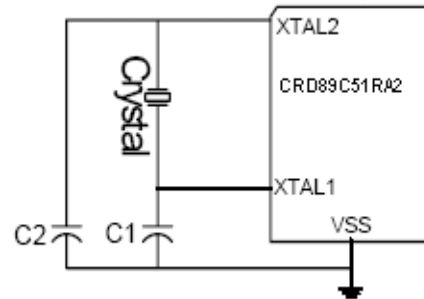
AC Characteristics

(16/25 MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT -20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT+20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT-10		3xT+10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT-20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT-35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63				1/fosc	nS	

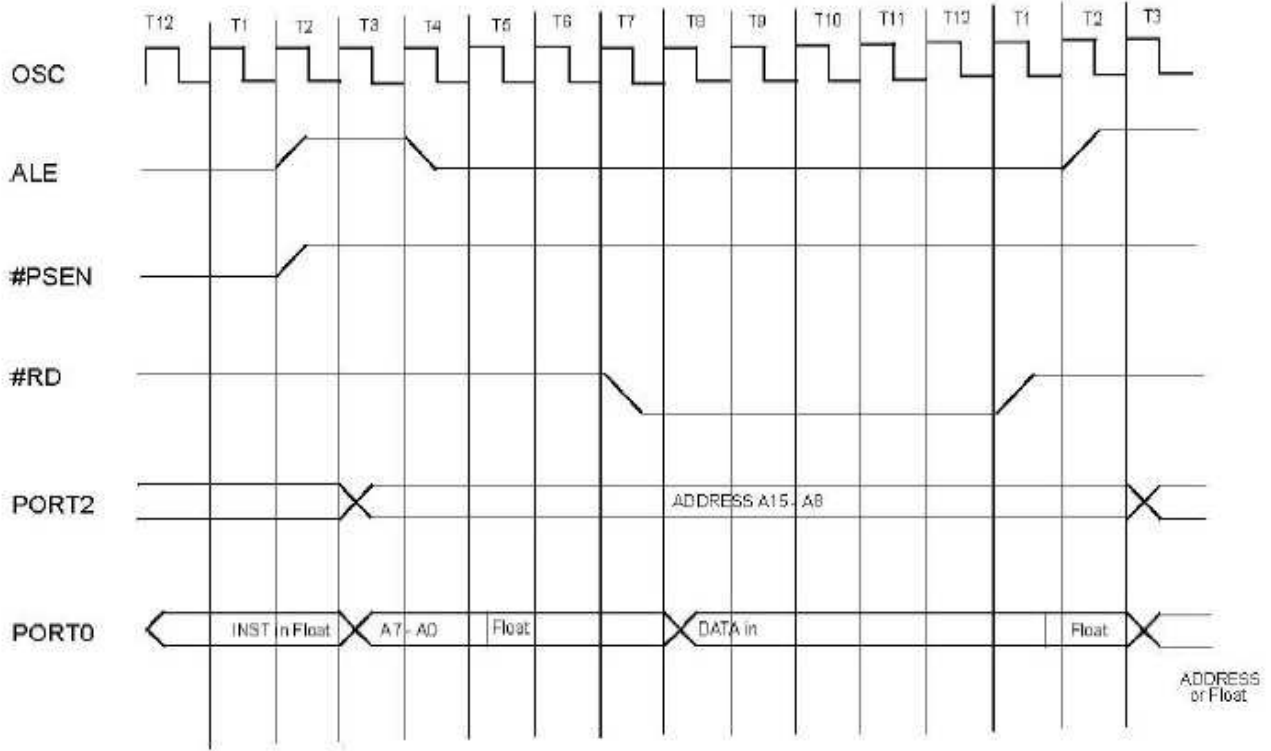
Application Reference

Valid for CRD89C51RA2				
X'tal	2MHz	6MHz	10MHz	12MHz
C1	47 pF	35 pF	30 pF	30 pF
C2	47 pF	35 pF	30 pF	30 pF
X'tal	16MHz	25MHz		
C1	30 pF	25 pF		
C2	30 pF	25 pF		

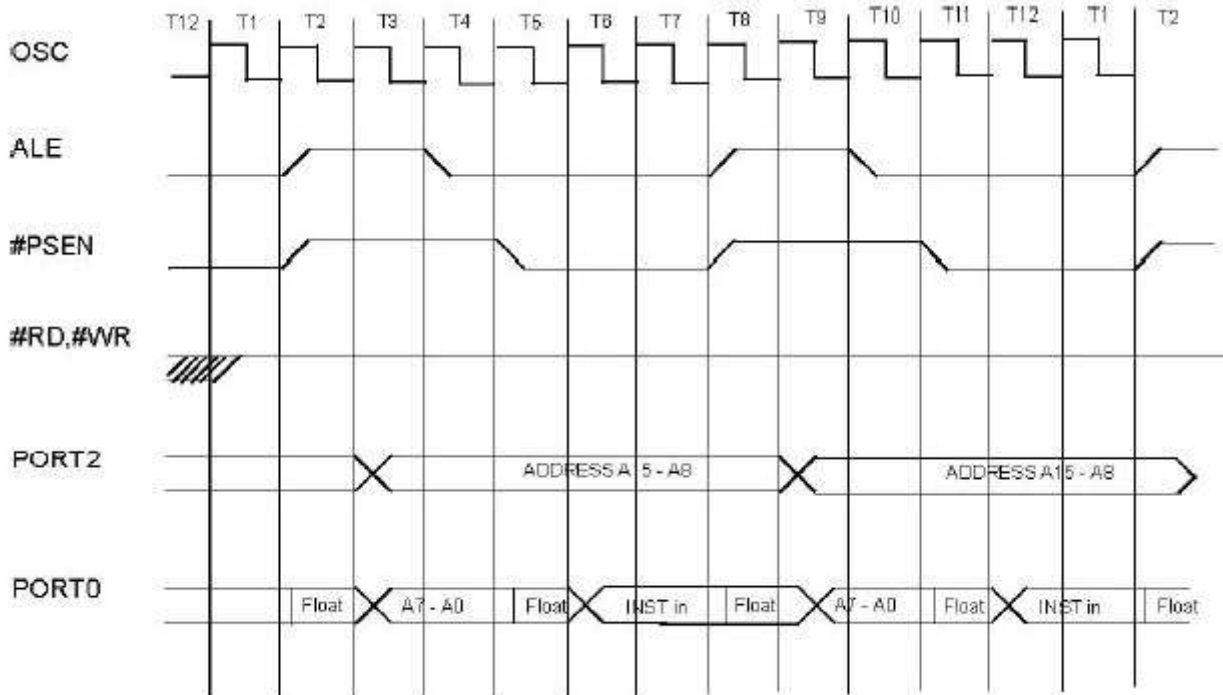


NOTE: The oscillation circuit may vary with different crystals, or ceramic resonators, in higher oscillation frequencies. This is due to each crystal, or ceramic resonator, having its own characteristics. The user should check with the crystal, or ceramic resonator, manufacturer in order to obtain advice on the appropriate values of the external components.

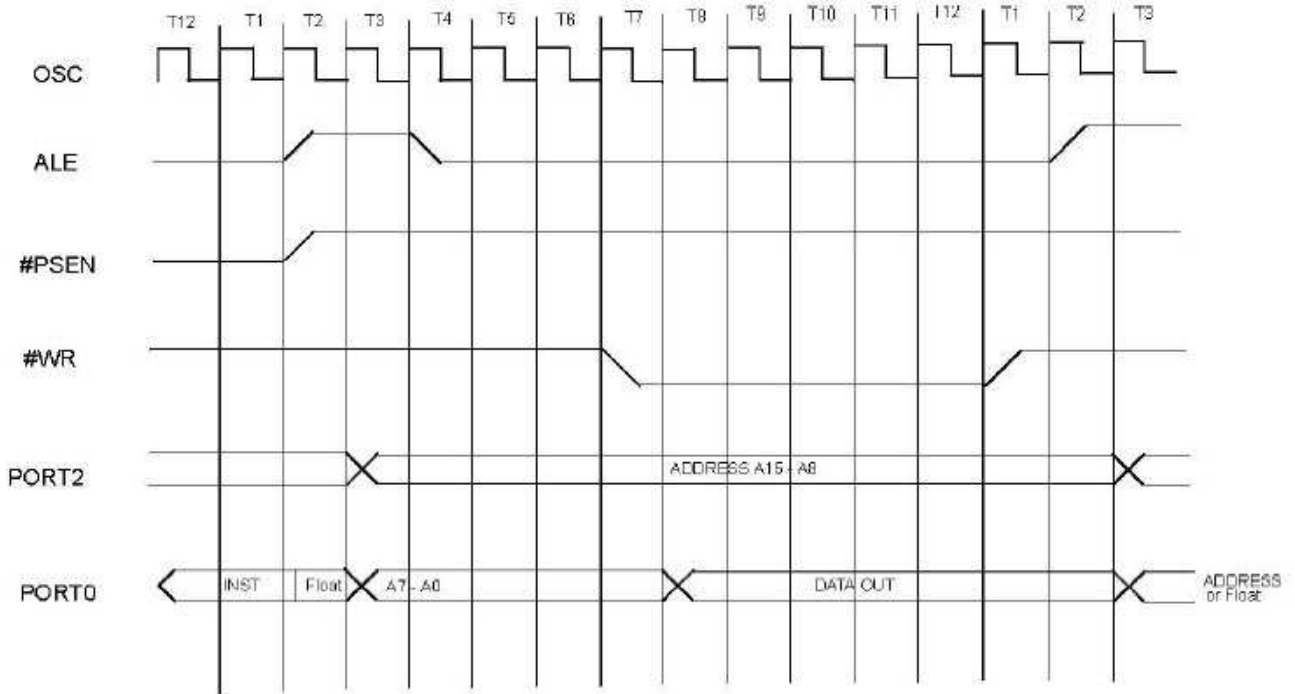
Data Memory Read Cycle Timing



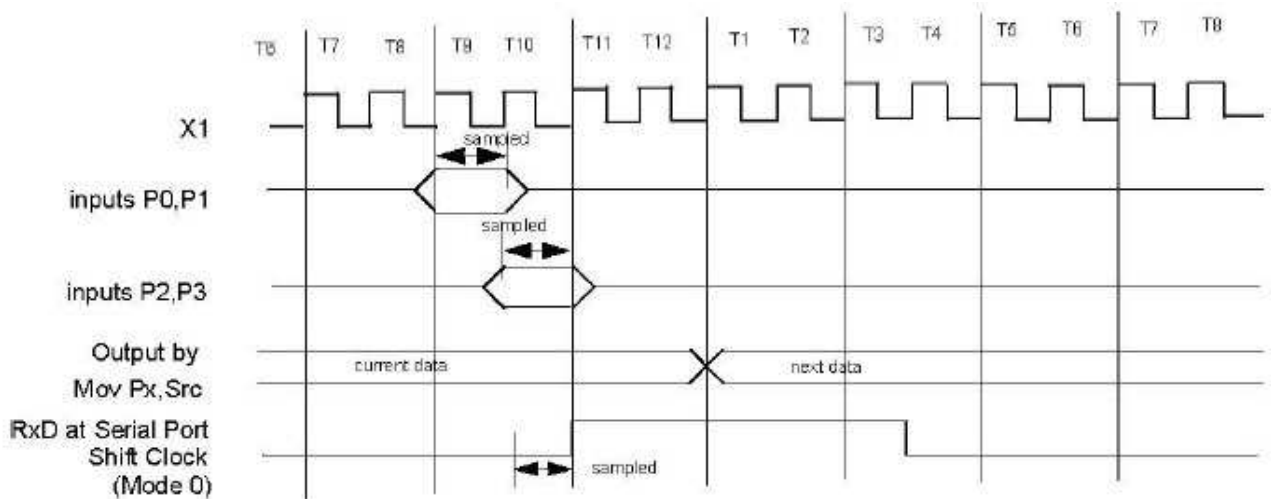
Program Memory Read Cycle Timing



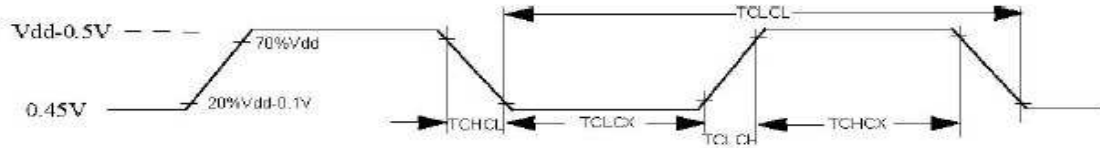
Data Memory Write Cycle Timing



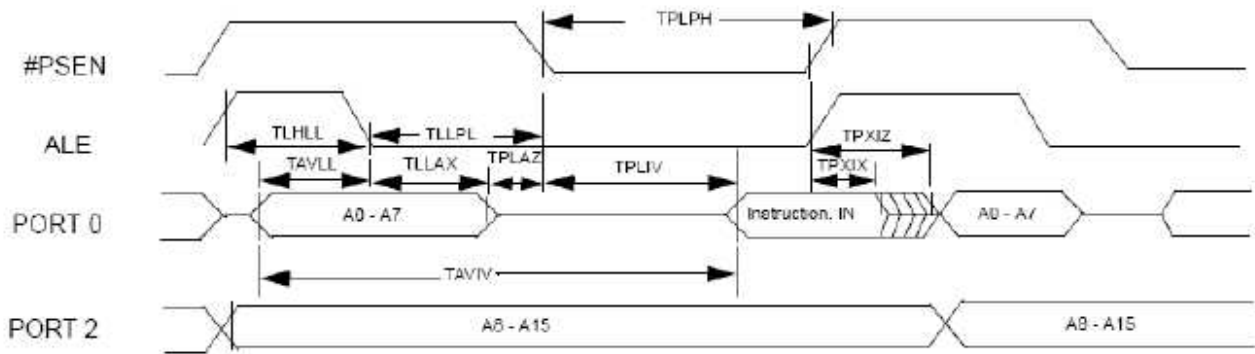
I/O Ports Timing



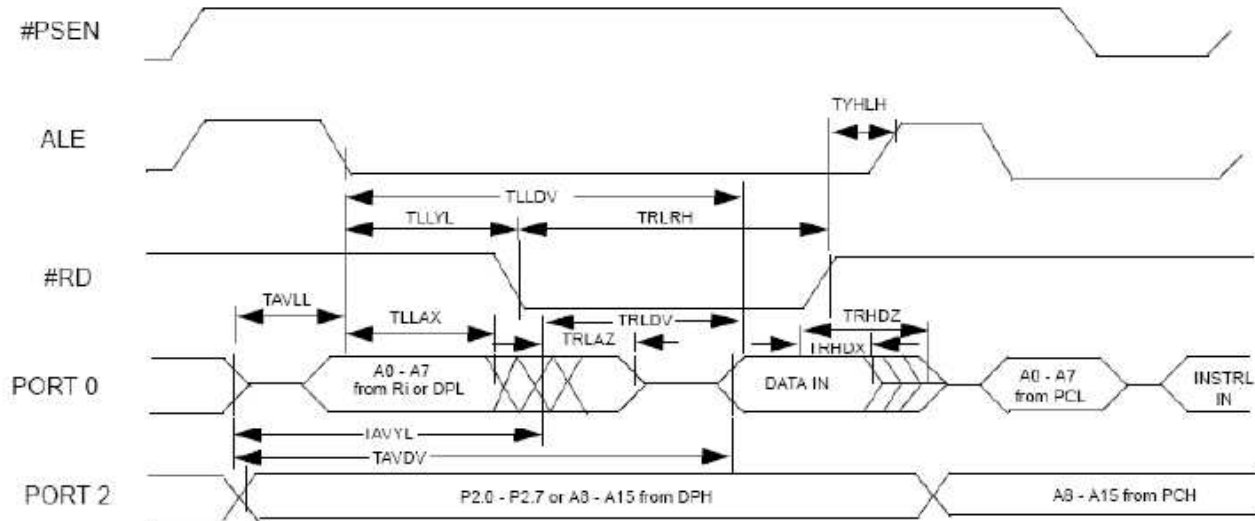
Critical Timing Requirement of External Clock (Vss=0.0V assumed)



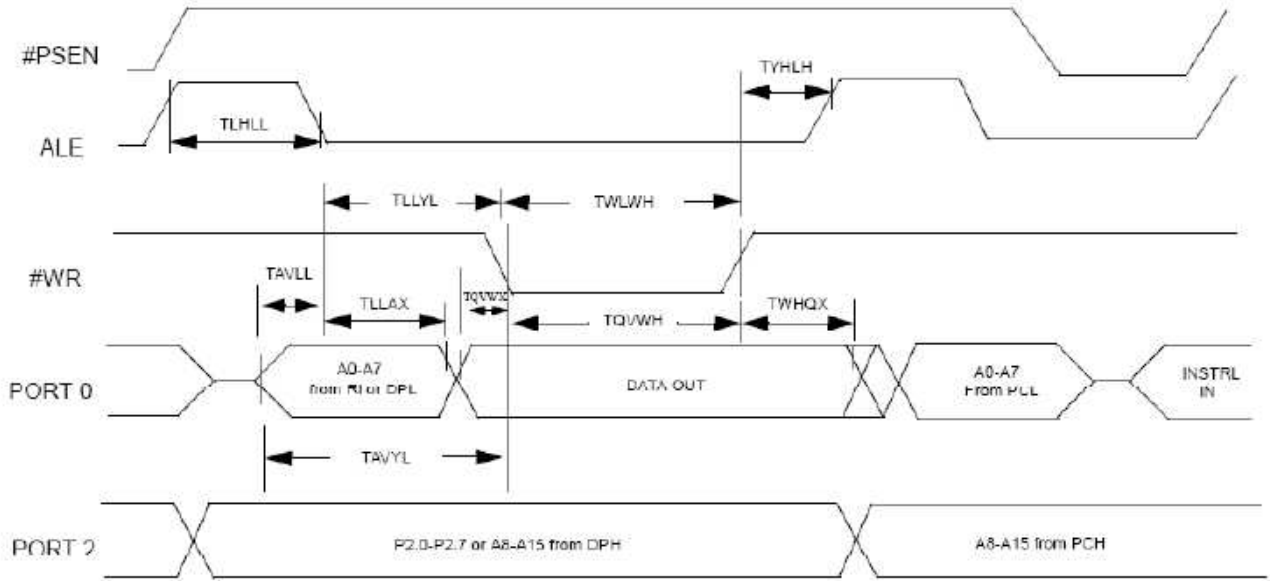
Tm.I External Program Memory Read Cycle



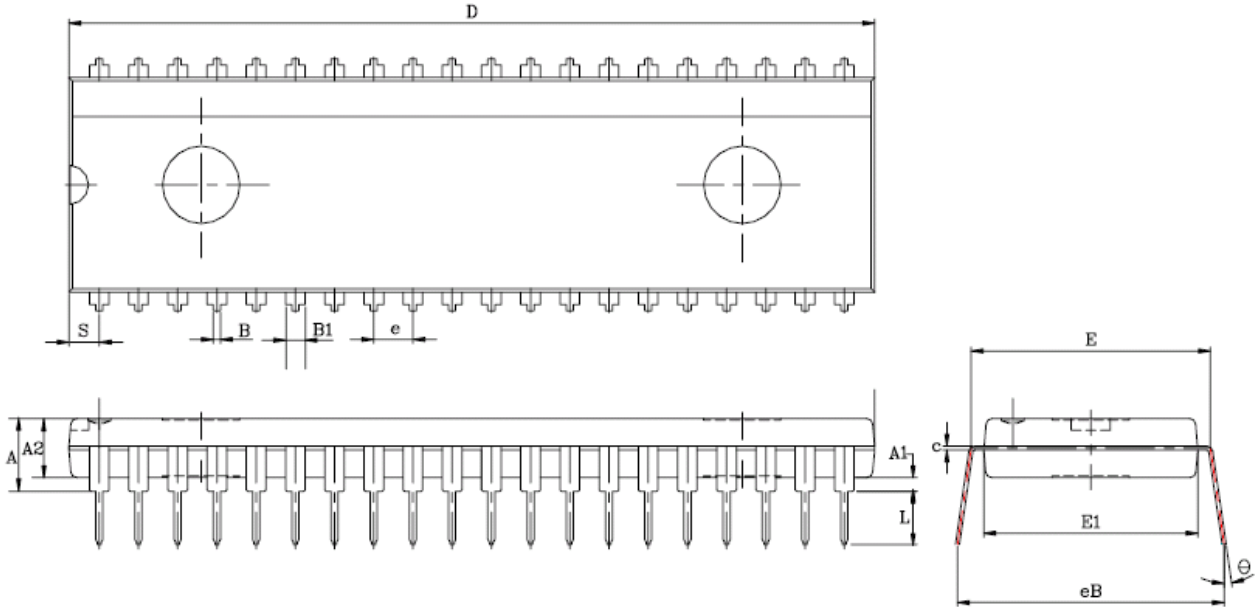
Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



40L PDIP (600mil) Package outline:

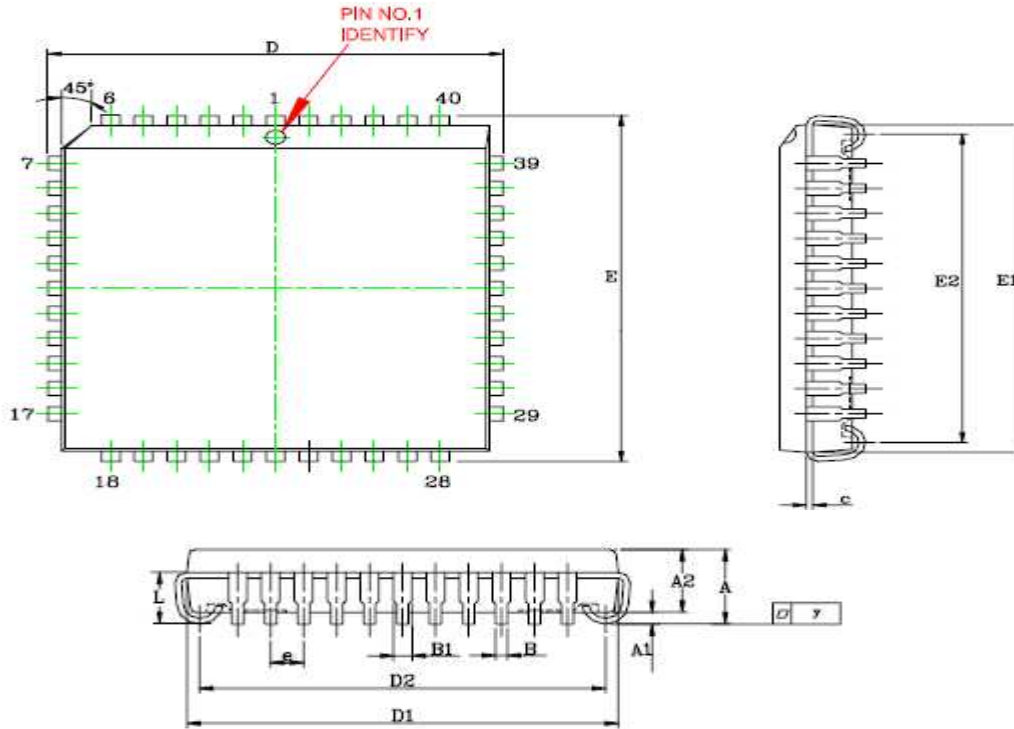


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	5.59	—	—	0.220
A1	0.25	—	—	0.010	—	—
A2	3.18	—	4.95	0.125	—	0.195
B	0.36	—	0.58	0.014	—	0.023
B1	0.76	—	1.78	0.030	—	0.070
c	0.20	—	0.38	0.008	—	0.015
D	50.29	—	53.21	1.980	—	2.095
E	14.99	—	15.88	0.590	—	0.625
E1	12.32	—	14.73	0.485	—	0.580
e	—	2.54	—	—	0.100	—
eB	15.24	—	17.78	0.600	—	0.700
L	2.921	—	5.08	0.115	—	0.200
S	—	—	2.43	—	—	0.096
θ	0°	—	15°	0°	—	15°

Note:

1. Dimensions D & E1, do not include mold protrusion, but are maximum plastic body dimensions, including mold mismatch.
2. Dimension B1 does not include dambar protrusion.

44L PLCC Package outline:

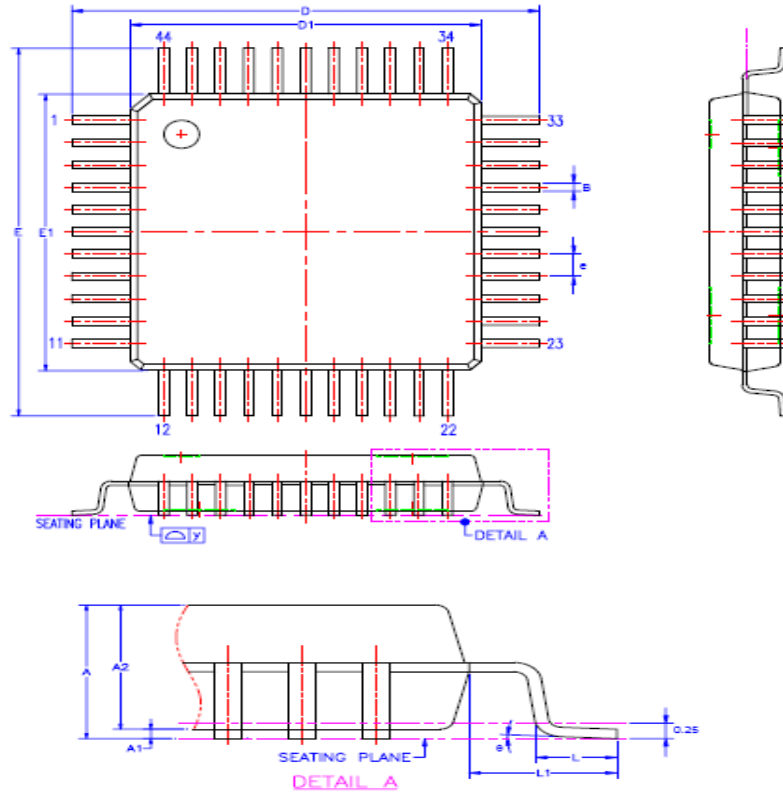


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	4.19	—	4.70	0.165	—	0.185
A1	0.51	—	0.65	0.020	—	0.026
A2	3.68	—	4.01	0.145	—	0.158
B	0.33	—	0.56	0.013	—	0.022
B1	0.66	—	0.81	0.026	—	0.032
c	0.18	—	0.33	0.007	—	0.013
D	17.27	—	17.78	0.680	—	0.700
D1	16.46	—	16.71	0.648	—	0.658
D2	14.99	—	16.00	0.590	—	0.630
E	17.27	—	17.78	0.680	—	0.700
E1	16.46	—	16.71	0.648	—	0.658
E2	14.99	—	16.00	0.590	—	0.630
e	—	1.27	—	—	0.050	—
L	2.29	—	3.05	0.090	—	0.120
y	—	—	0.10	—	—	0.004

Note:

1. Dimensions D1 & E1, do not include mold protrusion.
2. Dimension B1 does not include dambar protrusion.

44L PQFP Package Outline:



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	2.70	—	—	0.106
A1	0.05	—	0.50	0.002	—	0.020
A2	1.90	—	2.20	0.075	—	0.087
B	0.29	—	0.45	0.011	—	0.018
c	0.10	—	0.23	0.004	—	0.009
D	13.00	—	13.40	0.512	—	0.528
D1	9.90	—	10.10	0.390	—	0.398
E	13.00	—	13.40	0.512	—	0.528
E1	9.90	—	10.10	0.390	—	0.398
e	—	0.80	—	—	0.031	—
L	0.73	—	1.03	0.029	—	0.041
L1	—	1.60	—	—	0.063	—
y	—	0.10	—	—	0.004	—
θ	0°	—	7°	0°	—	7°

Note:

1. Dimensions D1 & E1, do not include mold protrusion.
2. Dimension B1 does not include dambar protrusion.