

CRD89C4051

8-bit microcontroller with 4KB Flash and 128B RAM

Product List

CRD89C4051-25, 25 MHz 4KB internal memory MCU
CRD89C4051-25, 25 MHz 4KB internal memory MCU
CRD89C4051-40, 40 MHz 4KB internal memory MCU

General Description

The CRD89C4051 series product is an 8-bit single chip microcontroller with 4KB Flash. It provides the hardware features and 8051 instruction set, necessary to make it a versatile and cost effective controller for applications demand up to 15 I/O pins in a low pin-count package.

The device can be programmed using a commercial programmer.

Ordering Information

CRD89C4051-40-SG

4KB Flash, 40 MHz, 5V, 20 SOIC

CRD89C4051-40-PG

4KB Flash, 40 MHz, 5V, 20 PDIP

CRD89L4051-25-SG

4KB Flash, 25 MHz, 3V, 20 SOIC

CRD89L4051-25-PG

4KB Flash, 25 MHz, 3V, 20 PDIP

Features

- Working voltage: 3.0V ~ 3.6V For L Version
4.5V ~ 5.5V For C Version
- 8051 family compatible
- 12 clocks per machine cycle
- 4 KB internal flash memory
- 128 bytes internal RAM
- Two 16-bit timers/counters
- 15 programmable I/O lines
- Full duplex serial UART channel
- Bit operation instruction
- Industrial temperature level
- 8-bits unsigned division
- 8-bits unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Two priority level interrupt
- Power save modes:
 - Idle mode
 - Power down mode (provide H/W wake-up function)
- Code protection function
- One watch dog timer (WDT)
- On-chip Analog Comparator
- Direct LED Drive Output (Default = 1)

Pin Configuration

Figure 1 20L PDIP Package

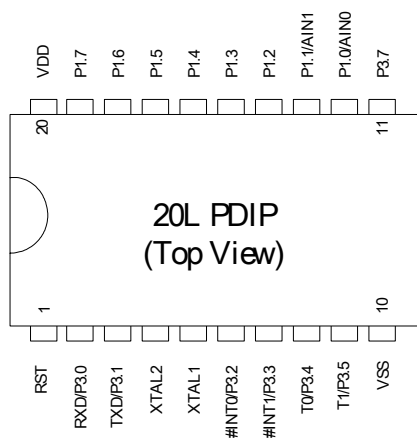
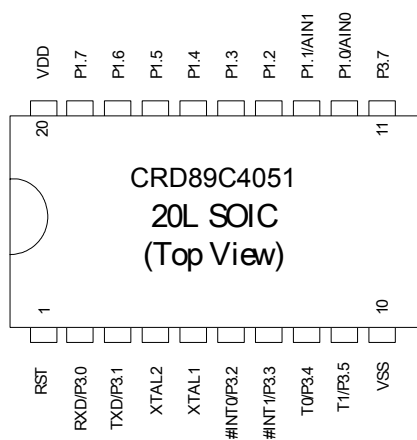
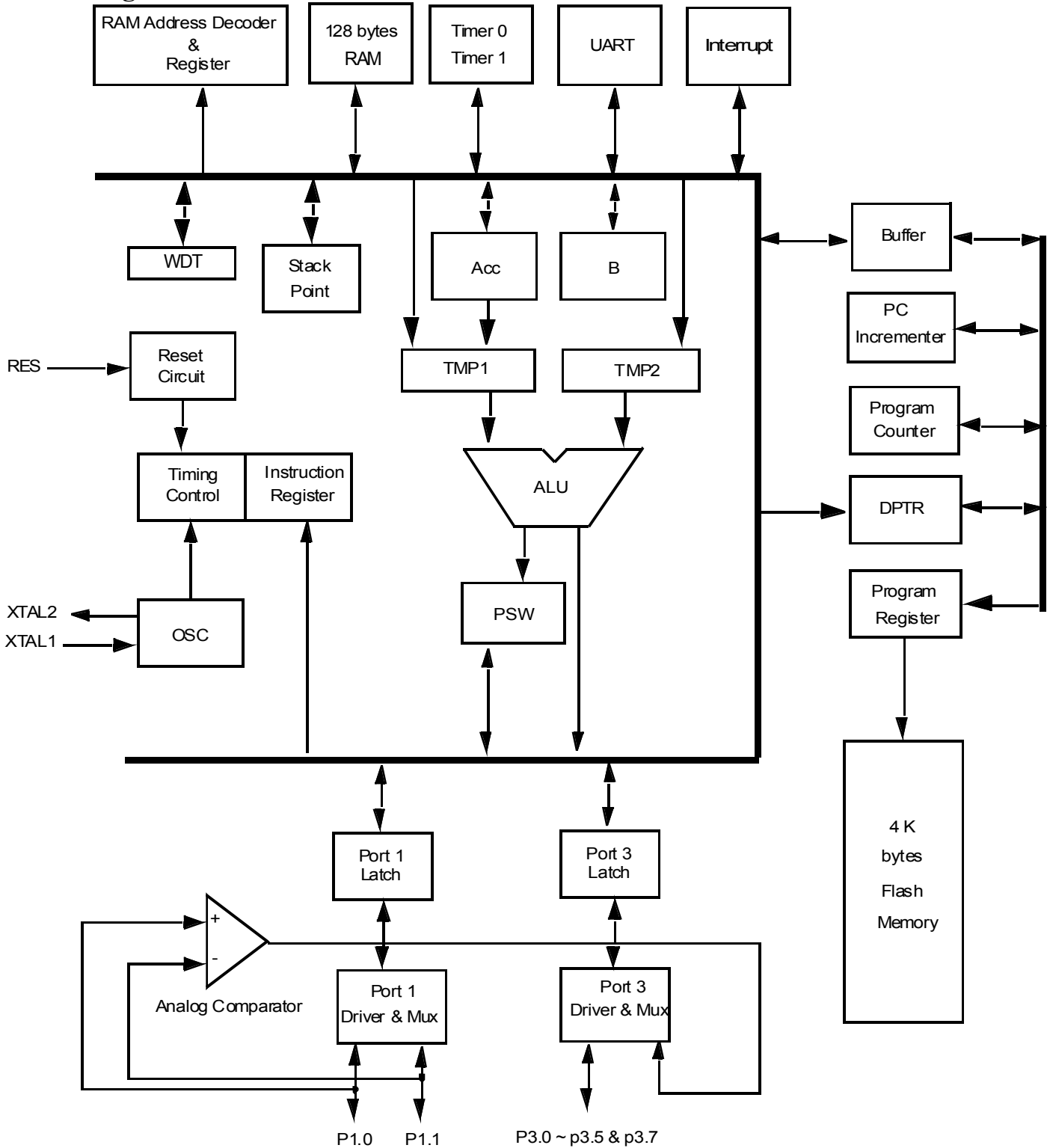


Figure 2 20L SOIC Package



Block Diagram



Pin Description (20L PDIP / 20L SOIC)

Pin	Symbol	Active	I/O	Names
1	RST	H	i	Reset
2	P3.0/RXD		i/o	bit 0 of port 3 & receive data
3	P3.1/TXD		i/o	bit 1 of port 3 & transmit data
4	XTAL2		o	Crystal out
5	XTAL1		i	Crystal in
6	P3.2/#INT0	-/L	i/o	bit 2 of port 3 & low true interrupt 0
7	P3.3/#INT1	-/L	i/o	bit 3 of port 3 & low true interrupt 1
8	P3.4/T0		i/o	bit 4 of port 3 & timer 0
9	P3.5/T1		i/o	bit 5 of port 3 & timer 1
10	VSS			Sink Voltage, Ground
11	P3.7		i/o	bit 7 of port 3
12	P1.0/AIN0		i/o	bit 0 of port 1 & positive 0 of the on chip analog comparator
13	P1.1/AIN1		i/o	bit 1 of port 1 & positive 1 of the on chip analog comparator
14	P1.2		i/o	bit 2 of port 1
15	P1.3		i/o	bit 3 of port 1
16	P1.4		i/o	bit 4 of port 1
17	P1.5		i/o	bit 5 of port 1
18	P1.6		i/o	bit 6 of port 1
19	P1.7		i/o	bit 7 of port 1
20	VDD			Drive voltage, +5 Vcc

Special Function Register (SFR) Memory Map

\$F8										\$FF
\$F0	B 0000 0000									\$F7
\$E8										\$EF
\$E0	ACC 0000 0000									\$E7
\$D8										\$DF
\$D0	PSW 0000 0000									\$D7
\$C8										\$CF
\$C0										\$C7
\$B8	IP 0000 0000								SCONF 0xxx xxxx	\$BF
\$B0	P3 1111 1111									\$B7
\$A8	IE 0000 0000									\$AF
\$A0										\$A7
\$98	SCON 0000 0000	SBUF xxxx xxxx							WDTC 0x0x x000	\$9F
\$90	P1 1111 1111			LEDENP1 0000 0000		LEDENP3 0000 0000			WDTKEY 0000 0000	\$97
\$88	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000				\$8F
\$80		SP 0000 0111	DPL 0000 0000	DPH 0000 0000	(Reserved)				PCON 0000 0000	\$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for CRD89C4051

Addr	SFR	Reset	7	6	5	4	3	2	1	0
93H	LEDENP1	00H	LEDEN P17	LEDEN P16	LEDEN P15	LEDEN P14	LEDEN P13	LEDEN P12	LEDEN P11	LEDEN P10
95H	LEDENP3	00H	LEDEN P37	Unused	LEDEN P35	LEDEN P34	LEDEN P33	LEDEN P32	LEDEN P31	LEDEN P30
97H	WDTKEY	00H	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
9FH	WDTC	0*0**000	WDTE	Reserve	CLEAR	Unused	Unused	PS2	PS1	PS0
BFH	SCONF	0*****0	WDR	Unused	Unused	Unused	Unused	Reserve	Unused	ALEI

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	□	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
VCC3.3	Supply voltage	3.0	3.3	3.6	V	
Fosc 25	Oscillator Frequency			25	MHz	For 3.3V application
Fosc 40	Oscillator Frequency			40	MHz	For 5.0V application

DC Characteristic

VCC = 5V (±10%), VSS=0V TA= -40°C to 85°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
VCC	Supply Voltage		4.5	5.5	V
ICC	Supply current operating	See notes 1 $f_{CLK} = 12\text{MHz}$ VCC = 5.5V		15	mA
IID	Supply current IDLE Mode	See note 2 $f_{CLK} = 12\text{MHz}$ VCC = 5.5V P1.0 & P1.1 =0V		5	mA
IPD	Supply current Power-Down MODE	See note 3 ; VCC (= 5.5V) P1.0 & P1.1 =0V		20	μA
INPUT					
VIL1	Input LOW voltage, P1, P3		-0.5	0.8	V
VIL2	Input LOW voltage, RES, XTAL1		0	0.8	V
VIH1	Input HIGH voltage, P1, P3		2.0	Vcc+0.5	V
VIH2	Input HIGH voltage, RES, XTAL1		70%VCC	Vcc+0.5	V
IIL	Input current LOW level, P3.0~P3.5, P3.7	VIN = 0.45V		-50	μA
ITL	Transition current High to Low, P3.0~P3.5, P3.7	VIN = 2.0 V		-650	μA
ILI	Input leakage current, P1.0~P1.1	0.45V < VIN < VCC-0.3V		±10	μA
OUTPUT					
VOL1	Output LOW voltage, P1.2~P1.7, P3.0~P3.5, P3.7	IOL = 8mA , VCC=5.0V		0.45	V
VOL2	Output LOW voltage, P1.0~P1.1	IOL = 6.5mA , VCC =5.0V		0.45	V
VOH1	Output High voltage, P3.0~P3.5, P3.7	IOH = -80uA , VCC =5.0V	2.4		V
	Output High voltage, P1.2~P1.7	IOH = -80uA , VCC =5.0V	2.4		V
ISK1	Sink Current P1, P3	VCC = 5.0V, VIN = 0.4 V		6	mA
ISK2	Sink Current P1, P3 (LEDD Enable)	VCC = 5.0V, VIN = 0.4 V		20	mA
ISR1	Source Current P1, P3	VCC = 5.0V, VIN = 2.4 V		-150	uA
RRST	Internal RESET pull-down resistor	VIN = 5.0 V	50	300	kΩ
CIO	Pin capacitance	Test freq=1MHz, TA=25°C		10	pF

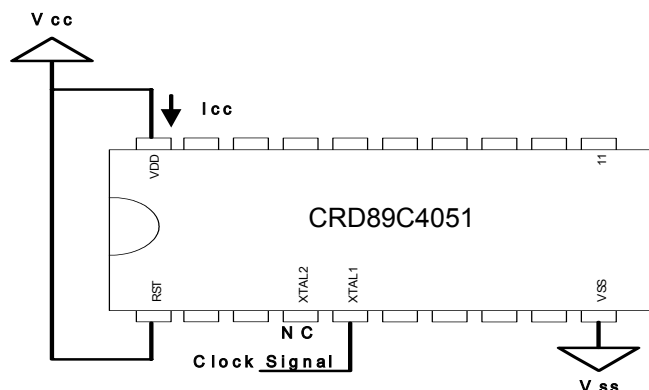
VCC = 3.3V ($\pm 10\%$), VSS=0V, TA= -40°C to 85°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
VCC	Supply Voltage		3.0	3.6	V
ICC	Supply current operating	See note 1 $f_{CLK} = 12\text{MHz}$ VCC = 3.6V		5.5	mA
IID	Supply current IDLE Mode	See note 2 $f_{CLK} = 12\text{MHz}$ VCC = 3.6V P1.0 & P1.1 =0V		2	mA
IPD	Supply current Power-Down MODE	See note 3 : VCC (= 3.6V) P1.0 & P1.1 =0V		5	μA
INPUT					
VIL1	Input LOW voltage, P1, P3	VCC = 3.6V	0	0.2 VCC -0.2	V
VIL2	Input LOW voltage, RST	VCC = 3.6V	0	0.2 VCC -0.2	V
VIL3	Input LOW voltage, XTAL1	VCC = 3.6V	0	0.2 VCC -0.2	V
VIH1	Input HIGH voltage, P1, P3	VCC = 3.6V	0.6 VCC -0.4	VCC + 0.2	V
VIH2	Input HIGH voltage, RST	VCC = 3.6V	0.6 VCC -0.4	VCC + 0.2	V
VIH3	Input HIGH voltage, XTAL1	VCC = 3.6V	0.8 VCC	VCC + 0.2	V
IIN1	Input current LOW level P1, P3	VCC = 3.0V ~3.6V, VIN = 0.45V.	-10	50	μA
ITL	Transition current High to Low P3.0~P3.5, P3.7	See note 4 VCC = 3.6V, VIN = 2.0 V	-75	400	μA
ILI	Input leakage current P1.0~P1.1	VCC = 3.0V ~3.6V, 0.45V<VIN<VCC	-10	10	μA
OUTPUT					
VOL1	Output LOW voltage, P1.2~P1.7, P3.0~P3.5, P3.7	IOL = 6mA , VCC =3.3V		0.4	V
VOL2	Output Low voltage P1.0~P1.1	IOL = 5mA , VCC =3.3V		0.4	V
VOH1	Output High voltage P3.0~P3.5, P3.7	IOH =-30uA , VCC =3.3V	2.4		V
	Output High voltage, P1.2~P1.7	IOH =-30uA , VCC =3.3V	2.4		V
ISK1	Sink Current P1, P3	VCC = 3.3V, VIN = 0.4 V		4	mA
ISK2	Sink Current P1, P3 (LEDD Enable)	VCC = 3.3V, VIN = 0.4 V		12	mA
ISR1	Source Current P1, P3	VCC = 3.3V, VIN = 2.4 V		-80	μA
RRST	Internal RESET pull-down resistor		50	300	k Ω
CIO	Pin capacitance	Test freq=1MHz, TA=25°C		10	pF

NOTES FOR DC ELECTRICAL CHARACTERISTICS

- The operating supply current is measured with all outputs disconnected;
XTAL1 driven with $t_r = t_f = 5\text{ns}$; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect;
- The IDLE MODE supply current is measured with all output pins disconnected;
XTAL1 driven with $t_r = t_f = 5\text{ns}$; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect;
- The POWER-DOWN MODE supply current is measured with all output pins disconnected;
VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect;
- Port 1, 3 source transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when VIN is approximately 2V.
- Under steady state (non-transient) conditions, IOL must be externally Limited as follows: Maximum IOL per port pin: 20mA
Maximum total IOL for all output pins: 80mA

ICC Active Mode Test Circuit:



AC Characteristic

VCC=3.3V±10%, VSS=0V, tclk min = 1/ fmax(maximum operating frequency)
TA= -40°C to +85°C

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
External Clock drive into XTAL1					
tCLK	4	Xtal1 Period	40(Note1)	-	ns
tCLKH	4	Xtal1 HIGH time	20	-	ns
tCLKL	4	Xtal1 LOW time	20	-	ns
tCLKR	4	XTAL1 rise time	-	10	ns
tLLIV	4	XTAL1 fall time	-	10	ns
tCYC	4	Controller cycle time = tCLK / 12	3.33	-	ns

NOTES:

- Operating at 25MHz.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
UART					
tXLXL	5	Serial port clock time	12tCLK		ns
tQVXH	5	Output data setup to clock rising edge	10tCLK-133		ns
tXHQX	5	Output data hold after clock rising edge	2tCLK-117		ns
tXHDX	5	Input data hold after clock rising edge	0		ns
tXHDV	5	Clock rising edge to input data valid		10tCLK-133	ns

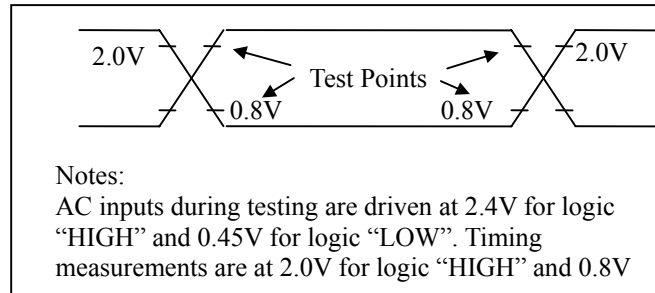


Figure 4 AC Testing Input/Output

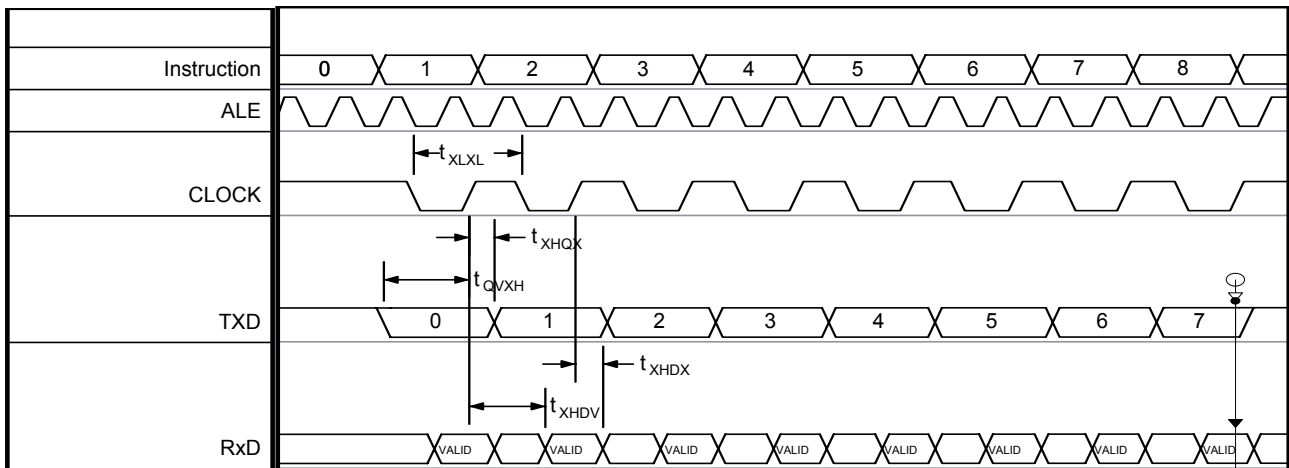


Figure 5 UART waveform in Shift Register MODE

Instruction Set

The CRD89C4051 uses the powerful instruction set of 80C51. It consists of 45 single-byte, 47 two-byte, and 15 three-byte instructions. Among them 65 instructions are executed in 1 machine-cycle, 40 instructions in 2 machine-cycles, and the multiply, 2 instructions in 4 machine-cycles.

A summary of the instruction set is given in Table 3.

Addressing Mode

Notes on instruction set and address modes:

Rn		Register R7-R0 of the currently selected register bank
direct		8-bits internal data location's address. This could be internal DATA RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)]
@Ri		8-bits RAM location addressed indirectly through register R1 or R0 of the actual register bank
#data		8-bits constant included in the instruction
#data16		16-bits constant included in the instruction
addr11		11-bits destination address. Used by ACALL and AJMP. The branch can be anywhere within the same 2 Kbytes page of program memory as the first byte of the following instruction.
rel		Signed (2's complement) 8-bits offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit		Direct addressed bit in internal data RAM or SFR

Table 3: A Summary of the instruction set

Mnemonic		OPERATION	BYTE	CYCLE
Arithmetic Instructions				
ADD	A,Rn	$A = A + Rn$	1	1
ADD	A,direct	$A = A + \text{direct}$	2	1
ADD	A,@Ri	$A = A + \langle @Ri \rangle$	1	1
ADD	A,#data	$A = A + \#data$	2	1
DDC	A,Rn	$A = A + Rn + C$	1	1
ADDC	A,direct	$A = A + \text{direct} + C$	2	1
ADDC	A,@Ri	$A = A + @Ri + C$	1	1
ADDC	A,#data	$A = A + \#data + C$	2	1
SUBB	A,Rn	$A = A - Rn - C$	1	1
SUBB	A,direct	$A = A - \text{direct} - C$	2	1
SUBB	A,@Ri	$A = A - \langle @Ri \rangle - C$	1	1
SUBB	A,#data	$A = A - \#data - C$	2	1
INC	A	$A = A + 1$	1	1
INC	Rn	$Rn = Rn + 1$	1	1
INC	direct	$\text{direct} = \text{direct} + 1$	2	1
INC	@Ri	$\langle @Ri \rangle = \langle @Ri \rangle + 1$	1	1
DEC	A	$A = A - 1$	1	1
DEC	Rn	$Rn = Rn - 1$	1	1
DEC	direct	$\text{direct} = \text{direct} - 1$	2	1
DEC	@Ri	$\langle @Ri \rangle = \langle @Ri \rangle - 1$	1	1
INC	DPTR	$DPTR = DPTR - 1$	1	2
MUL	AB	$B:A = A \times B$	1	4
DIV	AB	$A = \text{INT}(A/B)$ $B = \text{MOD}(A/B)$	1	4
DA	A	Decimal adjust ACC	1	1
Logical Instructions				
ANL	A,Rn	$A .AND. Rn$	1	1
ANL	A,direct	$A .AND. \text{direct}$	2	1
ANL	A,@Ri	$A .AND. \langle @Ri \rangle$	1	1
ANL	A,#data	$A .AND. \#data$	2	1
ANL	direct,A	$\text{direct} .AND. A$	2	1
ANL	direct,#data	$\text{direct} .AND. \#data$	3	2
ORL	A,Rn	$A .OR. Rn$	1	1
ORL	A,direct	$A .OR. \text{direct}$	2	1
ORL	A,@Ri	$A .OR. \langle @Ri \rangle$	1	1
ORL	A,#data	$A .OR. \#data$	2	1
ORL	direct,A	$\text{direct} .OR. A$	2	1
ORL	direct,#data	$\text{direct} .OR. \#data$	3	2
XRL	A,Rn	$A .XOR. Rn$	1	1
XRL	A,direct	$A .XOR. \text{direct}$	2	1
XRL	A,@Ri	$A .XOR. \langle @Ri \rangle$	1	1
XRL	A,#data	$A .XOR. \#data$	2	1
XRL	direct,A	$\text{direct} .XOR. A$	2	1
XRL	direct,#data	$\text{direct} .XOR. \#data$	3	2
CLR	A	$A = 0$	1	1
CPL	A	$A = /A$	1	1
RL	A	Rotate ACC Left 1 bit	1	1
RLC	A	Rotate Left through Carry	1	1
RR	A	Rotate ACC Right 1 bit	1	1
RRC	A	Rotate Right through Carry	1	1
SWAP	A	Swap Nibbles in A	1	1

Data Transfers Instructions				
MOV	A,Rn	A = Rn	1	1
MOV	A,direct	A = direct	2	1
MOV	A,@Ri	A = <@Ri>	1	1
MOV	A,#data	A = #data	2	1
MOV	Rn,A	Rn = A	1	1
MOV	Rn,direct	Rn = direct	2	2
MOV	Rn,#data	Rn = #data	2	1
MOV	direct,A	direct = A	2	1
MOV	direct,Rn	direct = Rn	2	2
MOV	direct,direct	direct = direct	3	2
MOV	direct,@Ri	direct = <@Ri>	2	2
MOV	direct,#data	direct = #data	2	1
MOV	@Ri,A	<@Ri> = A	1	1
MOV	@Ri,direct	<@Ri> = direct	2	2
MOV	@Ri,#data	<@Ri> = #data	2	1
MOV	DPTR,#data16	DPTR = #data16	3	2
MOVC	A,@A+DPTR	A = code memory[A+DPTR]	1	2
MOVC	A,@A+PC	A = code memory[A+PC]	1	2
PUSH	direct	INC SP: MOV "@SP", <direct >	2	2
POP	direct	MOV <direct >, "@SP": DEC SP	2	2
XCH	A,Rn	ACC and < Rn > exchange data	1	1
XCH	A,direct	ACC and < direct > exchange data	2	1
XCH	A,@Ri	ACC and < Ri > exchange data	1	1
XCHD	A,@Ri	ACC and @Ri exchange low nibbles	1	1
Boolean Instructions				
CLR	C	C = 0	1	1
CLR	bit	bit = 0	2	1
SETB	C	C = 1	1	1
SETB	bit	bit = 1	2	1
CPL	C	C = /C	1	1
CPL	bit	bit = /bit	2	1
ANL	C,bit	C = C .AND. bit	2	2
ANL	C,/bit	C = C .AND. /bit	2	2
ORL	C,bit	C = C .OR. bit	2	2
ORL	C,/bit	C = C .OR. /bit	2	2
MOV	C,bit	C = bit	2	1
MOV	bit,C	bit = C	2	2
JC	rel	Jump if C= 1	2	2
JNC	rel	Jump if C= 0	2	2
JB	bit,rel	Jump if bit = 1	3	2
JNB	bit,rel	Jump if bit = 0	3	2
JBC	bit,rel	Jump if C = 1	3	2
Jump Instructions				
ACALL	addr11	Call Subroutine only at 2k bytes Address	2	2
LCALL	addr16	Call Subroutine in max 64K bytes Address	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Jump only at 2k bytes Address	2	2
LJMP	addr16	Jump to max 64K bytes Address	3	2
SJMP	rel	Jump on at 256 bytes	2	2
JMP	@A+DPTR	Jump to A+ DPTR	1	2
JZ	rel	Jump if A = 0	2	2
JNZ	rel	Jump if A ≠ 0	2	2
CJNE	A, direct,rel	Jump if A ≠ < direct >	3	2
CJNZ	A, #data,rel	Jump if A ≠ < #data >	3	2
CJNZ	Rn, #data,rel	Jump if Rn ≠ < #data >	3	2

CJNZ	@Ri, #data,rel	Jump if @Ri \neq <#data >	3	2
DJNZ	Rn,rel	Decrement and jump if Rn not zero	2	2
DJNZ	direct,rel	Decrement and jump if direct not zero	3	2
NOP		No Operation	1	1

Branching instructions:

When the programmer executes branching instructions like AJMP, LJMP, ACALL, LCALL, SJMP etc..., they need to ensure that the destination branching address isn't over the internal program memory size. The CRD89C4051 contains 4K bytes of program memory between location 00H to 0FFFH.

Data Memory, MOVX-related instructions:

The CRD89C4051 contains 128 bytes of internal data memory and doesn't support external data memory access. Therefore, the CRD89C4051 doesn't include MOVX instructions.

Limited on down mode wake-up

The CRD89C4051 has two ways to wake-up from power down mode. One is by hardware reset. The other one is by using the external interrupt (#INT0, #INT1) to wake-up from power down. The external interrupt must be set for level trigger.

I/O Pin Configuration

Port 1:

Ports P1.2 to P1.7 have internal pull-up resistors. Ports P1.0 to P1.1 are open-drain configuration, so they require external pull-up resistors to pull low. P1.0 and P1.1 also use a positive input (AIN0) and a negative input (AIN1) of the on chip analog comparator. As long as the voltage level of P1.0 is greater than P1.1, the output voltage level of the on-chip analog comparator is "1" and this result is stored in bit 6 of port 3 SFR.

Port 3:

Port 3 is 7-bits bi-directional I/O pins which include P3.0 to P3.5 and P3.7. P3.6 isn't used as a general purpose I/O pin and the output pin of the on-chip analog comparator connects to the P3.6 which is hard-wired as an input.

I/O are provided with LED driving capacity

LEDEN (LEDENP1, 93H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDEN P17	LEDEN P16	LEDEN P15	LEDEN P14	LEDEN P13	LEDEN P12	LEDEN P11	LEDEN P10

LEDEN (LEDENP3, 95H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDEN P37	Unused	LEDEN P35	LEDEN P34	LEDEN P33	LEDEN P32	LEDEN P31	LEDEN P30

When I/O Ports (Port1 & Port3) output are low, they are provided with more sink current (IIL about 20mA) to drive an LED by setting the LED enable bit. For example, when setting LEDNP1 [0] to high then P1.0 is provided with more sink current (IIL) to drive the LED. Each I/O can be set to drive an LED by setting correspondent register.

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit, free-running counter that generates a reset signal if the counter overflows. The WDT is useful for systems that are susceptible to noise, power glitches, or electronics discharges which cause software dead loop or runaway conditions. The WDT function can help a user’s software recover from abnormal software conditions. The WDT is different from Timer0 and Timer1 of the general 8051. To prevent the WDT reset is done by the user’s software periodically clearing the WDT counter. The user should check WDR bit of SCONF register whenever unexpected resets happen.

The purpose of this procedure is to prevent the WDTC value from being changed when the system is on a runaway condition. There is a 250 KHz RC oscillator embedded in the chip. Set WDTE = “1” will enable this RC oscillator which is frequency independent from the system frequency clock. The WDT is enabled by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE is set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when it overflows. The WDTE bit will then be cleared to 0 automatically when the CRD89C4051 has been reset, either by a hardware reset or a WDT reset. The WDT is reset by setting 1 to the CLEAR bit of WDTC before the counter overflow occurs. This will clear the contents of the 16-bit counter and let the counter re-start the count from the beginning.

Watch Dog Timer Registers

Watch Dog Key Register

WDTKEY (\$97)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0

By default, the WDTC is read only. User needs to write values 1EH, 0E1H sequentially to the WDTKEY (97H) register to enable the WDTC write attribute, which is

```
MOV WDTKEY, # 01EH
MOV WDTKEY, # 0E1H
```

When WDTC is set, the user needs to write another value E1H, 1EH sequentially to the WDTKEY (97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # 0E1H
MOV WDTKEY, # 01EH
```

Watch Dog Timer Registers - WDT Control Register

WDTC (\$9F)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTE	Reserve	CLEAR	Unused	Unused	PS2	PS1	PS0

WDTE: Watch Dog Timer enable bit

CLEAR: Watch Dog Timer reset bit

If CLEAR bit set to1, Watch Dog Timer will be reset. User don’t reset value to 0 .

PS [2:0] : Overflow period select bits

PS2~PS0: clock sourer divider bit

PS [2:0]	Overflow Period (ms)
000	2.048

001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.14

Watch Dog Timer Register - System Control Register

SCONF (\$BFH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDR	Unused	Unused	Unused	Unused	Reserved	Unused	Unused

WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1

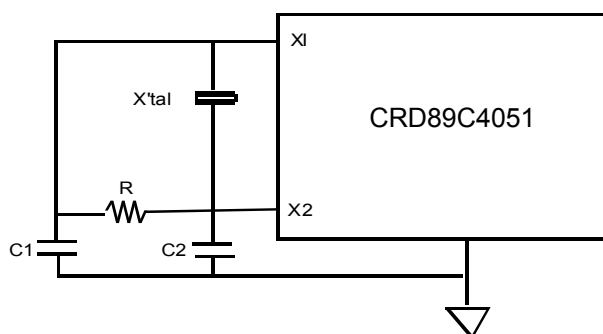
ALEI: ALE output inhibit bit, to reduce EMI

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted resets occur.

Application Reference

Valid for CRD89C4051				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62K \square	6.8K \square	4.7K \square



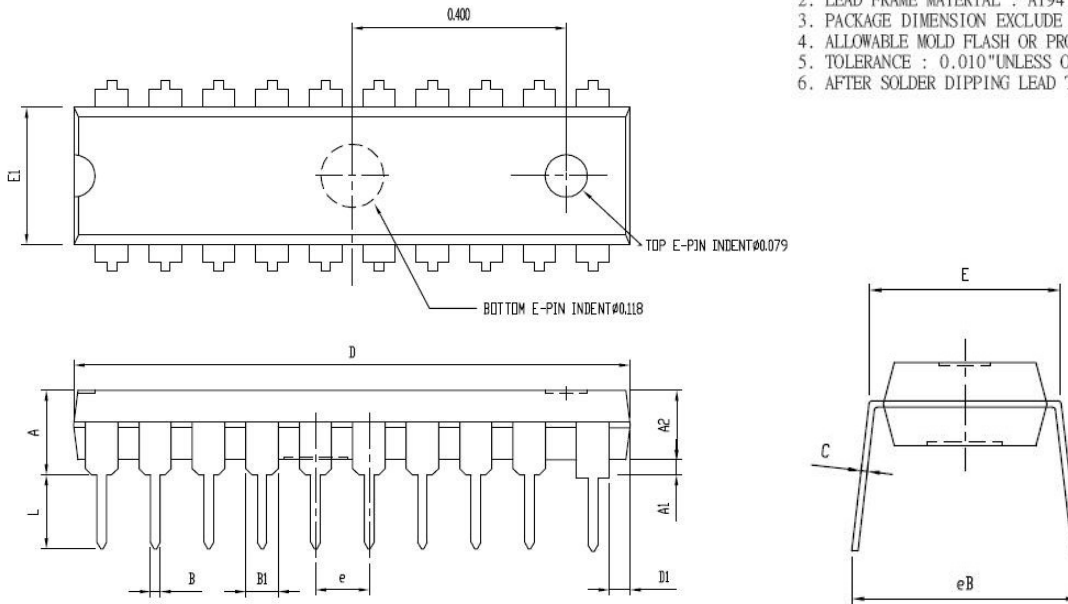
Note:

Oscillation circuit may differ with a different crystal or a ceramic resonator in higher oscillation frequency which is due to each crystal or ceramic resonator having its own unique characteristics. The user should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

20-Pin 300 mil PDIP Information

NOTE:

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : A194
3. PACKAGE DIMENSION EXCLUDE MOLD FLASH OR PROTRUSION.
4. ALLOWABLE MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010"
5. TOLERANCE : 0.010"UNLESS OTHERWISE SPECIFIED.
6. AFTER SOLDER DIPPING LEAD THICKNESS WILL BE 0.020"MAX.



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	—	3.30	3.56	—	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	26.32	26.416	26.52	1.036	1.040	1.044
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	—	8.26	0.300	—	0.325
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.65	0.330	—	0.380

20-Pin 300 mil SOIC Information

